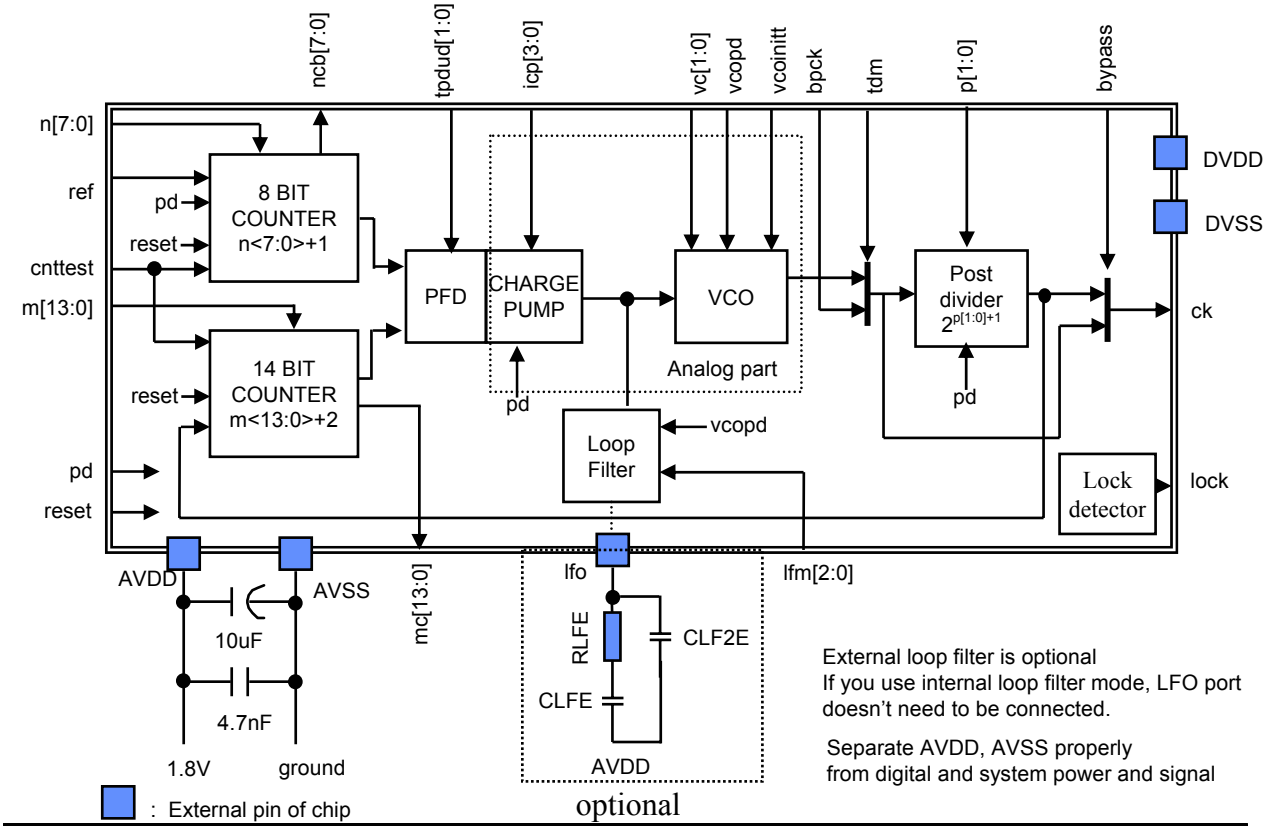
## 1. General Description

The H18GPL11S is a 1.8V CMOS (0.18㎛ 1-poly, 3-metal) analog programmable frequency synthesizer based on charged pump type PLL for an on-chip application using Hynix standard 0.18㎛ ASIC Process. H18GPL11S has 5MHz to 320MHz output range. Operating frequency and loop characteristics of PLL are fully programmable.

## 2. Features

- On-chip charge pump type PLL clock generator
- Input reference clock range : 5MHz ~ 100MHz
- Clock output frequency range : 5MHz ~ 160MHz( extend to 320MHz )
- Reference divider range : 1 ~ 256 ( 8-bit programmable divider)
- Feedback divider range : 3 ~ 16386 ( 14-bit programmable divider)
- 8 mode programmable loop filter
- programmable VCO range and VCO gain( 2-bit )
- programmable PD gain ( 2-bit )
- Maximum Power consumption : 12mW
- Process : 0.18 ㎛ CMOS generic Process( 1-poly, 3-metal )
- Cell Size : 740㎛ x 816㎛( with guard ring )

## 3. Block Diagram and Recommended Application Circuits



## 4. Pin Descriptions

| Pin Name | Type | Description |
|---|---|---|
| DVDD | Power | Digital power supply |
| DVSS | Ground | Digital ground |
| AVDD | Power | Analog power supply |
| AVSS | Ground | Analog ground |
| ASUB | Ground | Guard ring ground |
| ref | Input | PLL reference clock input signal |
| bpck | Input | Bypass clock input signal |
| pd | Input | PLL power down mode except VCO : active high |
| vcopd | Input | VCO power down mode : active high |
| bypass | Input | Bypass mode : active high |
| tdm | Input | Digital part test mode : active high |
| reset | Input | Digital part reset signal : active high |
| vcoinit | Input | VCO initialize signal : active high |
| cnttest | Input | Counter toggle test : active high |
| tpdud[1:0] | Input | Charge pump test mode( Normal mode : “00”) |
| m[13:0] | Input | Feedback divisor is M[13:0]+2 |
| n[7:0] | Input | Reference divisor is N[7:0]+1 |
| p[1:0] | Input | Post divisor is $2^{P[1:0]+1}$ |
| vc[1:0] | Input | VCO range control vector |
| icp[3:0] | Input | Charge pump bias current control vector |

| Pin Name | Type | Description |
|---|---|---|
| lfm[2:0] | input | loop filter mode selector |
| lfo | Analog | External loop filter port |
| ck | Output | PLL output clock |
| lock | Output | PLL lock detect signal : active high |
| ncb[7:0] | Output | Reference divider test output |
| mc[13:0] | Output | Feedback divider test output |

## 5. Function Descriptions

H18GPL11S is ideally suited to provide the graphics system clock signals required by video signal AD and DA. Fully Programmable feedback and reference divider capability allow virtually any frequency to be generated, not just simple multiples of reference frequency. Also PD gain, VCO gain and VCO range are programmable for user-define PLL characteristics.

### (1) Determining Output Frequency

H18GPL11S generates its output frequencies using charge pump PLL techniques. Then The output frequency is ratiometrically related to the reference frequency.

a) Normal Frequency mode

Output frequency range : 5MHz ~ 160MHz

* PLL control setting

TDM = “low”, BYPASS = “low”

At this condition, the output frequency, F(ck), is actually determined by the following equation.

$$F(ck) = \frac{F(ref) \cdot (\text{Feedback Divisor})}{(\text{Reference Divisor})}$$

F(ck) : frequency of output, **ck**

F(ref) : frequency of reference pin, **ref**

Feedback Divisor : **m[13:0]** +2

Reference Divisor : **n[7:0]** +1

* F(ck) range is showed section 3).

F(ref) range is restricted by loop filter mode at section 4).

b) Extended Frequency mode

* PLL control setting

TDM = “low”, BYPASS = “high”

At this condition, the output frequency, F(ck), is actually determined by the following equation.

$$F(ck) = \frac{F(ref) \cdot (\text{Feedback Divisor}) \cdot (\text{Post divisor})}{(\text{Reference Divider})}$$

Pre divisor : $2^{p[1:0]+1}$

Table. F(ck) range at extended frequency range

| vc[1:0] | F(ck) | |
|---|---|---|
| | min | max |
| 00 | 80MHz | 200MHz |
| 01 | 120MHz | 240MHz |
| 10 | 160MHz | 280MHz |
| 11 | 200MHz | 320MHz |

## (2) PD gain programming

H18GPL11S provides various PD gain. Actually PD gain is controlled internally by charge pump current. At charge pump PLL, PD gain is charge pump current over 2π. H18GPL11S controls charge pump current by 4-bit resolution with the following equations.

$$ICP = (ICPB/16) \cdot (16 - \mathbf{icp[3:0]}) \quad [A]$$

$$Kpd = ICP / 2\pi \quad [A/rad]$$

ICPB : Charge pump reference current. Typically 40uA

ICP : Charge pump current

Kpd : PD gain

## (3) VCO range and gain programming

H18GPL11S provides 4 different VCO ranges and a post divider. VCO ranges are controlled by **vc[1:0]** and clock output frequency is divided by 2 power ( **p[1:0]** +1) then clock output range has 16 ranges. The gain of VCO which is the ratio of input voltage v.s. clock output frequency variation, Kvcop, has 4 different values. Following table shows each range by **vc[1:0]** and Kvcop.

| vc[1:0] | p[1:0] | Fck | | Kvcop |
|---|---|---|---|---|
| | | min | max | |
| 00 | 00 | 40MHz | 100MHz | 150MHz/V |
| | 01 | 20MHz | 50MHz | 75MHz/V |
| | 10 | 10MHz | 25MHz | 37.5MHz/V |
| | 11 | 5MHz | 12.5MHz | 18.75MHz/V |
| 01 | 00 | 60MHz | 120MHz | 150MHz/V |
| | 01 | 30MHz | 60MHz | 75MHz/V |
| | 10 | 15MHz | 30MHz | 37.5MHz/V |
| | 11 | 7.5MHz | 15MHz | 18.75MHz/V |
| 10 | 00 | 80MHz | 140MHz | 150MHz/V |
| | 01 | 40MHz | 70MHz | 75MHz/V |
| | 10 | 20MHz | 35MHz | 37.5MHz/V |
| | 11 | 10MHz | 17.5MHz | 18.75MHz/V |
| 11 | 00 | 100MHz | 160MHz | 150MHz/V |
| | 01 | 50MHz | 80MHz | 75MHz/V |
| | 10 | 25MHz | 40MHz | 37.5MHz/V |
| | 11 | 12.5MHz | 20MHz | 18.75MHz/V |

## (4) Programmable loop filter

H18GPL11S has 7 internal loop filter mode, and an external loop filter mode, totally 8 mode. Following table shows each loop filter mode characteristics. Figure 1 represents loop filter schematic.

Table. Loop Filter device value

| lfm[2:0] | RLF [Ohm] | CLF [pF] | CLF2 [pF] | ZERO [kHz] | POLE [kHz] |
|---|---|---|---|---|---|
| 000 | 40k | 1437 | 96.4 | 2.77 | 44.0 |
| 001 | 24.1k | 1437 | 96.4 | 4.6 | 73.1 |
| 010 | 40k | 518 | 35.8 | 7.68 | 118.8 |
| 011 | 24.1k | 518 | 35.8 | 12.75 | 197.2 |
| 100 | 24.1k | 310 | 22 | 21.3 | 321.5 |
| 101 | 14.7k | 310 | 22 | 34.9 | 527 |
| 110 | 8.9k | 310 | 22 | 57.7 | 871 |
| 111 | External loop filter | | | | |

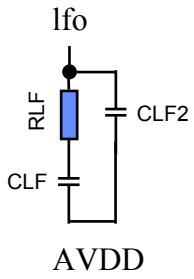



Figure 1. loop filter schematic.

In H18GPL11S, to get sufficient stability margin and efficient loop characteristics, loop filter mode(LFM) must be selected properly. Each LFM restricts feedback divisor and reference frequency ranges. At internal loop filter mode( lfm : 000 to 110), PD reference input frequency(F(ref)/(Ref divisor)) is 150kHz to 20MHz. In this mode external loop filter and **lfo** pin are not needed. If PD ref frequency is smaller than 150kHz, the external mode ( lfm : 111) must be selected to get sufficient loop stability. However, it is recommended that PD reference input frequency is bigger than 2MHz for low jitter frequency synthesis.

Following equation shows relation of loop filter and PLL loop characteristics.

$$Kpll = \frac{Kvcop*Kpd*RLF}{\mathbf{m[13:0]}+2} \quad [Hz/s] : \text{PLL loop gain}$$

$$Zero1 = 1/(2\pi*RLF*CLF) \quad [Hz] : \text{Open loop first zero}$$

$$Pol3 = (CLF+CLF2)/(2\pi*RLF*CLF*CLF2) \quad [Hz] : \text{Open loop third pole}$$

Kpll is restricted by PD ref frequency, loop filter zero1, and pole3 according to the following equation.

Kpll < (PD ref frequency)/6

Kpll > 1.5*zero1

Kpll < 0.7*pole3

Typically Kpll is recommended smaller than Fpdref/10, Kpll is lager than 2*zero1, and Kpll is smaller than 0.5*pole3 to get sufficient stability margin.

## (5) PLL power down, VCO power down and VCO initialization

H18GPL11S has PLL power down mode, VCO power down mode, and VCO initialize mode. **pd** signal is PLL power down. When **pd** is active( active high), H18GPL11S digital circuits do not operate and the charge pump circuit is disabled. v**copd** signal means VCO power down. When **vcopd** is active(active high), VCO does not oscillate. **vcoinit** is VCO initializing signal. During power-up sequence, **vcoinit** must be activated. To ensure the proper operation of the H18GPL11S, the activation of **vcoinit** signal is required just after the deactivation of the **vcopd** signal. If you want use external VCO, **vcopd** is active only. Following figure 2 is a configuration of external VCO mode.

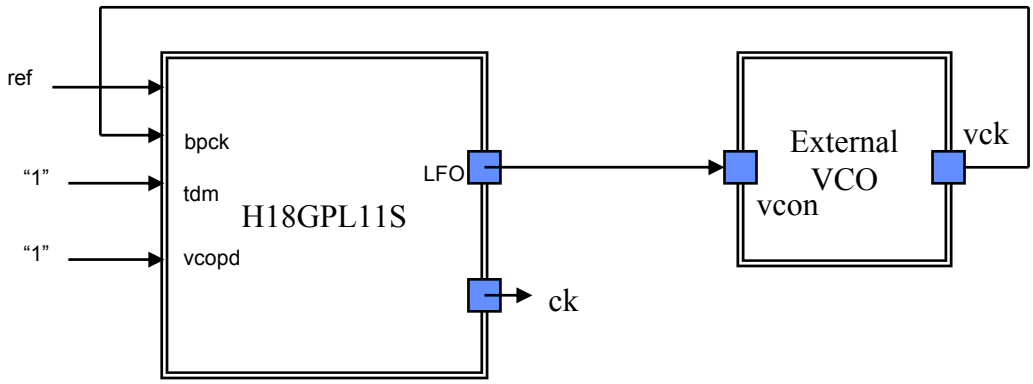



Figure 2. External VCO configuration block diagram

At this mode, frequency of **ck** is determined by section 1.a), and frequency of **vck** is determined by section 1.b)

## (6) Bypass mode

H18GPL11S has bypass mode for test main block of chip. When **bypass** signal and **tdm** is active(active high), PLL output clock is **bpck**.

## (7) Digital block test mode

At mass product test, H18GPL11S provides digital block test. When **tdm** is active(active high), **bpck** clock is provided to the whole digital blocks in H18GPL11S and check **mc[13:0]** and **ncb[7:0]** . If **cnttest** is high, internal counter is toggle each bit by m, or n.

## (8) VCO block and Charge pump test mode

At mass product test, **tpdud[1:0]** enables you to access the VCO control voltage directly from off-chip to get VCO gain and to measure charge pump up or down currents.

## (9) H18PL11S control modes summary

Table. Mode settings of H18GPL11S

tpdud[1:0] = “00”, tvco[1:0] = “00”, reset = “0”

| MODE | pd | by pass | tdm | vcopd | vcoinit | DESCRIPTION |
|---|---|---|---|---|---|---|
| Normal mode | 0 | 0 | 0 | 0 | 0 | Fck = Fref*(m+2)/(n+1) |
| Extended mode | 0 | 1 | 0 | 0 | 0 | Fck = Fref*(m+2)*2 $^{P+1}$/(n+1) |
| Bypass mode | 0 | 1 | 1 | 0 | 0 | CK = ~BPCK |
| vco initialize mode | 0 | 0 | 0 | 0 | 1 | When power turn on, vcoinit must be activated |
| Power down mode | 1 | 0 | 0 | 1 | 0 | H18GPL11S is disabled at this mode |
| External VCO mode | 0 | 0 | 1 | 1 | 0 | Using External VCO |
| Digital part test | 0 | 0 | 1 | 0 | 0 | digital part toggle test( cnttest = 1) |

Table. VCO and charge pump test mode

p[1:0] = “11”, pd = “0”, BYPASS = “0”, reset = “0”,tdm = “0”

vcopd = “0”, vcoinit = “0”

| tpdud | DESCRIPTION |
|---|---|
| 00 | Charge pump normal mode operation |
| 01 | Charge pump down current test, or VCO maximum frequency test |
| 10 | Charge pump up current test, or VCO minimum frequency test |
| 11 | **lfo** pin is high impedance, for charge pump and loop filter leakage test |

## 6. Operating Conditions

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| DVDD | Power Supply | 1.6 | 2.0 | V |
| AVDD | | 1.6 | 2.0 | V |
| DVSS-AVSS | | 0 | 50 | mV |
| ASUB | Guarding Ground | 0 | 50 | mV |
| Top | Operating temperature | 0 | 100 | ℃ |

## 7. Electrical Characteristics

| SYMBOL | ITEM | CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Idd | PLL dynamic current | @F(vco)=100MHz | 3 | 4 | 6 | mA |
| Fckn | Output frequency | Normal Range | 5 | - | 160 | MHz |
| Fckh | Output frequency | Extended Range | 80 | - | 320 | MHz |
| Dtn | Output duty cycle | Normal Range | 45 | 50 | 55 | % |
| Dtht | Output duty cycle | Extended Range | 40 | 50 | 60 | % |
| Tpolock | Power on lock time | When power turn on | - | - | 10 | msec |
| Tlock | Lock time in lock range | Lock state, Internal loop filter mode | - | - | 2 | msec |
| Tjit | Cycle peak to peak jitter | LOCK STATE | - | - | 500 | psec |

## 8. Timing Diagram

### (1) Power on and loop dynamic timing

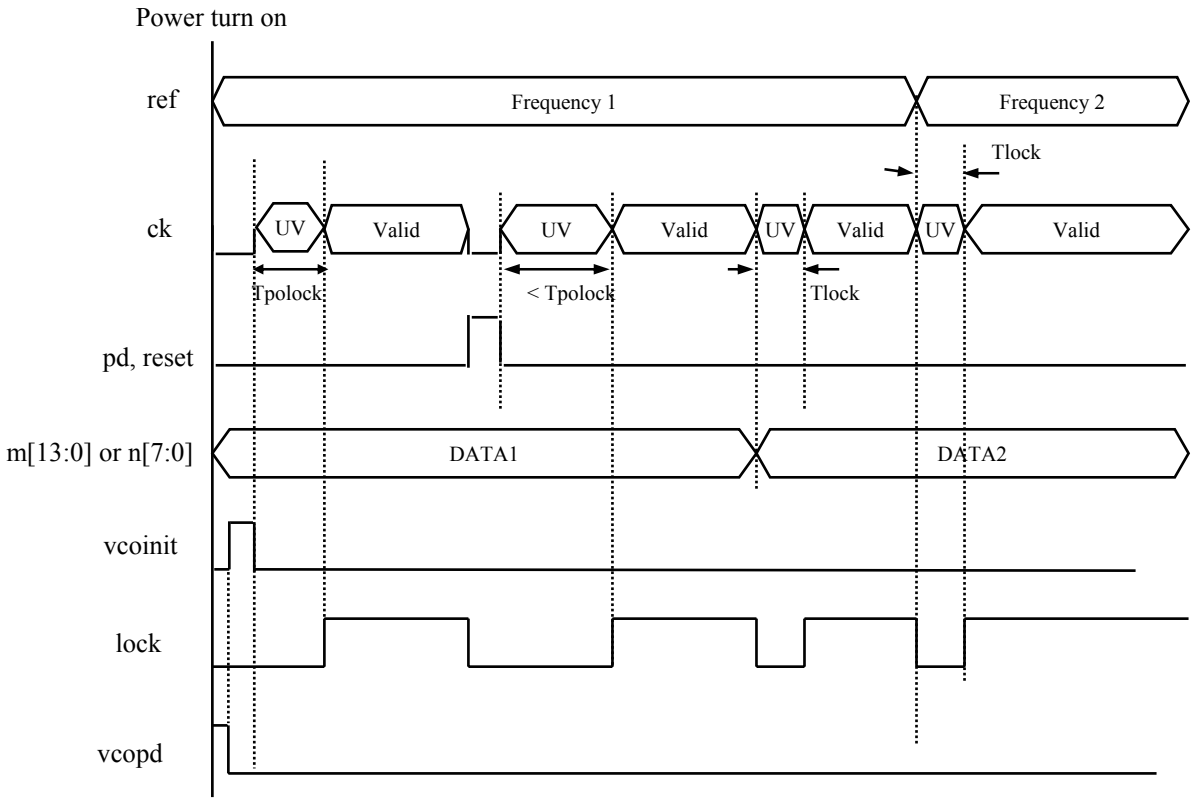



Figure 3. Timing diagram

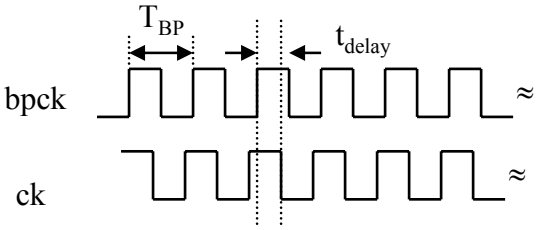
When **ck** is UV(Un-Valid) state, frequency of **ck** is undesirable. In this state H18GPL11S tracks valid frequency of **ck**. When **ck** is in the Valid state, frequency of **ck** is frequency of **ref** multiplied by (**m[13:0]** +2)/(**n[9:0]** +1).

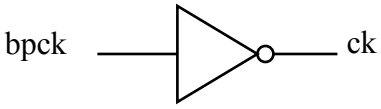
Tpolock is a power on lock time. While **pd** is high, loop filter charges are held. When **pd** is disabled, PLL tracks valid frequency fast. However, when **pd** remains high for a long time, loop filter charges are discharged slowly and at last charges are completely discharged. After long **pd**'s active state, the lock time of H18GPL11S, i.e. Tpolock is maximized. Tlock is a lock time when control data ( **m[13:0]** , **n[9:0]** ) or reference clock frequency are changed in lock range.

To ensure the proper operation of the H18GPL11S, the activation of **vcoinit** signal is required just after the deactivation of the **vcopd** signal. During power-up sequence **vcoinit** is recommended to be activated for more than 100ns.

### (2) Bypass mode

tdm = “high”, bypass = “high”




$t_{delay}$ : 3ns : **bpck** to **ck** delay time

## 9. Layout Guide

### (1) Power Pads guide

1) PLL requires dedicated analog (AVDD, AVSS, ASUB) and digital (DVDD, DVSS) power and ground pads to ensure proper operation.
2) ASUB ground must be connected from the analog ground pad and merged in front of the pad as can be seen in the Figure 4.
3) AVDD and DVDD are supplied with 1.8V and 1.8V power respectively. To isolate the analog and the digital power and the ground from digital pad ring, use the power cutting cells i.e. diode cells (PDO). Refer to the I/O library (HGI1113TP1_TYP or HGI1113TP3_TYP page 9) for more information. See Figure 5 for an example.
4) If you can place more pads for PLL, use as many power pads as you can and use those pads with double (multiple)-bond configuration. It is required to reduce power bouncing.
5) You may insert buffers between reference clock input pad and PLL input pin to make the rise/fall time of the clock input short.

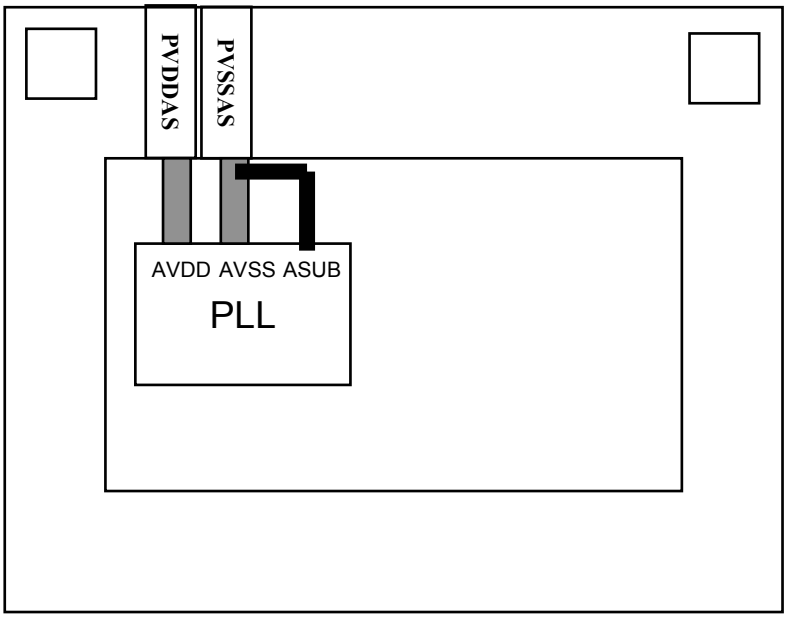



Figure 4. Routing consideration for the analog ground pads

## (2) Placement & Routing

1) Please place PLL at a corner of the chip and do not put noisy or high driving I/O pads near the PLL.
2) Please keep the routing from power pads to PLL power pins as short as possible.
3) The power metal width should be larger than the width of the PLL IP connection. See Figure 6 for an example.
4) Do not rout over the PLL IP and place 30um space from the IP to the other circuitry.
5) Minimize the crossing of digital core power or signal over the power lines of the PLL IP.
6) Figure 5 is a placement and routing example of PLL. In the figure analog and digital power are separated with diode cut cells.

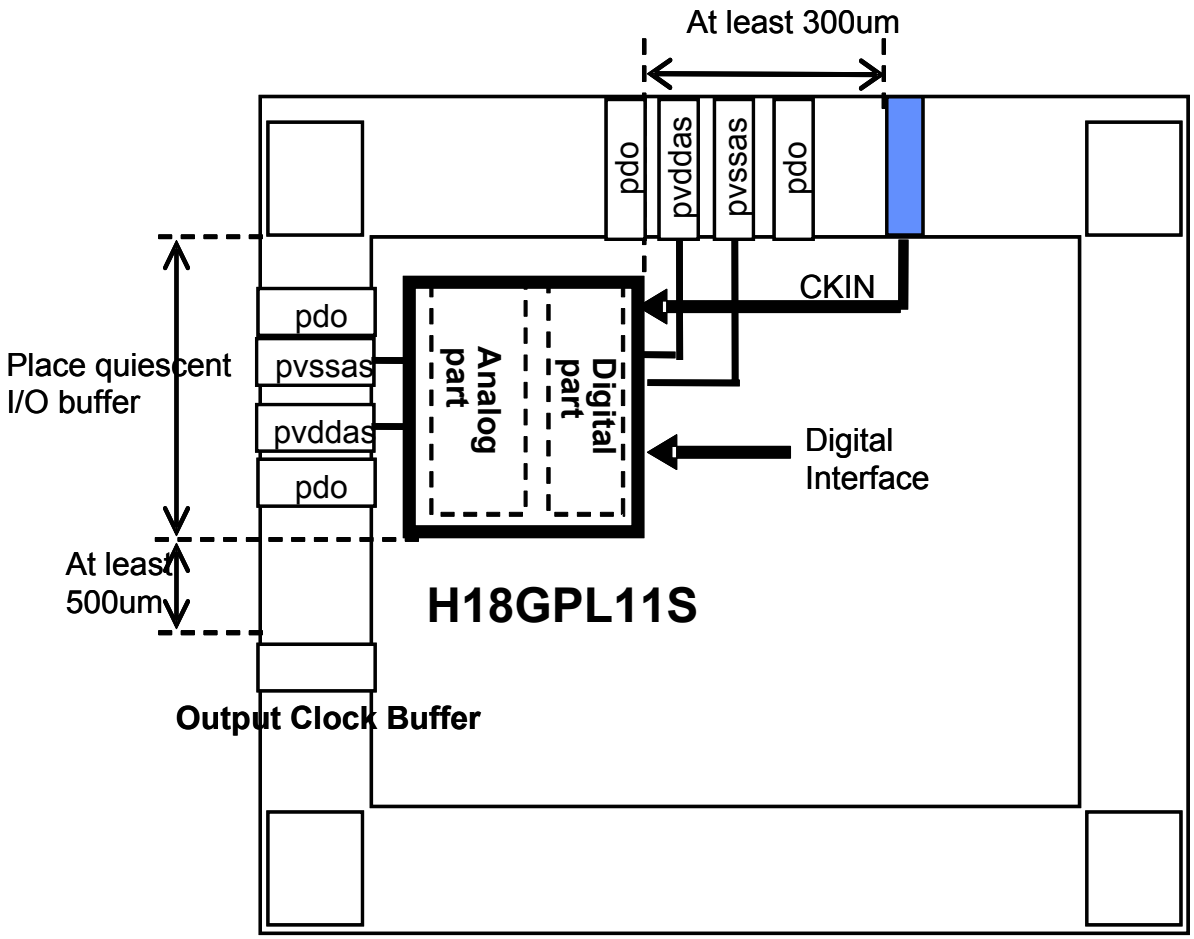



Figure 5. Placement and Routing consideration of PLL

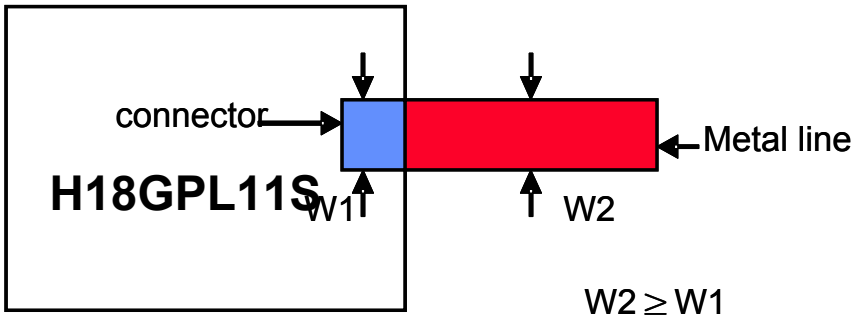



Figure 6. Connector width