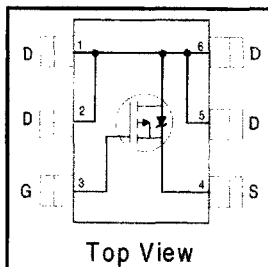


IRLMS6702

HEXFET® Power MOSFET

- Generation V Technology
- Micro6 Package Style
- Ultra Low $R_{DS(on)}$
- P-Channel MOSFET



$$V_{DSS} = -20V$$

$$R_{DS(on)} = 0.20\Omega$$

Description

Fifth Generation HEXFET® Power MOSFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design for which HEXFET Power MOSFETs are well known, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The Micro6 package with its customized leadframe produces a HEXFET power MOSFET with $R_{DS(on)}$ 60% less than a similar size SOT-23. This package is ideal for applications where printed circuit board space is at a premium. It's unique thermal design and $R_{DS(on)}$ reduction enables a current-handling increase of nearly 300% compared to the SOT-23.



Micro6

Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_A = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ -4.5V$	-2.3	A
$I_D @ T_A = 70^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ -4.5V$	-1.9	
I_{DM}	Pulsed Drain Current ①	-13	
$P_D @ T_A = 25^\circ\text{C}$	Power Dissipation	1.7	W
	Linear Derating Factor	13	mW/°C
V_{GS}	Gate-to-Source Voltage	± 12	V
dv/dt	Peak Diode Recovery dv/dt ②	5.0	V/ns
T_J, T_{STG}	Junction and Storage Temperature Range	-55 to + 150	°C

Thermal Resistance Ratings

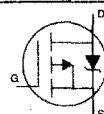
	Parameter	Min.	Typ.	Max	Units
$R_{\theta JA}$	Maximum Junction-to-Ambient ④	—	—	75	°C/W

Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	-20	—	—	V	$V_{GS} = 0V$, $I_D = -250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	-0.005	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = -1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.200	Ω	$V_{GS} = -4.5V$, $I_D = -1.6A$ ③
		—	—	0.375		$V_{GS} = -2.7V$, $I_D = -0.80A$ ③
$V_{GS(th)}$	Gate Threshold Voltage	-0.70	—	—	V	$V_{DS} = V_{GS}$, $I_D = -250\mu A$
g_{fs}	Forward Transconductance	1.5	—	—	S	$V_{DS} = -10V$, $I_D = -0.80A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	-1.0	μA	$V_{DS} = -16V$, $V_{GS} = 0V$
		—	—	-25		$V_{DS} = -16V$, $V_{GS} = 0V$, $T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	-100	nA	$V_{GS} = -12V$
	Gate-to-Source Reverse Leakage	—	—	100		$V_{GS} = 12V$
Q_g	Total Gate Charge	—	5.8	8.8	nC	$I_D = -1.6A$
Q_{gs}	Gate-to-Source Charge	—	1.8	2.6		$V_{DS} = -16V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	2.1	3.1		$V_{GS} = -4.5V$, see figure 6 and 9 ③
$t_{d(on)}$	Turn-On Delay Time	—	13	—	ns	$V_{DD} = -10V$
t_r	Rise Time	—	20	—		$I_D = -1.6A$
$t_{d(off)}$	Turn-Off Delay Time	—	21	—		$R_G = 6.0\Omega$
t_f	Fall Time	—	18	—		$R_D = 6.1\Omega$, see figure 10 ③
C_{iss}	Input Capacitance	—	210	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	130	—		$V_{DS} = -15V$
C_{rss}	Reverse Transfer Capacitance	—	73	—		$f = 1.0\text{MHz}$, see figure 5

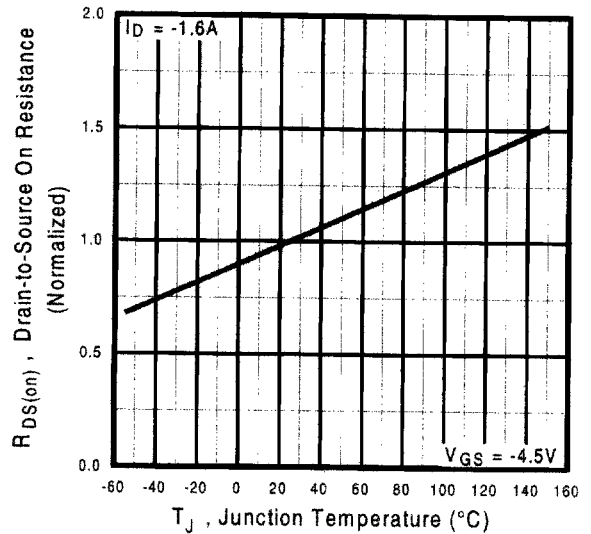
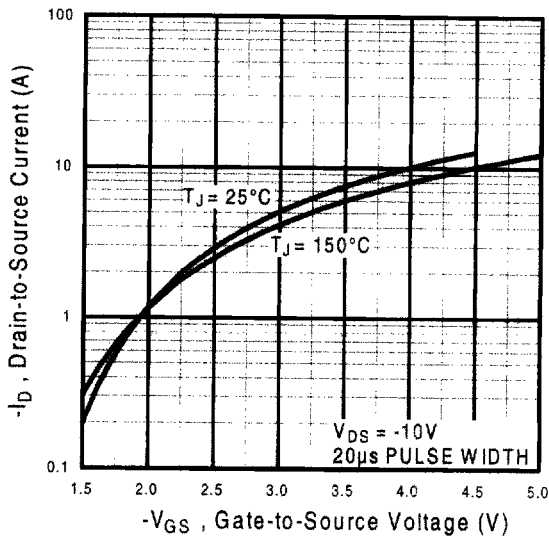
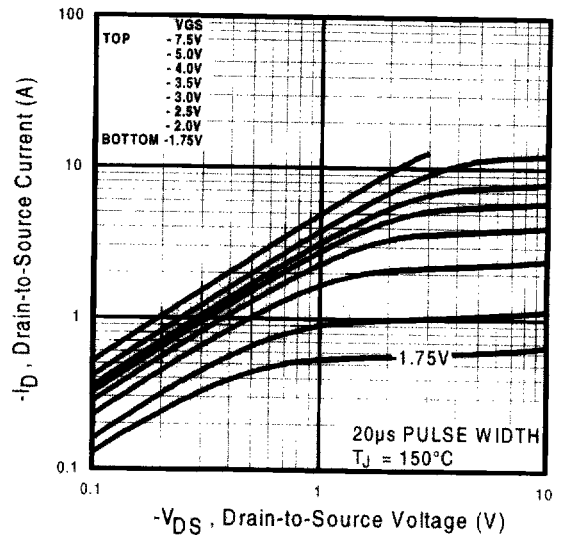
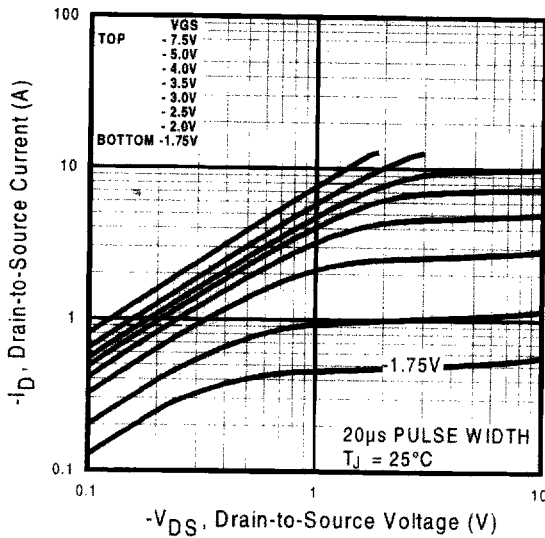
Source-Drain Ratings and Characteristics

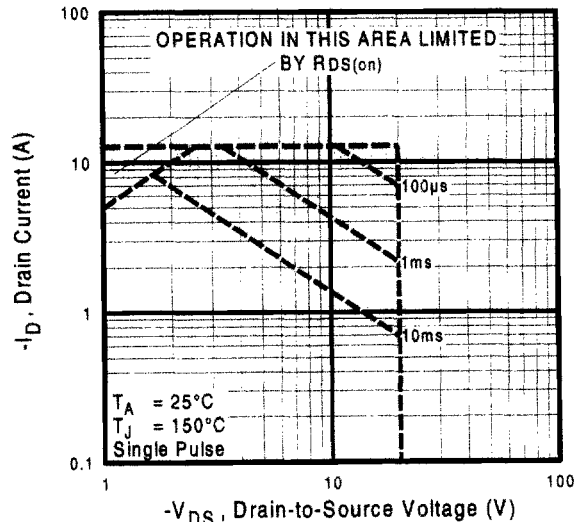
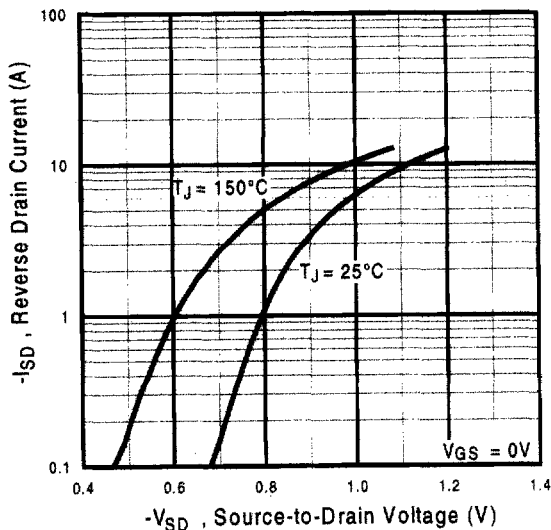
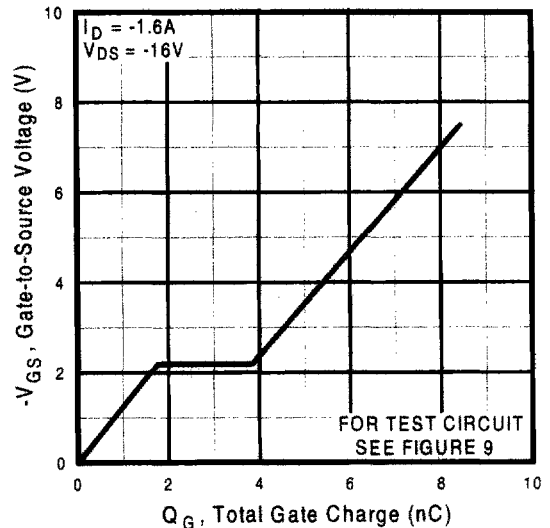
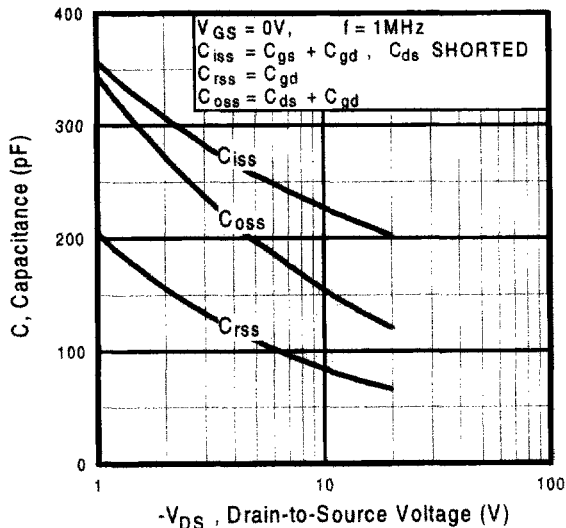
	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	-1.7	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	-13		
V_{SD}	Diode Forward Voltage	—	—	-1.2	V	$T_J = 25^\circ\text{C}$, $I_S = -1.6A$, $V_{GS} = 0V$ ③
t_{rr}	Reverse Recovery Time	—	25	37	ns	$T_J = 25^\circ\text{C}$, $I_F = -1.6A$
Q_{rr}	Reverse Recovery Charge	—	15	22	nC	$di/dt = -100A/\mu s$ ③



Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (see figure 11)
- ② $I_{SD} \leq -1.6A$, $di/dt \leq -100A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 150^\circ\text{C}$
- ③ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.
- ④ Surface mounted on FR-4 board, $t \leq 5\text{sec}$.





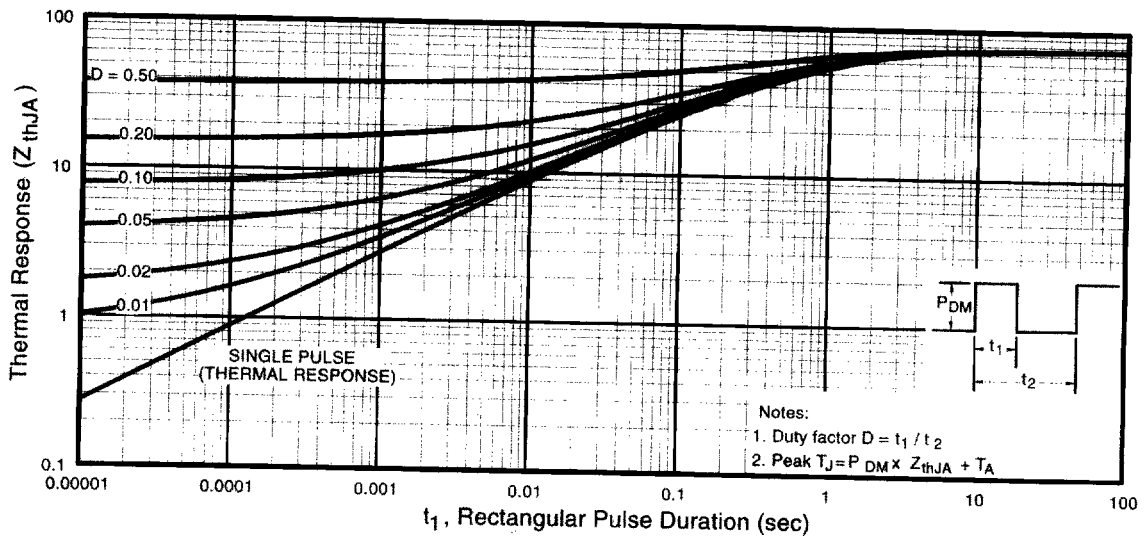


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient