GD54/74HC670, GD54/74HCT670

4-BY-4 REGISTER FILE WITH 3-STATE OUTPUTS

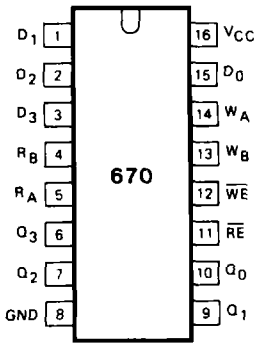
General Description

These devices are identical in pinout to the 54/74LS670. This register file is organized as 4 words of 4 bits each and separate on-chip decoding is provided for addressing the four word locations to either write-in or retrieve data. This permits simultaneous writing into one location and reading from another word location. The individual address lines permit direct acquisition of data stored in any four of the latches. This circuit can be used as:

Scratch-pad Memory
Buffer storage between processors
Bit storage in fast multiplication designs

These devices are characterized for operation over wide temperature ranges to meet industry and military specifications.

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package
Suffix-D : Small Outline Package

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 15 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
  for HCT 4.5 to 5.5 volts
- Low input current: 1μA Max.
- Low quiescent current: 80μA Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Function Table

WRITE MODE SELECT TABLE

OPERATING MODE	INPUTS		INTERNAL LATCHES★
	$\overline{WE}$	D_n	
write data	L	L	L
	L	H	H
data latched	H	X	no change

★ The write address (W_A and W_B) to the internal latches must be stable while $\overline{WE}$ is LOW for conventional operation

READ MODE SELECT TABLE

OPERATING MODE	INPUTS		OUTPUT
	$\overline{RE}$	INTERNAL LATCHES★★	Q_n
read	L	L	L
	L	H	H
disabled	H	X	Z

★★ The selection of the internal latches by read address (R_A and R_B) are not constrained by $\overline{WE}$ or $\overline{RE}$ operation

Logic Diagram

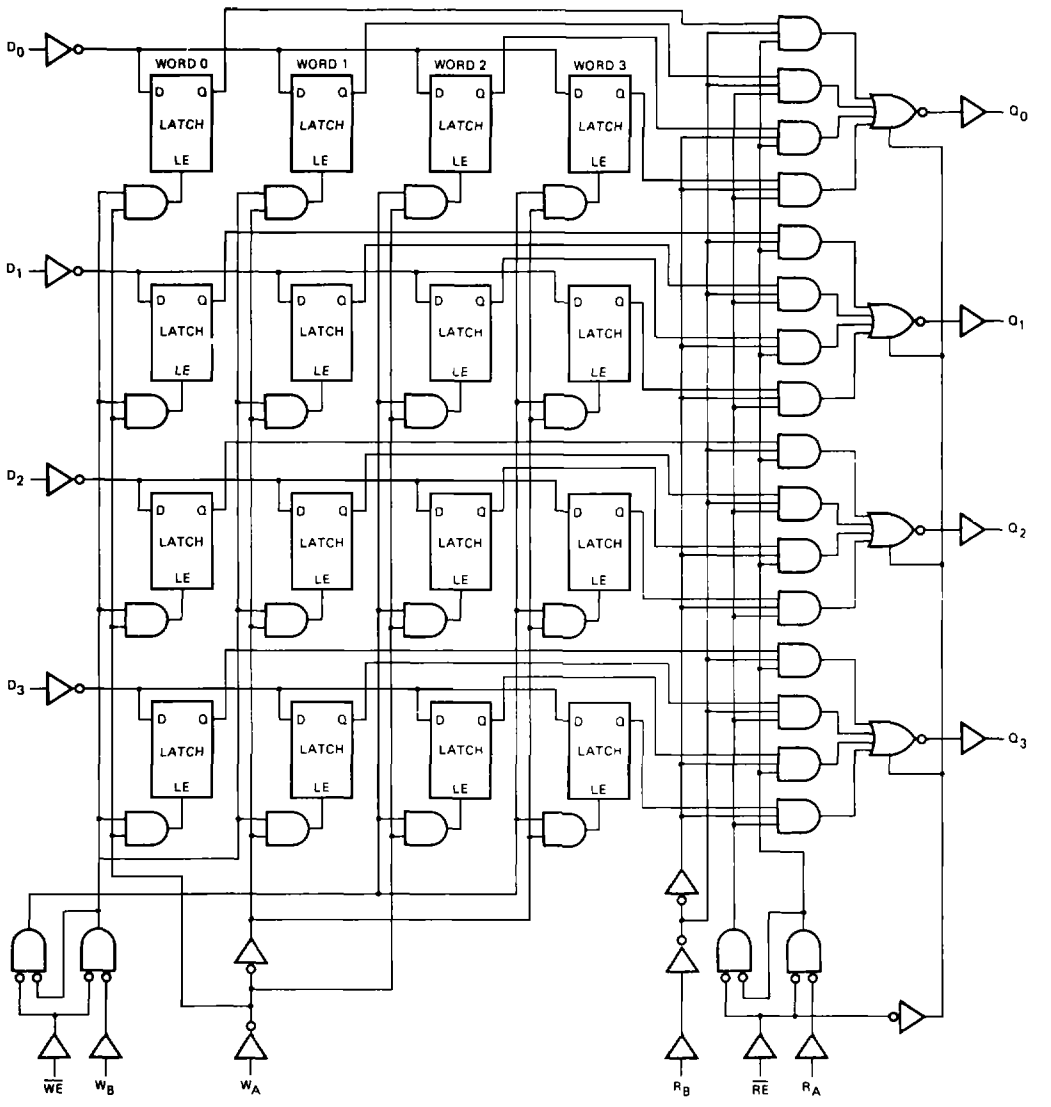


Fig. 1 Logic diagram

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{CC}	DC Supply voltage		−0 5	+7	V
I_{IK} I_{OK}	DC input or output diode current	for $V_I<-0$ 5 or $V_I>V_{CC}+0$ 5V		|20|	mA
I_O	DC output source or sink current	for -0 5V$<V_O<V_{CC}+0$ 5V		|25|	mA
I_{CC}	DC V_{CC} or GND current			|50|	mA
T_{stg}	Storage temperature range		−65	150	°C
P_D	Power dissipation per package	above +70°C derate linearly with 8mW K		500	mW
T_L	Lead temperature	At distance 1 16±1 32 in from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		 300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN	MAX	
Supply-Voltage Range V_{CC}. GD54,74HC Types	2	6	V
GD54·74HCT Types	4 5	5 5	
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A GD74 Types	−40	+85	°C
GD54 Types	−55	+125	
Input Rise and Fall times t_r, t_f GD54 74HC Types at 2V		1000	ns
at 4 5V		500	
at 6V		400	
GD54 74HCT Types at 4 5 V		500	

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION		V_{CC} (V)	T_A=25°C MIN	T_A=25°C TYP	T_A=25°C MAX.	GD74HC670 MIN	GD74HC670 MAX.	GD54HC670 MIN	GD54HC670 MAX.	UNIT
V_{IH}	HIGH level input Voltage			2 0 4 5 6 0	1 5 3.15 4.2			1.5 3.15 4.2		1.5 3 15 4 2		V
V_{IL}	LOW level input voltage			2 0 4 5 6 0			0 3 0 9 1 2		0 3 0.9 1.2		0 3 0 9 1 2	V
V_{OH}	HIGH level output voltage	V_{IN}=V_{IH} or V_{IL}	I_{OH}=−20μA	2.0 4.5 6.0	1 9 4 4 5 9	2 0 4 5 6 0		1 9 4.4 5 9		1 9 4 4 5 9		V
			I_{OH}=−4mA I_{OH}=−5.2mA	4 5 6 0	3 98 5 48	4 3 5 2		3 84 5.34		3.7 5.2		
V_{OL}	LOW level output voltage	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2 0 4 5 6 0			0 1 0 1 0 1		0 1 0 1 0 1		0 1 0 1 0 1	V
			I_{OL}=4mA I_{OL}=5.2mA	4 5 6.0		0 17 0 15	0.26 0.26		0 33 0 33		0 4 0 4	
$\|I_{IN}\|$	Input leakage Current	V_{IN}=V_{CC} or GND		6.0			0.1		1 0		1.0	μA
I_{CC}	Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{out}=0μA		6.0			8		80		160	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION		V_{CC} (V)	T_A=25°C MIN	T_A=25°C TYP	T_A=25°C MAX.	GD74HCT670 MIN	GD74HCT670 MAX	GD54HCT670 MIN	GD54HCT670 MAX	UNIT
V_{IH}	HIGH level input Voltage			4.5 to 5.5	2 0			2.0		2.0		V
V_{IL}	LOW level input voltage			4.5 to 5.5			0.8		0 8		0.8	V
V_{OH}	HIGH level output voltage	V_{IN}=V_{IH}	I_{OH}=−20μA	4 5	4 4	4 5		4 4		4 4		V
		or V_{IL}	I_{OH}=−4mA	4.5	3.98	4 3		3.84		3.7		
V_{OL}	LOW level output voltage	V_{IN}=V_{IH}	I_{OL}=20μA	4.5			0.1		0 1		0 1	V
		or V_{IL}	I_{OL}=4mA	4 5		0 17	0.26		0 33		0 4	
$\|I_{IN}\|$	Input leakage Current	V_{IN}=V_{CC}or GND		5 5			0.1		1 0		1 0	μA
I_{CC}	Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{out}=0μA		5 5			8		80		160	μA

Timing Requirements for HC: $t_r=t_f=6ns$ $C_L=50$ pF

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25°C$			GD74HC670		GD54HC670		UNIT
				MIN	TYP	MAX	MIN.	MAX	MIN	MAX	
t_w	Pulse width	RE low	2 0	70			115		135		ns
			4 5	18			23		27		
			6.0	15			20		23		
		$\overline{WE}$ low	2 0	90			115		135		ns
			4 5	18			23		27		
			6 0	15			20		23		
t_{su}	Setup time	Dn before $\overline{WE}$ ↑	2.0	60			75		90		ns
			4 5	12			15		18		
			6 0	10			13		15		
		W_A, W_B before $\overline{WE}$ ↓	2 0	60			75		90		ns
			4.5	12			15		18		
			6 0	10			13		15		
t_h	Hold time	Dn after $\overline{WE}$ ↑	2 0	5			5		5		ns
			4 5	5			5		5		
			6.0	5			5		5		
		W_A, W_B after $\overline{WE}$ ↑	2 0	5			5		5		ns
			4 5	5			5		5		
			6 0	5			5		5		
t_{latch}	Latch time	$\overline{WE}$ to R_A, R_B ↑	2 0	225			230		340		ns
			4.5	45			56		68		
			6 0	38			48		58		

AC Characteristics for HC: $t_r=t_f=6ns$ $C_L=50$ pF

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25°C$			GD74HC670		GD54HC670		UNIT
			MIN.	TYP.	MAX.	MIN	MAX	MIN	MAX.	
t_{PLH}, t_{PHL}	Propagation Delay Time R_A R_B to Qn	2 0			225		280		340	ns
		4 5			45		56		68	
		6 0			38		48		58	
t_{PLH}, t_{PHL}	Propagation Delay Time $\overline{WE}$ to Qn	2 0			250		315		375	ns
		4.5			50		63		75	
		6 0			43		54		64	
t_{PLH}, t_{PHL}	Propagation Delay Time Dn to Qn	2 0			250		315		375	ns
		4 5			50		63		75	
		6.0			43		54		64	
t_{PZH}, t_{PZL}	3-state Output Enable Time $\overline{RE}$ to Qn	2.0			175		220		265	ns
		4.5			35		44		53	
		6 0			30		37		45	
t_{PLZ}, t_{PHZ}	3-state Output Disable Time $\overline{RE}$ to Qn	2.0			175		220		265	ns
		4.5			35		44		53	
		6 0			30		37		45	
t_{TLH}, t_{THL}	Output Transition Time	2 0		19	75		95		110	ns
		4.5		7	15		19		22	
		6 0		6	13		16		19	

Timing Requirements for HCT: $t_r=t_f=6ns$ $C_L=50$ pF

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25°C$			GD74HCT670		GD54HCT670		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse width	$\overline{RE}$ low	4.5	25			31		38		ns
		$\overline{WE}$ low	4.5	25			31		38		ns
t_{su}	Setup time	Dn before $\overline{WE}$ ↑	4.5	12			15		18		ns
		W_A, W_B before $\overline{WE}$ ↓	4.5	18			23		27		ns
t_h	Hold time	Dn after $\overline{WE}$ ↑	4 5	5			5		5		ns
		W_A, W_B after $\overline{WE}$ ↑	4 5	5			5		5		ns
t_{latch}	Latch time	$\overline{WE}$ to R_A, R_B ↑	4 5	50			63		75		Mhz

AC Characteristics for HCT: $t_r=t_f=6ns$ $C_L=50$ pF

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25°C$			GD74HCT670		GD54HCT670		UNIT
			MIN	TYP	MAX	MIN.	MAX.	MIN.	MAX.	
t_{PLH}, t_{PHL}	Propagation Delay Time R_A, R_B to Qn	4 5			50		63		75	ns
t_{PLH}, t_{PHL}	Propagation Delay Time $\overline{WE}$ to Qn	4.5			53		66		80	ns
t_{PLH}, t_{PHL}	Propagation Delay Time Dn to Qn	4 5			50		63		75	ns
t_{PZH}, t_{PZL}	3-state Output Enable Time $\overline{RE}$ to Qn	4.5			40		50		60	ns
t_{PLZ}, t_{PHZ}	3-state Output Disable Time $\overline{RE}$ to Qn	4.5			35		44		53	ns
t_{TLH}, t_{THL}	Output Transition Time	4.5		7	15		19		22	ns

AC Waveforms

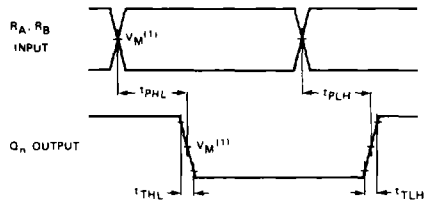


Fig. 2 Waveforms showing the read address input (R_A, R_B) to output (Q_n) propagation delays and output transition times.

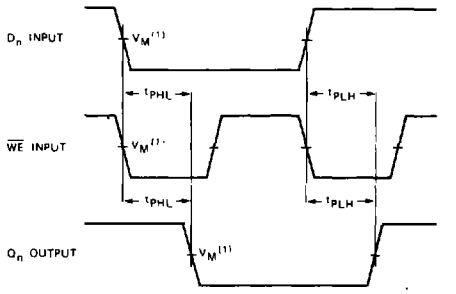
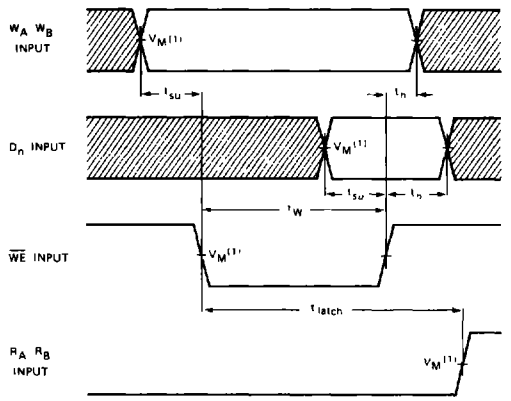


Fig. 3 Waveforms showing the write enable input ($\overline{WE}$) and data input (D_n) to output (Q_n) propagation delays, and the write enable pulse width



Note to Fig. 4

The shaded areas indicate when the input is permitted to change for predictable output performance

The time allowed for the internal output of the latch to assume the state of the new data (t_{latch}) is important only when attempting to read from a location immediately after that location has received new data. This parameter is measured from the falling edge of $\overline{WE}$ to the rising edge of R_A or R_B. $\overline{RE}$ must be LOW

Fig. 4 Waveforms showing the write address input (W_A, W_B)and data input (D_n) to write enable ($\overline{WE}$) set-up, hold and latch times.

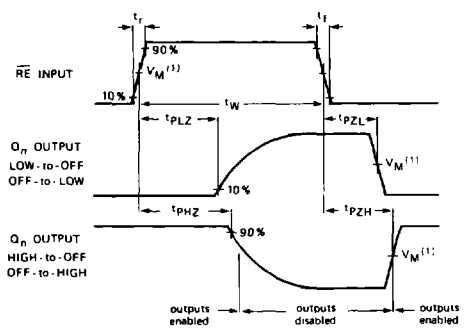


Fig. 5 Waveforms showing the read enable ($\overline{RE}$) to output (Q_n) enable and disable times, and read enable pulse width

Note to AC waveforms

(1) HC : V_M=50% V_I=GND to V_{CC}
HCT : V_M=1.3V, V_I=GND to 3V