Innovasic®
Semiconductor
Extended Life Semiconductor Solutions

IA186XL/IA188XL
16-Bit Microcontroller
Data Sheet

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TABLE OF CONTENTS

List of Figures 5
List of Tables 6
1. Introduction 7
    1.1 General Description 7
    1.2 Features 7
2. Packaging, Pin Descriptions, and Physical Dimensions 9
    2.1 Packages and Pinouts 9
        2.1.1 IA186XL 68 PLCC Package 10
        2.1.2 IA188XL 68 PLCC Package 12
        2.1.3 PLCC Physical Dimensions 14
        2.1.4 IA186XL 80 PQFP Package 15
        2.1.5 IA188XL 80 PQFP Package 17
        2.1.6 PQFP Physical Dimensions 19
        2.1.7 IA186XL 80 LQFP Package 20
        2.1.8 IA188XL 80 LQFP Package 22
        2.1.9 LQFP Physical Dimensions 24
    2.2 IA186XL Pin/Signal Descriptions 25
    2.3 IA188XL Pin/Signal Descriptions 31
3. Maximum Ratings, Thermal Characteristics, and DC Parameters 37
4. Functional Description 39
    4.1 Device Architecture 39
        4.1.1 Bus Interface Unit 39
        4.1.2 Clock Generator 42
        4.1.3 Interrupt Control Unit 42
        4.1.4 Timer/Counter Unit 42
        4.1.5 Chip-Select/Ready Generation Logic 43
        4.1.6 DMA 44
        4.1.7 DRAM Refresh Control Unit 44
        4.1.8 Power-Save Control 44
    4.2 Operating Modes 45
        4.2.1 Enhanced Mode 45
        4.2.2 Queue Status Mode 45
        4.2.3 ONCE Mode 45
        4.2.4 Math Coprocessor (IA186XL Only) 45
    Table 12. Internal Register Map 46
5. AC Specifications 47
    5.1 Major Cycle Timings – Read Cycle 47
    5.2 Major Cycle Timings – Write Cycle 49
    5.3 Major Cycle Timings – Interrupt Acknowledge Cycle 51
    5.4 Software Halt Cycle Timings 53
    5.5 Clock Timings 55
    5.6 Ready, Peripheral and Queue Status Timings 56

5.7 Reset and HOLD/HLDA Timings....57
6. Instruction Execution Times....61
7. Innovasic Part Number Cross-Reference....66
8. Errata....69
8.1 Summary....69
8.2 Detail....70
9. Data Sheet Revision History....74
10. For Additional Information....75

LIST OF FIGURES

Figure 1. IA186XL 68-Lead PLCC Package Diagram 10
Figure 2. IA188XL 68-Lead PLCC Package Diagram 12
Figure 3. PLCC Physical Package Dimensions 14
Figure 4. IA186XL 80-Lead PQFP Package Diagram 15
Figure 5. IA188XL 80-Lead PQFP Package Diagram 17
Figure 6. PQFP Physical Package Dimensions 19
Figure 7. IA186XL 80-Lead LQFP Package Diagram 20
Figure 8. IA188XL 80-Lead LQFP Package Diagram 22
Figure 9. LQFP Physical Package Dimensions 24
Figure 10. IA186XL/IA188XL Functional Block Diagram 41
Figure 11. Clock Circuit Connection Options 43
Figure 12. Read Cycle Waveforms 48
Figure 13. Write Cycle Waveforms 50
Figure 14. Interrupt Acknowledge Cycle Waveforms 52
Figure 15. Software Halt Cycle Waveforms 54
Figure 16. Clock Waveforms 58
Figure 17. Reset Waveforms 58
Figure 18. Synchronous Ready (SRDY) Waveforms 58
Figure 19. Asynchronous Ready (ARDY) Waveforms 59
Figure 20. Peripheral and Queue Status Waveforms 59
Figure 21. HOLDA/HLDA Waveforms (Entering Hold) 60
Figure 22. HOLD/HLDA Waveforms (Leaving Hold) 60

LIST OF TABLES

Table 1. IA186XL 68-Lead PLCC Pin Listing 11
Table 2. IA188XL 68-Lead PLCC Pin Listing 13
Table 3. IA186XL 80-Lead PQFP Pin Listing 16
Table 4. IA188XL 80-Lead PQFP Pin Listing 18
Table 5. IA186XL 80-Lead LQFP Pin Listing 21
Table 6. IA188XL 80-Lead LQFP Pin Listing 23
Table 7. IA186XL Pin/Signal Descriptions 25
Table 8. IA188XL Pin/Signal Descriptions 31
Table 9. IA186XL and IA188XL Absolute Maximum Ratings 37
Table 10. IA186XL and IA188XL Thermal Characteristics 37
Table 11. IA186XL and IA188XL DC Parameters 38
Table 13. Major Cycle Timings – Read Cycle 47
Table 14. Major Cycle Timings – Write Cycle 49
Table 15. Major Cycle Timings – Interrupt Acknowledge Cycle 51
Table 16. Software Halt Cycle Timings 53
Table 17. Clock Timings 55
Table 18. Ready, Peripheral and Queue Status Timings 56
Table 19. Reset and HOLD/HLDA Timings 57
Table 20. Instruction Set Timing 61
Table 21. Innovasic Part Number Cross-Reference for the PLCC 66
Table 22. Innovasic Part Number Cross-Reference for the PQFP (Special Order only) 67
Table 23. Innovasic Part Number Cross-Reference for the LQFP (Special Order only) 68
Table 24. Summary of Errata 69
Table 25. Data Sheet Revision History 74

1. Introduction

The Innovasic Semiconductor IA186XL and IA188XL microcontrollers are form, fit, and function replacements for the original Intel 80C186XL and 80C188XL 16-bit high-integration embedded processors.

These devices are produced using Innovasic's Managed IC Lifetime Extension System (MILES™). This cloning technology, which produces replacement ICs beyond simple emulations, ensures compatibility with the original device, including any "undocumented features." Additionally, the MILES™ process captures the clone design in such a way that production of the clone can continue even as silicon technology advances.

The IA186XL and IA188XL microcontrollers replace the obsolete Intel 80C186XL and 80C188XL devices, allowing users to retain existing board designs, software compilers/assemblers, and emulation tools, thereby avoiding expensive redesign efforts.

1.1 General Description

The Innovasic Semiconductor IA186XL and IA188XL microcontrollers have a set of base peripherals beneficial to many embedded applications and include a standard numeric interface, an interrupt control unit, a chip-select unit/Ready Generation Logic, a DRAM refresh control unit, a Power-Save Control unit, DMA and three 16-bit timer/counters.

The IA186XL and IA188XL microcontrollers operate at 5.0 volts ± 10%.

The following functional description describes the base architecture of the 80C186XL. The 80C186XL is a very high integration 16-bit microprocessor. It combines some of the most common microprocessor system components onto one chip. The 80C186XL is object-code compatible with the 8086/8088 microprocessors and adds ten new instruction types to the 8086/8088 instruction set.

The 80C186XL has two major modes of operation, Compatible and Enhanced. In Compatible Mode, the 80C186XL is completely compatible with the 80186, with the exception of 8087 support. The Enhanced mode adds three new features to the system design. These are Power-Save control, Dynamic RAM refresh, and an asynchronous Numerics Coprocessor interface (80C186XL only).

1.2 Features

The primary features of the IA186XL and IA188XL microcontrollers are as follows:

- Form, fit, and function compatible version of the low power Intel 80C186XL/80C188XL
- Operation modes:
  - Enhanced mode
    - DRAM refresh control unit

    - Power-save mode
    - Direct interface to 80C187 (IA186XL only)
  - Compatible mode
    - Pin-for-pin replacement for NMOS 80186/80188 non-numeric applications
- Integrated feature set
  - Static, modular CPU
  - Clock generator
  - Two independent DMA channels
  - Programmable interrupt controller
  - Three programmable 16-bit timers
  - Dynamic RAM refresh control unit
  - Programmable memory and peripheral chip select logic
  - Programmable wait state generator
  - Local bus controller
  - Power-save mode
  - System-level testing support (high impedance test mode)
- Completely object-code compatible with existing 8086/8088 software and has ten additional instructions over 8086/8088
- Crystal supports internal 20–25 MHz operation
- Direct addressing capability to 1 MByte memory and 64 Kbyte I/O
- Available in 68-Lead:
  - Plastic Leaded Chip Carrier (PLCC)
- Available in 80-Lead:
  - Plastic Quad Flat Pack (PQFP)
  - Low Profile Quad Flat Pack (LQFP)
- Extended Temperature Range (-40°C to +85°C)

Chapter 4, Functional Description, provides details of the IA186XL and IA188XL microcontrollers, including the features listed above.

2. Packaging, Pin Descriptions, and Physical Dimensions

Information on the packages and pin descriptions for the IA186XL and the IA188XL is provided separately. Refer to sections, figures, and tables for information on the device of interest.

2.1 Packages and Pinouts

The Innovasic Semiconductor IA186XL and IA188XL microcontroller is available in the following packages:

- 68-Lead Plastic Leaded Chip Carrier (PLCC), equivalent to original PLCC package
- 80-Lead Plastic Quad Flat Pack (PQFP), equivalent to original PQFP package
- 80-Lead Low Profile Quad Flat Pack (LQFP), equivalent to original SQFP package

2.1.1 IA186XL 68 PLCC Package

The pinout for the IA186XL 68 PLCC package is as shown in Figure 1. The corresponding pinout is provided in Table 1.

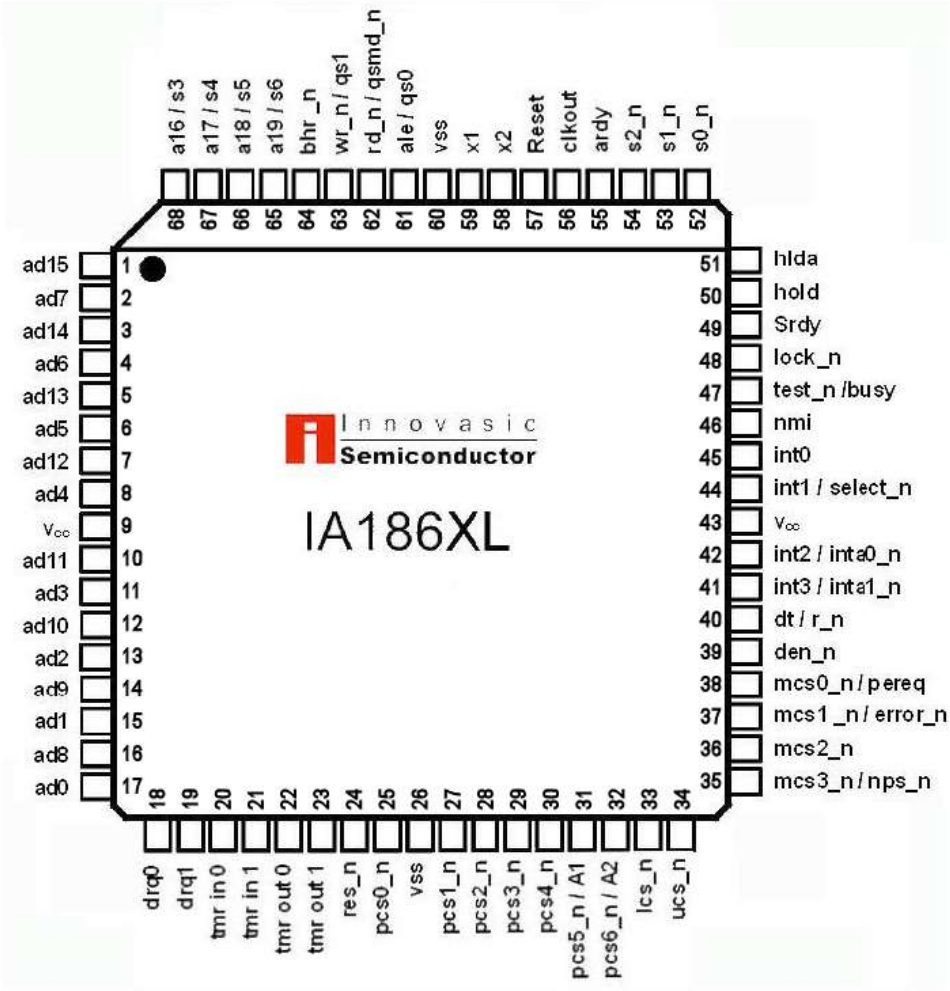


Figure 1. IA186XL 68-Lead PLCC Package Diagram

Table 1. IA186XL 68-Lead PLCC Pin Listing

Pin	Name
1	ad15
2	ad7
3	ad14
4	ad6
5	ad13
6	ad5
7	ad12
8	ad4
9	v_{cc}
10	ad11
11	ad3
12	ad10
13	ad2
14	ad9
15	ad1
16	ad8
17	ad0

Pin	Name
18	drq0
19	drq1
20	tmr in 0
21	tmr in 1
22	tmr out 0
23	tmr out 1
24	res_n
25	pcs0_n
26	v_{ss}
27	pcs1_n
28	pcs2_n
29	pcs3_n
30	pcs4_n
31	pcs5_n/a1
32	pcs6_n/a2
33	lcs_n
34	ucs_n

Pin	Name
35	mcs3_n/nps_n
36	mcs2_n
37	mcs1 _n/error_n
38	mcs0_n/pereq
39	den_n
40	dt/r_n
41	int3/inta1_n
42	int2/inta0_n
43	v_{cc}
44	int1/select_n
45	int0
46	nmi
47	test_n /busy
48	lock_n
49	srdy
50	hold
51	hlda

Pin	Name
52	s0_n
53	s1_n
54	s2_n
55	ardy
56	clkout
57	reset
58	x2
59	x1
60	v_{ss}
61	ale/qs0
62	rd_n/qsmd_n
63	wr_n/qs1
64	bhe_n
65	a19/s6
66	a18/s5
67	a17/s4
68	a16/s3

2.1.2 IA188XL 68 PLCC Package

The pinout for the IA188XL 68 PLCC package is as shown in Figure 2. The corresponding pinout is provided in Table 2.

NOTE: The Innovasic 68-Lead PLCC package has both an ink mark and an indentation to indicate proper orientation. Pin 1 is designated by the ink mark, as shown in Figure 2.

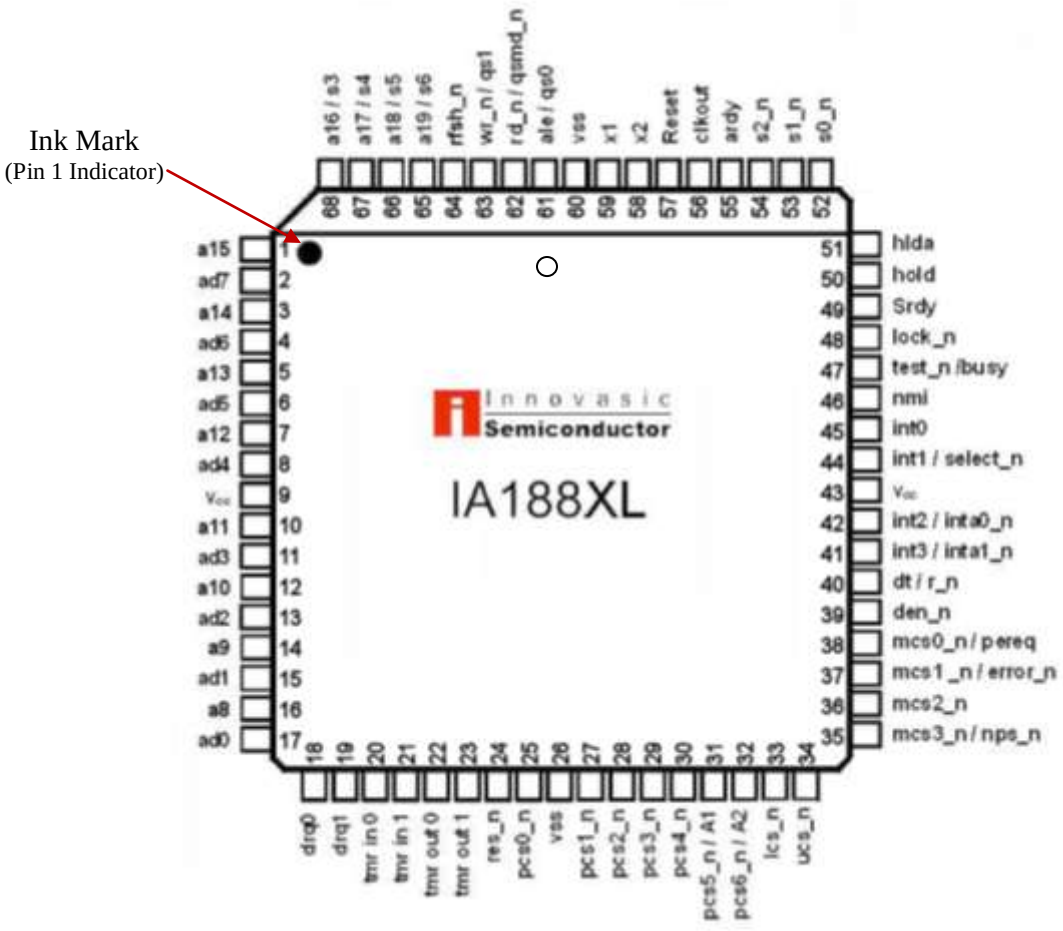


Figure 2. IA188XL 68-Lead PLCC Package Diagram

Table 2. IA188XL 68-Lead PLCC Pin Listing

Pin	Name
1	a15
2	ad7
3	a14
4	ad6
5	a13
6	ad5
7	a12
8	ad4
9	v_{cc}
10	a11
11	ad3
12	a10
13	ad2
14	a9
15	ad1
16	a8
17	ad0

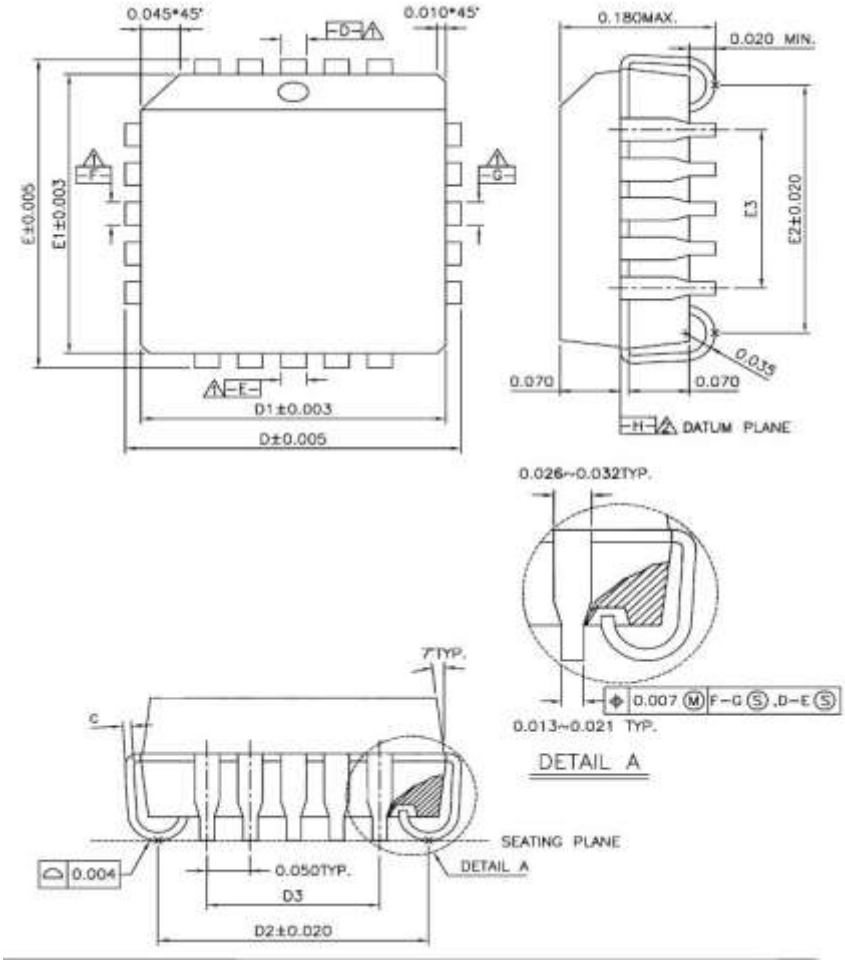
Pin	Name
18	drq0
19	drq1
20	tmr in 0
21	tmr in 1
22	tmr out 0
23	tmr out 1
24	res_n
25	pcs0_n
26	v_{ss}
27	pcs1_n
28	pcs2_n
29	pcs3_n
30	pcs4_n
31	pcs5_n/a1
32	pcs6 _n/a2
33	lcs_n
34	ucs_n

Pin	Name
35	mcs3_n/nps_n
36	mcs2_n
37	mcs1 _n/error_n
38	mcs0 _n/pereq
39	den_n
40	dt/r_n
41	int3/inta1_n
42	int2/inta0_n
43	v_{cc}
44	int1/select_n
45	int0
46	nmi
47	test_n /busy
48	lock_n
49	srdy
50	hold
51	hlda

Pin	Name
52	s0_n
53	s1_n
54	s2_n
55	ardy
56	clkout
57	reset
58	x2
59	x1
60	v_{ss}
61	ale/qs0
62	rd _n/qsmd_n
63	wr _n/qs1
64	rfsh_n
65	a19/s6
66	a18/s5
67	a17/s4
68	a16/s3

2.1.3 PLCC Physical Dimensions

The physical dimensions for the 68 PLCC are as shown in Figure 3.



Legend:

Symbol	Min	Nom[1]	Max
c	–	0.008	–
D	–	0.990	–
D1	–	0.953	–
D2	–	0.910	
D3	–	0.800	–
E	–	0.990	–
E1	–	0.953	–
E2	–	0.910	–
E3	–	0.800	–

1. Datums D–E and F–G to be determined where center leads exit plastic body at Datum Plane –H–.

2. Datum Plane –H– located at top of mold parting line and coincident with top of lead. Where lead exits plastic body.

Note: [1]Controlling dimension in inches.

Figure 3. PLCC Physical Package Dimensions

2.1.4 IA186XL 80 PQFP Package

The pinout for the IA186XL 80 PQFP package is as shown in Figure 4. The corresponding pinout is provided in Table 3.

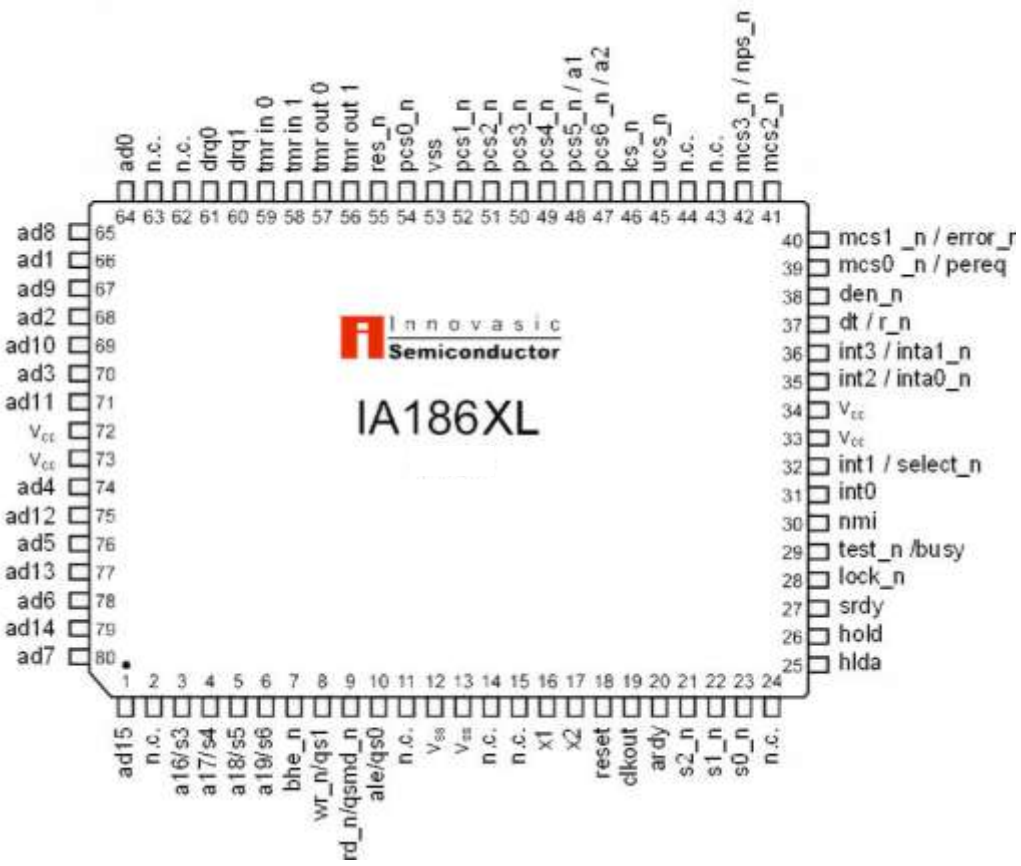


Figure 4. IA186XL 80-Lead PQFP Package Diagram

Table 3. IA186XL 80-Lead PQFP Pin Listing

Pin	Name
1	ad15
2	n.c.
3	a16/s3
4	a17/s4
5	a18/s5
6	a19/s6
7	bhe_n
8	wr_n/qs1
9	rd_n/qsmd_n
10	ale/qs0
11	n.c.
12	V_{SS}
13	V_{SS}
14	n.c.
15	n.c.
16	x1
17	x2
18	reset
19	clkout
20	ardy

Pin	Name
21	s2_n
22	s1_n
23	s0_n
24	n.c.
25	hlda
26	hold
27	srdy
28	lock_n
29	test_n /busy
30	nmi
31	int0
32	int1/select_n
33	V_{CC}
34	V_{CC}
35	int2/inta0_n
36	int3/inta1_n
37	dt/r_n
38	den_n
39	mcs0 _n/pereq
40	mcs1 _n/error_n

Pin	Name
41	mcs2_n
42	mcs3_n/nps_n
43	n.c.
44	n.c.
45	ucs_n
46	lcs_n
47	pcs6 _n/a2
48	pcs5_n/a1
49	pcs4_n
50	pcs3_n
51	pcs2_n
52	pcs1_n
53	V_{SS}
54	pcs0_n
55	res_n
56	tmr out 1
57	tmr out 0
58	tmr in 1
59	tmr in 0
60	drq1

Pin	Name
61	drq0
62	n.c.
63	n.c.
64	ad0
65	ad8
66	ad1
67	ad9
68	ad2
69	ad10
70	ad3
71	ad11
72	V_{CC}
73	V_{CC}
74	ad4
75	ad12
76	ad5
77	ad13
78	ad6
79	ad14
80	ad7

2.1.5 IA188XL 80 PQFP Package

The pinout for the IA186XL 80 PQFP package is as shown in Figure 5. The corresponding pinout is provided in Table 4.

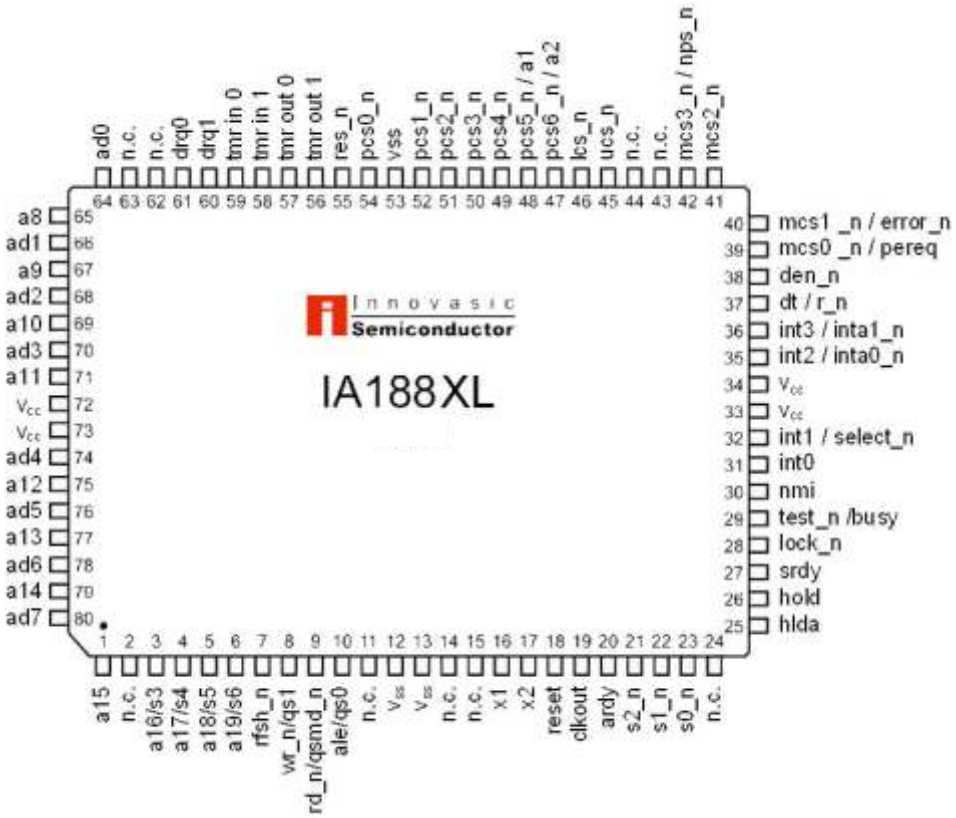


Figure 5. IA188XL 80-Lead PQFP Package Diagram

Table 4. IA188XL 80-Lead PQFP Pin Listing

Pin	Name
1	a15
2	n.c.
3	a16/s3
4	a17/s4
5	a18/s5
6	a19/s6
7	rfsh_n
8	wr_n/qs1
9	rd_n/qsmd_n
10	ale/qs0
11	n.c.
12	V_{SS}
13	V_{SS}
14	n.c.
15	n.c.
16	x1
17	x2
18	reset
19	clkout
20	ardy

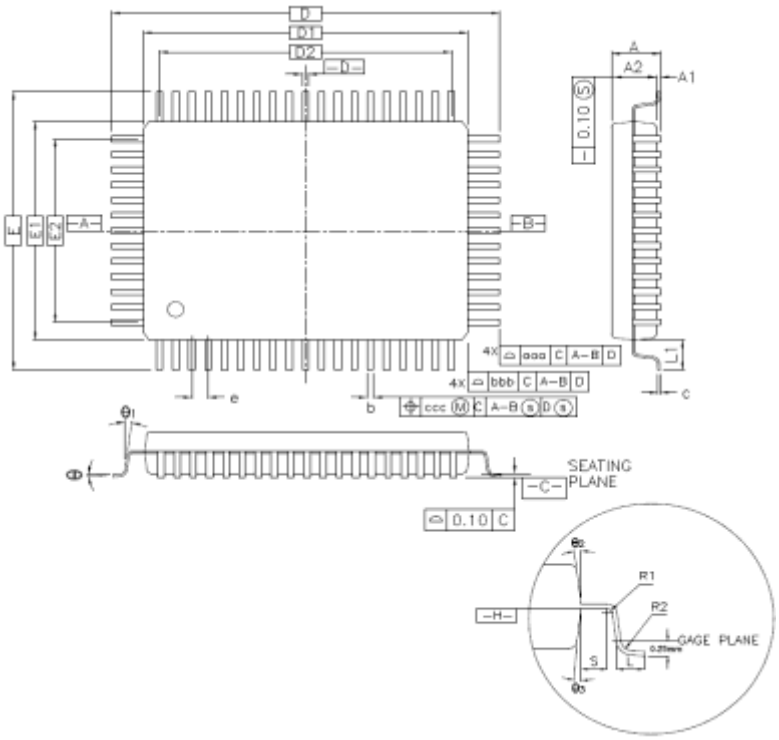
Pin	Name
21	s2_n
22	s1_n
23	s0_n
24	n.c.
25	hlda
26	hold
27	srdy
28	lock_n
29	test_n /busy
30	nmi
31	int0
32	int1/select_n
33	V_{CC}
34	V_{CC}
35	int2/inta0_n
36	int3/inta1_n
37	dt/r_n
38	den_n
39	mcs0 _n/pereq
40	mcs1 _n/error_n

Pin	Name
41	mcs2_n
42	mcs3_n/nps_n
43	n.c.
44	n.c.
45	ucs_n
46	lcs_n
47	pcs6 _n/a2
48	pcs5_n/a1
49	pcs4_n
50	pcs3_n
51	pcs2_n
52	pcs1_n
53	V_{SS}
54	pcs0_n
55	res_n
56	tmr out 1
57	tmr out 0
58	tmr in 1
59	tmr in 0
60	drq1

Pin	Name
61	drq0
62	n.c.
63	n.c.
64	ad0
65	a8
66	ad1
67	a9
68	ad2
69	a10
70	ad3
71	a11
72	V_{CC}
73	V_{CC}
74	ad4
75	a12
76	ad5
77	a13
78	ad6
79	a14
80	ad7

2.1.6 PQFP Physical Dimensions

The physical dimensions for the 80 PQFP are as shown in Figure 6.



Legend:

Symbol	Millimeter Min	Nom	Max	Inch Min	Nom	Max
A	–	–	3.40	–	–	0.134
A1	0.25	–	–	0.010	–	–
A2	2.55	2.72	3.05	0.100	0.107	0.120
D	23.90 Basic			0.941 Basic		
D1	20.00 Basic			0.787 Basic		
E	17.90 Basic			0.705 Basic		
E1	14.00 Basic			0.551 Basic		
R2	0.013	–	0.30	0.005	–	0.012
R1	0.013	–	–	0.005	–	–
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	–	–	0°	–	–
θ2, θ3[a]	7° REF			7° REF		
θ2, θ3[b]	15° REF			15° REF		
c	0.11	0.15	0.23	0.004	0.006	0.009
L	0.73	0.88	1.03	0.029	0.035	0.041
L1	1.95 REF			0.077 REF		
S	0.40	–	–	0.016	–	–
b	0.30	0.35	0.45	0.012	0.014	0.018
e	0.80 BSC			0.031 BSC		
D2	18.40 REF			0.724		
E2	12.00 REF			0.472		
Tolerances of Form and Position						
aaa	0.25			0.010		
bbb	0.20			0.008		
ccc	0.20			0.008		

[a]Alloy 42 L/F.
[b]Copper L/F.

Notes:
1. Dimension D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. Dimension D1 and E1 do not include mold mismatch and are determined a datum plane –H–.
2. Dimension b does not include dambar protrusion. Allowable dambar protrusion will not cause the lead width to exceed the maximum b dimension by more than 0.08mm. Dambar cannot be located on the lower radius of the lead foot.

Figure 6. PQFP Physical Package Dimensions

2.1.7 IA186XL 80 LQFP Package

The pinout for the IA186XL 80 LQFP package is as shown in Figure 7. The corresponding pinout is provided in Table 5.

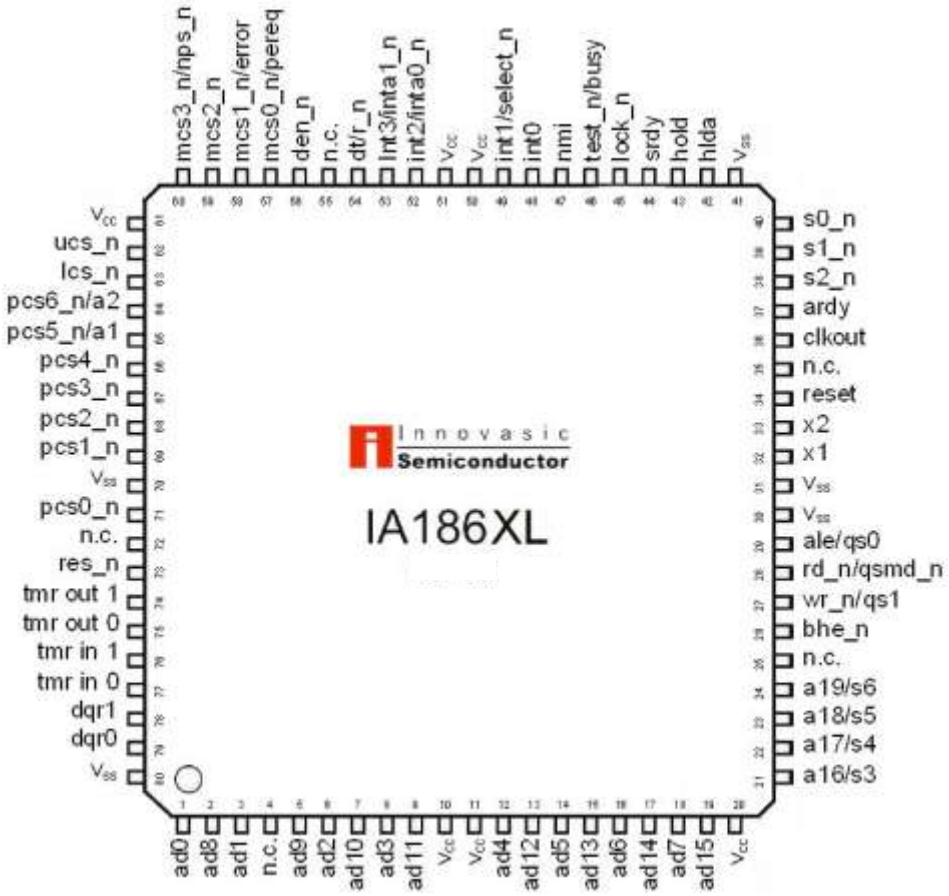


Figure 7. IA186XL 80-Lead LQFP Package Diagram

Table 5. IA186XL 80-Lead LQFP Pin Listing

Pin	Name
1	ad0
2	ad8
3	ad1
4	n.c.
5	ad9
6	ad2
7	ad10
8	ad3
9	ad11
10	v_{cc}
11	v_{cc}
12	ad4
13	ad12
14	ad5
15	ad13
16	ad6
17	ad14
18	ad7
19	ad15
20	v_{cc}

Pin	Name
21	a16/s3
22	a17/s4
23	a18/s5
24	a19/s6
25	n.c.
26	bhe_n
27	wr_n/qs1
28	rd_n/qsmd_n
29	ale/qs0
30	v_{ss}
31	v_{ss}
32	x1
33	x2
34	reset
35	n.c.
36	clkout
37	ardy
38	s2_n
39	s1_n
40	s0_n

Pin	Name
41	v_{ss}
42	hlda
43	hold
44	srdy
45	lock_n
46	test_n/busy
47	nmi
48	int0
49	int1/select_n
50	v_{cc}
51	v_{cc}
52	int2/inta0_n
53	int3/inta1_n
54	dt/r_n
55	n.c.
56	den_n
57	mcs0_n/pereq
58	mcs1_n/error
59	mcs2_n
60	mcs3_n/nps_n

Pin	Name
61	v_{cc}
62	ucs_n
63	lcs_n
64	pcs6_n/a2
65	pcs5_n/a1
66	pcs4_n
67	pcs3_n
68	pcs2_n
69	pcs1_n
70	v_{ss}
71	pcs0_n
72	n.c.
73	res_n
74	tmr out 1
75	tmr out 0
76	tmr in 1
77	tmr in 0
78	dqr1
79	dqr0
80	v_{ss}

2.1.8 IA188XL 80 LQFP Package

The pinout for the IA188XL 80 LQFP package is as shown in Figure 8. The corresponding pinout is provided in Table 6.

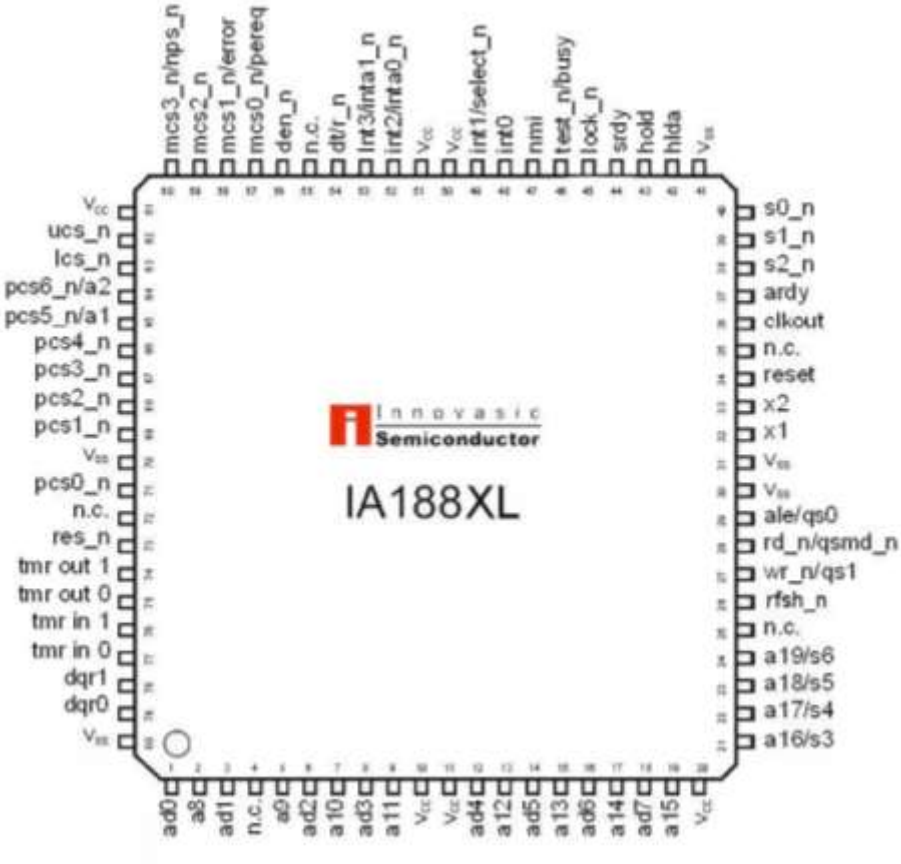


Figure 8. IA188XL 80-Lead LQFP Package Diagram

Table 6. IA188XL 80-Lead LQFP Pin Listing

Pin	Name
1	ad0
2	a8
3	ad1
4	n.c.
5	a9
6	ad2
7	a10
8	ad3
9	a11
10	v_{cc}
11	v_{cc}
12	ad4
13	a12
14	ad5
15	a13
16	ad6
17	a14
18	ad7
19	a15
20	v_{cc}

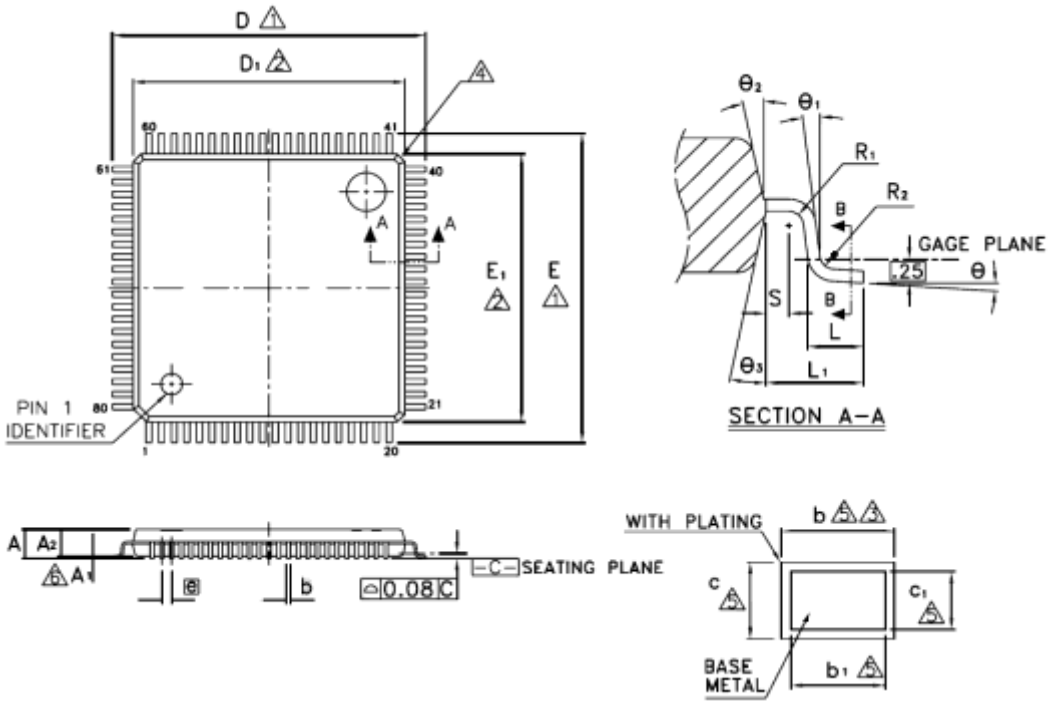
Pin	Name
21	a16/s3
22	a17/s4
23	a18/s5
24	a19/s6
25	n.c.
26	rfsh_n
27	wr_n/qs1
28	rd_n/qsmd_n
29	ale/qs0
30	v_{ss}
31	v_{ss}
32	x1
33	x2
34	reset
35	n.c.
36	clkout
37	ardy
38	s2_n
39	s1_n
40	s0_n

Pin	Name
41	v_{ss}
42	hlda
43	hold
44	srdy
45	lock_n
46	test_n/busy
47	nmi
48	int0
49	int1/select_n
50	v_{cc}
51	v_{cc}
52	int2/inta0_n
53	Int3/inta1_n
54	dt/r_n
55	n.c.
56	den_n
57	mcs0_n/pereq
58	mcs1_n/error
59	mcs2_n
60	mcs3_n/nps_n

Pin	Name
61	v_{cc}
62	ucs_n
63	lcs_n
64	pcs6_n/a2
65	pcs5_n/a1
66	pcs4_n
67	pcs3_n
68	pcs2_n
69	pcs1_n
70	v_{ss}
71	pcs0_n
72	n.c.
73	res_n
74	tmr out 1
75	tmr out 0
76	tmr in 1
77	tmr in 0
78	dqr1
79	dqr0
80	v_{ss}

2.1.9 LQFP Physical Dimensions

The physical dimensions for the 80 LQFP are as shown in Figure 9.



Legend:

Symbol	Dimension in mm Min	Nom	Max	Dimension in Inch Min	Nom	Max
A	–	–	1.60	–	–	0.063
A_1	0.05	–	0.15	0.002	–	0.006
A_2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
b_1	0.17	0.20	0.23	0.007	0.008	0.009
c	0.09	–	0.20	0.004	–	0.008
c_1	0.09	–	0.16	0.004	–	0.006
D	14.00 BSC			0.551 BSC		
D_1	12.00 BSC			0.472 BSC		
E	14.00 BSC			0.551 BSC		
E_1	12.00 BSC			0.472 BSC		
e	0.50 BSC			0.020 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
R_1	0.08	–	–	0.003	–	–
R_2	0.08	–	0.20	0.003	–	0.008
S	0.20	–	–	0.008	–	–
θ	0°	3.5°	7°	0°	3.5°	7°
θ_1	0°	–	–	0°	–	–
θ_2	11°	12°	13°	11°	12°	13°
θ_3	11°	12°	13°	11°	12°	13°

1. To be determined at seating plane C.
2. Dimensions D1 and E1 do not include mold protrusion. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Dimension b does not include dambar protrusion. Dambar cannot be located on the lower radius of the foot.
4. Exact shape of each corner is optional.
5. These dimensions apply to the flat section of the lead between 0.10 and 0.25mm from the lead tip.
6. A1 is defined as the distance from the seating plane to the lowest point of the package body.

Notes:
1. Exact shape of each corner is optional.
2. Controlling dimension: mm.

Figure 9. LQFP Physical Package Dimensions

2.2 IA186XL Pin/Signal Descriptions

Descriptions of the pin and signal functions for the IA186XL microcontroller are provided in Table 7.

Several of the IA186XL pins have different functions depending on the operating mode of the device. Each of the different signals supported by a pin is listed and defined in Table 7, indexed alphabetically in the first column of the table. Additionally, the name of the pin associated with the signal as well as the pin numbers for the PLCC, PQFP, and LQFP packages are provided in the "Pin" column. Signals not used in a specific package type are designated "NA."

Table 7. IA186XL Pin/Signal Descriptions

Signal	Pin				Description
	Name	PLCC	PQFP	LQFP	
a1	pcs5_n/a1	31	48	65	Latched address bit a1. Output.
a2	pcs6_n/a2	32	47	64	Latched address bit a2. Output.
a16	a16/s3	68	3	21	**a**ddress bits **16**–**19**. Output. These pins provide the four most-significant bits of the Address Bus during T_1 only. During T_2, T_3, T_W and T_4 they provide bus status.
a17	a17/s4	67	4	22	
a18	a18/s5	66	5	23	
a19	a19/s6	65	6	24	
ad0	ad0	17	64	1	**a**ddress/**d**ata bits **0**–**15**. Input/Output. These pins provide the multiplexed Address Bus and Data Bus. During the address portion of the IA186XL bus cycle, Address Bits [0–15] are presented on the bus and can be latched using the ale signal (see next table entry). During the data portion of the bus cycle, data are present on these lines.
ad1	ad1	15	66	3	
ad2	ad2	13	68	6	
ad3	ad3	11	70	8	
ad4	ad4	8	74	12	
ad5	ad5	6	76	14	
ad6	ad6	4	78	16	
ad7	ad7	2	80	18	
ad8	ad8	16	65	2	
ad9	ad9	14	67	5	
ad10	ad10	12	69	7	
ad11	ad11	10	71	9	
ad12	ad12	7	75	13	
ad13	ad13	5	77	15	
ad14	ad14	3	79	17	
ad15	ad15	1	1	19	

Table 7. IA186XL Pin/Signal Descriptions *(Continued)*

Signal	Pin				Description
	Name	PLCC	PQFP	LQFP	
ale	ale/qs0	61	10	29	**a**ddress **l**atch **e**nable. Output. Active High. This signal is used to latch valid address information on the falling edge of **ale** during the address portion of a bus cycle.
ardy	ardy	55	20	37	**a**synchronous **r**ea**dy**. Input. Indicates to the processor the addressed memory space or i/o device will complete the transfer.
bhe_n	bhe_n	64	7	26	**b**yte **h**igh **e**nable. Output. Active Low. When **bhe_n** is asserted (low), it indicates that the bus cycle in progress is transferring data over the upper half of the data bus. Additionally, **bhe_n** and **ad0** encode the following bus information: ad0 bhe_n Bus Status 0 0 Word Transfer 0 1 Even Byte Transfer 1 0 Odd Byte Transfer 1 1 Refresh Operation (Enhanced Mode) Note: **bhe_n** is used as **refresh_n** in the IA188XL.
busy	test_n/busy	47	29	46	**busy**. Input. Active High. Used in Enhanced Mode. When the **busy** input is asserted, it causes the IA186XL to suspend operation during the execution of the Intel 80C187 Numerics Coprocessor instructions. Operation resumes when the pin is sampled low.
clkout	clkout	56	19	36	**cl**oc**k ou**tput. Output. The **clkout** pin provides a timing reference for inputs and outputs of the IA186XL. This clock output is one-half the input clock (**clkin**) frequency. The **clkout** signal has a 50% duty cycle, transitioning every falling edge of **clkin**.
den_n	den_n	39	38	56	**d**ata **en**able. Output. Active Low. This signal is used to enable bidirectional transceivers in a buffered system. The **den_n** signal is asserted (low) only when data are to be transferred on the bus.
drq0	drq0	18	61	79	**d**ma **r**e**q**uest **0** or **1.** Input. Asserted high by an external device to request DMA Channel 0 or 1 to perform a transfer. These signals are level-triggered and internally synchronized.
drq1	drq1	19	60	78	

Table 7. IA186XL Pin/Signal Descriptions *(Continued)*

Signal	Pin				Description
	Name	PLCC	PQFP	LQFP	
dt/r_n	dt/r_n	40	37	54	**d**ata **t**ransmit**/r**eceive. Output. This signal is used to control the direction of data flow for bidirectional buffers in a buffered system. When **dt/r_n** is high, the direction indicated is transmit; when **dt/r_n** is low, the direction indicated is receive.
error_n	mcs1_n/error_n	37	40	58	**error**. Input. Active Low. When this signal is asserted (low), it indicates that the last numerics coprocessor operation resulted in an exception condition.
hlda	hlda	51	25	42	**h**o**ld a**cknowledge. Output. Active High. When **hlda** is asserted (high), it indicates that the IA186XL has relinquished control of the local bus to another bus master in response to a HOLD request (see next table entry). When **hlda** is asserted, the IA186XL data bus and control signals are floated allowing another bus master to drive the signals directly.
hold	hold	50	26	43	**hold**. Input. Active High. This signal is a request indicating that an external bus master wishes to gain control of the local bus. The IA186XL will relinquish control of the local bus between instruction boundaries not conditioned by a LOCK prefix.
int0	int0	45	31	48	**int**errupt N (N = **0**–**3**). Input. Active High. These maskable inputs interrupt program flow and cause execution to continue at an interrupt vector of a specific interrupt type as follows: • **int0**: Type 12 • **int1**: Type 13 • **int2**: Type 14 • **int3**: Type 15 To allow interrupt expansion, **int0** and **int1** can be used with the interrupt acknowledge signals **inta0_n** and **inta1_n** (see next table entries).
int1	int1	44	32	49	
int2	int2/inta0_n	42	35	52	
int3	int3/inta1_n	41	36	53	
inta 0_n	int2/inta0_n	42	35	52	**int**errupt **a**cknowledge**.** Output. Active low. When used with external interrupt controllers.
inta 1_n	int3/inta1_n	41	36	53	

Table 7. IA186XL Pin/Signal Descriptions *(Continued)*

Signal	Pin				Description
	Name	PLCC	PQFP	LQFP	
lcs_n	lcs_n	33	46	63	**l**ower **c**hip **s**elect. Output. Active Low. This pin provides a chip select signal that will be asserted (low) whenever the address of a memory bus cycle is within the address space programmed for that output.
lock_n	lock_n	48	28	45	**lock**. Output. Active Low. When asserted (low), this signal indicates that the bus cycle in progress cannot be interrupted. While **lock_n** is active, the IA186XL will not service bus requests such as HOLD. When **resin_n** is active, this pin is weakly held high and must not be driven low.
mcs0_n	mcs0_n/pereq	38	39	57	**m**id-range memory **c**hip **s**elect. Output.
mcs1_n	mcs1_n/error_n	37	40	58	
mcs2_n	mcs2_n	36	41	59	
mcs3_n	mcs3_n/nps_n	35	42	60	
n.c.	n.c.	NA	2, 11, 14, 15, 24, 43, 44, 62, 63	4, 25, 35, 55, 72	**n**ot **c**onnected.
nmi	nmi	46	30	47	**n**on-**m**askable **i**nterrupt. Input. Active High. When the **nmi** signal is asserted (high) it causes a Type 2 interrupt.
nps_n	mcs3_n/nps_n	35	42	60	**n**umeric **p**rocessor **s**elect
pcs0_n	pcs0_n	25	54	71	**p**eripheral **c**hip **s**elect signals **0**–**6**. Output.
pcs1_n	pcs1_n	27	52	69	
pcs2_n	pcs2_n	28	51	68	
pcs3_n	pcs3_n	29	50	67	
pcs4_n	pcs4_n	30	49	66	
pcs5_n	pcs5_n/a1	31	48	65	
pcs6_n	pcs6_n/a2	32	47	64	
pereq	mcs0_n/pereq	38	39	57	numerics co**p**rocessor **e**xternal **req**uest. Input. Active High. When asserted (high), this signal indicates that a data transfer between an Intel 80C187 Numerics Coprocessor and the CPU is pending.

Table 7. IA186XL Pin/Signal Descriptions *(Continued)*

Signal	Pin				Description
	Name	PLCC	PQFP	LQFP	
qs0	ale/qs0	61	10	29	**q**ueue **s**tatus **0**, **q**ueue **s**tatus **1.** Output. QS1 QS0 0 0 No Queue operations 0 1 First byte of opcode pulled from Queue 1 1 Additional bytes pulled from Queue 1 0 Queue is flushed
qs1	wr_n/qs1	63	8	27	
qsmd_n	rd_n/qsmd_n	62	9	28	**q**ueue **s**tatus **mod**e. Input. Sampled at reset.
rd_n	rd_n/qsmd_n	62	9	28	**r**ea**d**. output. Active Low. When asserted (low), **rd_n** indicates that the accessed memory or I/O device must drive data from the location being accessed onto the data bus.
res_n	res_n	24	55	73	**res_n**. Input. Forces the processor to terminate present activity, reset the internal logic, and enter a dormant state until res_n goes high.
reset	reset	57	18	34	**reset** is an output signal indicating the CPU is being reset. It can be used as a system reset.
s0_n	s0_n	52	23	40	**s**tatus [**2**:**0**]_**n** are outputs. During a bus cycle, the status (i.e., type) of cycle is encoded on these lines as follows: **s2_n** **s1_n** **s0_n** Bus Cycle Status 0 0 0 Interrupt Acknowledge 0 0 1 Read I/O 0 1 0 Write I/O 0 1 1 Processor HALT 1 0 0 Queue Instruction Fetch 1 0 1 Read Memory 1 1 0 Write Memory 1 1 1 No Bus Activity
s1_n	s1_n	53	22	39	
s2_n	s2_n	54	21	38	
s3	a16/s3	68	3	21	**s**tatus [**6**:**3]** are Outputs. Bus Cycle A19/s6 A18/s5 A17/s4 A16/s3 T_1 A19 A18 A17 A16 T_2 N 0 0 0 T_3 N 0 0 0 T_w N 0 0 0 T_4 N 0 0 0 N = 0 for CPU bus cycle. N = 1 for DMA or refresh cycle.
s4	a17/s4	67	4	22	
s5	a18/s5	66	5	23	
s6	a19/s6	65	6	24	
srdy	srdy	49	27	44	**s**ynchronous **r**ea**dy.** Input.

Table 7. IA186XL Pin/Signal Descriptions *(Continued)*

Signal	Pin				Description
	Name	PLCC	PQFP	LQFP	
test_n	test_n/busy	47	29	46	**test**. Input. Active Low. When the **test_n** input is high (i.e., not asserted), it causes the IA186XL to suspend operation during the execution of the WAIT instruction. Operation resumes when the pin is sampled low (asserted).
tmr in 0	tmr in 0	20	59	77	**timer 0 input**. Input. Depending on the Timer Mode programmed for Timer 0, this input is used either as clock input or a control signal.
tmr in 1	tmr in 1	21	58	76	**timer 1 input**. Input. Depending on the Timer Mode programmed for Timer 1, this input is used either as clock input or a control signal.
tmr out 0	tmr out 0	22	57	75	**timer 0 output**. Output. Depending on the Timer Mode programmed for Timer 0, this output can provide a single pulse or a repetitive waveform.
tmr out 1	tmr out 1	23	56	74	**timer 1 output**. Output. Depending on the Timer Mode programmed for Timer 1, this output can provide a single clock or a repetitive waveform.
ucs_n	ucs_n	34	45	62	**u**pper **c**hip **s**elect. Output. Active Low. This pin provides a chip select signal that will be asserted (low) whenever the address of a memory bus cycle is within the address space programmed for that output.
V_{CC}	V_{CC}	9, 43	33, 34, 72, 73	10, 11, 20, 50, 51, 61	Power (**V_{CC}**). This pin provides power for the IA186XL device. It must be connected to a +5V DC power source.
V_{SS}	V_{SS}	26, 60	12, 13, 53	30, 31, 41, 70, 80	Ground (**V_{SS}**). This pin provides the digital ground (0V) for the IA186XL. It must be connected to a V_{SS} board plane.
wr_n	wr_n/qs1	63	8	27	**wr**ite. Output. Active Low. When asserted (low), **wr_n** indicates that data available on the data bus are to be latched into the accessed memory or I/O device.
x1	x1	59	16	32	**x1** and **x2** are inputs for the crystal
x2	x2	58	17	33	

2.3 IA188XL Pin/Signal Descriptions

Descriptions of the pin and signal functions for the IA188XL microcontroller are provided in Table 8.

Several of the IA188XL pins have different functions depending on the operating mode of the device. Each of the different signals supported by a pin is listed and defined in Table 8, indexed alphabetically in the first column of the table. Additionally, the name of the pin associated with the signal as well as the pin numbers for the PLCC, QFP, and LQFP packages are provided in the "Pin" column.

Table 8. IA188XL Pin/Signal Descriptions

Signal	Pin				Description
	Name	PLCC	PQFP	LQFP	
a1	pcs5_n/a1	31	48	65	Latched address bit **a1.** Output.
a2	pcs6_n/a2	32	47	64	Latched address bit **a2.** Output.
a16	a16/s3	68	3	21	**a**ddress bits **16**–**19**. Output. These pins provide the four most-significant bits of the Address Bus during T_1 only. During T_2, T_3, T_W and T_4 they provide bus status.
a17	a17/s4	67	4	22	
a18	a18/s5	66	5	23	
a19	a19/s6	65	6	24	
ad0	ad0	17	64	1	**a**ddress/**d**ata bits **0 - 15**. Input/Output. These pins provide the multiplexed Address Bus and Data Bus. During the address portion of the IA188XL bus cycle, address bits 0 through 15 are presented on the bus and can be latched using the ale signal (see next table entry). During the data portion of the IA188XL bus cycle, data are present on these lines.
ad1	ad1	15	66	3	
ad2	ad2	13	68	6	
ad3	ad3	11	70	8	
ad4	ad4	8	74	12	
ad5	ad5	6	76	14	
ad6	ad6	4	78	16	
ad7	ad7	2	80	18	
a8	a8	16	65	2	valid address information is provided for the entire bus cycle
a9	a9	14	67	5	
a10	a10	12	69	7	
a11	a11	10	71	9	
a12	a12	7	75	13	
a13	a13	5	77	15	
a14	a14	3	79	17	
a15	a15	1	1	19	

Table 8. IA188XL Pin/Signal Descriptions *(Continued)*

Signal	Pin				Description
	Name	PLCC	PQFP	LQFP	
ale	ale/qs0	61	10	29	**a**ddress **l**atch **e**nable. Output. Active High. This signal is used to latch address information during the address portion of a bus cycle.
ardy	ardy	55	20	37	**a**synchronous **r**ea**dy.** Input. Indicates to the processor the addressed memory space or i/o device will complete the transfer.
clkout	clkout	56	19	36	**cl**oc**k ou**tput. Output. The **clkout** pin provides a timing reference for inputs and outputs of the IA188XL. This clock output is one-half the input clock (**clkin**) frequency. The **clkout** signal has a 50% duty cycle, transitioning every falling edge of **clkin**.
den_n	den_n	39	38	56	**d**ata **en**able. Output. Active Low. This signal is used to enable bidirectional transceivers in a buffered system. The **den_n** signal is asserted (low) only when data are to be transferred on the bus.
drq0	drq0	18	61	79	**d**ma **req**uest **0** or **1.** Input. Asserted high by an external device to request DMA Channel 0 or 1 to perform a transfer. These signals are level-triggered and internally synchronized
drq1	drq1	19	60	78	
dt/r_n	dt/r_n	40	37	54	**d**ata **t**ransmit**/r**eceive. Output. This signal is used to control the direction of data flow for bidirectional buffers in a buffered system. When **dt/r_n** is high, the direction indicated is transmit; when **dt/r_n** is low, the direction indicated is receive.

Table 8. IA188XL Pin/Signal Descriptions *(Continued)*

Signal	Pin				Description
	Name	PLCC	PQFP	LQFP	
hlda	hlda	51	25	42	**h**o**ld a**cknowledge. Output. Active High. When **hlda** is asserted (high), it indicates that the IA188XL has relinquished control of the local bus to another bus master in response to a HOLD request (see next table entry). When **hlda** is asserted, the IA188XL data bus and control signals are floated allowing another bus master to drive the signals directly.
hold	hold	50	26	43	**hold**. Input. Active High. This signal is a request indicating that an external bus master wishes to gain control of the local bus. The IA188XL will relinquish control of the local bus between instruction boundaries not conditioned by a LOCK prefix.
int0	int0	45	31	48	**int**errupt N (N = **03**). Input. Active High. These maskable inputs interrupt program flow and cause execution to continue at an interrupt vector of a specific interrupt type as follows: • **int0**: Type 12 • **int1**: Type 13 • **int2**: Type 14 • **int3**: Type 15 To allow interrupt expansion, **int0** and **int1** can be used with the interrupt acknowledge signals **inta0_n** and **inta1_n** (see next table entries).
int1	int1	44	32	49	
int2	int2/inta0_n	42	35	52	
int3	int3/inta1_n	41	36	53	
inta 0_n	int2/inta0_n	42	35	52	**int**errupt **a**cknowledge**.** Output. Active low. When used with external interrupt controllers.
inta 1_n	int3/inta1_n	41	36	53	
lcs_n	lcs_n	33	46	63	**l**ower **c**hip **s**elect. Output. Active Low. This pin provides a chip select signal that will be asserted (low) whenever the address of a memory bus cycle is within the address space programmed for that output.

Table 8. IA188XL Pin/Signal Descriptions *(Continued)*

Signal	Pin				Description
	Name	PLCC	PQFP	LQFP	
lock_n	lock_n	48	28	45	**lock**. Output. Active Low. When asserted (low), this signal indicates that the bus cycle in progress cannot be interrupted. While **lock_n** is active, the IA188XL will not service bus requests such as HOLD. When **resin_n** is active, this pin is weakly held high and must not be driven low.
mcs0_n	mcs0_n/pereq	38	39	57	**m**id-range memory **c**hip **s**elect. Output.
mcs1_n	mcs1_n/error_n	37	40	58	
mcs2_n	mcs2_n	36	41	59	
mcs3_n	mcs3_n/nps_n	35	42	60	
n.c.	n.c.	NA	2, 11, 14, 15, 24, 43, 44, 62, 63	4, 25, 35, 55, 72	**n**ot **c**onnected
nmi	nmi	46	30	47	**n**on-**m**askable **i**nterrupt. Input. Active High. When the **nmi** signal is asserted (high) it causes a Type 2 interrupt .
pcs0_n	pcs0_n	25	54	71	**p**eripheral **c**hip **s**elect signals **0**–**6.** Output.
pcs1_n	pcs1_n	27	52	69	
pcs2_n	pcs2_n	28	51	68	
pcs3_n	pcs3_n	29	50	67	
pcs4_n	pcs4_n	30	49	66	
pcs5_n	pcs5_n/a1	31	48	65	
pcs6_n	pcs6_n/a2	32	47	64	
qs0	ale/qs0	61	10	29	**q**ueue **s**tatus **0**, **q**ueue **s**tatus **1.** Output. QS1 QS0 0 0 No Queue operations 0 1 First byte of opcode pulled from Queue 1 1 Additional bytes pulled from Queue 1 0 Queue is flushed
qs1	wr_n/qs1	63	8	27	
qsmd_n	rd_n/qsmd_n	62	9	28	**q**ueue **s**tatus **mod**e. Input. Sampled at reset.
rd_n	rd_n/qsmd_n	62	9	28	**rea**d. output. Active Low. When asserted (low), **rd_n** indicates that the accessed memory or I/O device must drive data from the location being accessed onto the data bus.

Table 8. IA188XL Pin/Signal Descriptions *(Continued)*

Signal	Pin Name	Pin PLCC	Pin PQFP	Pin LQFP	Description
res_n	res_n	24	55	73	**res_n**. Input. Forces the processor to terminate its present activity, reset the internal logic, and enter a dormant state until res_n goes high.
reset	reset	57	18	34	**reset** is an output signal indicating the CPU is being reset. It can be used as a system reset.
rfsh_n	rfsh_n	64	7	26	**refresh.** Output. **rfsh_n** is asserted low to indicate a refresh bus cycle.
s0_n	s0_n	52	23	40	**s**tatus [**2**:**0**]_**n** are outputs. During a bus cycle the status (i.e., type) of cycle is encoded on these lines as follows: **s2_n s1_n s0_n** Bus Cycle Status 0 0 0 Interrupt Acknowledge 0 0 1 Read I/O 0 1 0 Write I/O 0 1 1 Processor HALT 1 0 0 Queue Instruction Fetch 1 0 1 Read Memory 1 1 0 Write Memory 1 1 1 No Bus Activity
s1_n	s1_n	53	22	39	
s2_n	s2_n	54	21	38	
s3	a16/s3	68	3	21	**s**tatus [**6**:**3**] are outputs. Bus Cycle A19/s6 A18/s5 A17/s4 A16/s3 T_1 A19 A18 A17 A16 T_2 N 0 0 0 T_3 N 0 0 0 T_w N 0 0 0 T_4 N 0 0 0 N = 0 for CPU bus cycle. N = 1 for DMA or refresh cycle.
s4	a17/s4	67	4	22	
s5	a18/s5	66	5	23	
s6	a19/s6	65	6	24	
srdy	srdy	49	27	44	**s**ynchronous **rea**d**y.** Input.
test_n	test_n/busy	47	29	46	**test**. Input. Active Low. When the **test_n** input is high (i.e., not asserted), it causes the IA188XL to suspend operation during the execution of the WAIT instruction. Operation resumes when the pin is sampled low (asserted).
tmr in 0	tmr in 0	20	59	77	**timer 0 in**put. Input. Depending on the Timer Mode programmed for Timer 0, this input is used either as clock input or a control signal.
tmr in 1	tmr in 1	21	58	76	**timer 1 in**put. Input. Depending on the Timer Mode programmed for Timer 1, this input is used either as clock input or a control signal.

Table 8. IA188XL Pin/Signal Descriptions *(Continued)*

Signal	Pin				Description
	Name	PLCC	PQFP	LQFP	
tmr out 0	tmr out 0	22	57	75	**tim**er **0 out**put. Output. Depending on the Timer Mode programmed for Timer 0, this output can provide a single pulse or a repetitive waveform.
tmr out 1	tmr out 1	23	56	74	**tim**er **1 out**put. Output. Depending on the Timer Mode programmed for Timer 1, this output can provide a single pulse or a repetitive waveform.
ucs_n	ucs_n	34	45	62	**u**pper **c**hip **s**elect. Output. Active Low. This pin provides a chip select signal that will be asserted (low) whenever the address of a memory bus cycle is within the address space programmed for that output.
V_{cc}	V_{cc}	9, 43	33, 34, 72, 73	10, 11, 20, 50, 51, 61	Power (**V_{cc}**). This pin provides power for the IA188XL device. It must be connected to a +5V DC power source.
V_{ss}	V_{ss}	26, 60	12, 13, 53	30, 31, 41, 70, 80	Ground (**V_{ss}**). This pin provides the digital ground (0V) for the IA186XL. It must be connected to a V_{SS} board plane.
wr_n	wr_n/qs1	63	8	27	**wr**ite. Output. Active Low. When asserted (low), **wr_n** indicates that data available on the data bus are to be latched into the accessed memory or I/O device.
x1	x1	59	16	32	**x1** and **x2** are inputs for the crystal
x2	x2	58	17	33	

3. Maximum Ratings, Thermal Characteristics, and DC Parameters

For the Innovasic Semiconductor IA186XL and IA188XL microcontrollers, the absolute maximum ratings, thermal characteristics, and DC parameters are provided in Tables 9 through 11, respectively.

Table 9. IA186XL and IA188XL Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	−40°C to +125°C
Supply Voltage with Respect to v_{ss}	−0.3V to +6.0V
Voltage on Pins other than Supply with Respect to v_{ss}	−0.3V to +(Vcc + 0.3)V

Table 10. IA186XL and IA188XL Thermal Characteristics

Symbol	Characteristic	Value	Units
T_A	Ambient Temperature	-40°C to 85°C	°C
P_D	Power Dissipation	MHz × ICC × V/1000	W
Θ_{Ja}	68-Lead PLCC Package	32	°C/W
	80-Lead PQFP Package	46	
	80-Lead LQFP Package	52	
T_J	Average Junction Temperature	$T_A + (P_D \times \Theta_{Ja})$	°C

Table 11. IA186XL and IA188XL DC Parameters

Symbol	Parameter	Min	Max	Units	Notes
5.0 Volt Operation V_{CC}	Supply Voltage	4.5	5.5	V	–
V_{IL}	Input Low Voltage	−0.3	0.3 V_{CC}	V	Input Hysteresis on resin_n = 0.50V
V_{IH}	Input High Voltage	0.7 V_{CC}	V_{CC} + 0.3	V	–
V_{OL}	Output Low Voltage $V_{CC = 5.0V}$	–	0.4	V	I_{OL} = 12 mA
V_{OH}	Output High Voltage $V_{CC = 4.5V}$	3.5	-	V	I_{OH} = −12 mA
I_{LEAK}	Input Leakage Current for Pins: ad0-ad15, ad0-ad7 (IA188XL), resin_n, clkin, t0in_in, t1in_in, drq0, drq1, int0, int1, rmi, hold, srdy, ardy, int2_inta0_n, int3_inta1_n	–	± 1	µA	$0V \le V_{IN} \le V_{CC}$
	Input Leakage Current for pin (@5V): ucs_n, lcs_n, mcs0_n_pereq, mcs1_n_error_n, rd_n, test_n_busy	-.227	-.833	mA	V_{IN} = 0V
I_{LO}	Output Leakage Current	–	± 10	µA	$0.45V \le V_{OUT} \le V_{CC}$
I_{ID}	Supply Current (IDLE) - @ 50 MHz	-	90	mA	-
C_{IN}	Input Pin Capacitance	0	5	pF	T_F = 1 MHz
C_{OUT}	Output Pin Capacitance	0	5	pF	T_F = 1 MHz
Operating temperature is −40°C to 85°C.					

4. Functional Description

The follow descriptions apply to both the IA186XL and IA188XL unless otherwise noted. Module descriptions are followed by descriptions of special operating modes.

Additional information on the operation and programming of the 80C186XL/80C188XL can be found in the following Intel® publications:

- *80C186XL/80C188XL and 80L186XL/80L188XL 16-Bit High-Integration Embedded Processors* (272433-006)
- *80C186XL/80C188XL Microprocessor User's Manual* (270830-00n)

4.1 Device Architecture

Architecturally, the IA186XL microcontrollers include the following functional modules:

– Bus Interface Unit
– Clock Generator
– Interrupt Control Unit
– Timer/Counter Unit
– Chip-Select Unit
– Refresh Control Unit
– Power-Save Control
– DMA Unit

A functional block diagram of the IA186XL/IA188XL is shown in Figure 10. Descriptions of the functional modules are provided in the follow subsections.

Control registers for the peripheral modules are located in a 256 byte control block. This block can be mapped to either memory or I/O space. The offset map for addressing these registers is given in Table 12.

4.1.1 Bus Interface Unit

A local bus controller generates the local bus control signals. It also employs a hold/hlda protocol for relinquishing the local bus to other bus masters. Its outputs can be used to enable external buffers and to direct the flow of data on and off the local bus. The bus controller is responsible for generating 20 bits of address, read and write strobes, bus-cycle status information and data. This controller is also responsible for reading data from the local bus during a read operation. Synchronous and asynchronous ready input pins are provided to extend a bus cycle beyond the minimum four clocks. The bus controller also generates two control signals (den_n

and dt/r_n) when interfacing to external transceiver chips. This capability allows the addition of transceivers for simple buffering of the multiplexed address/data bus. During reset, the local bus controller performs the following actions:

1. Floats ad0–15 (ad0–8), a16–19 (a9–a19), bhe_n (rfsh_n), dt/r_n
2. Drives ale LOW
3. Drives hlda LOW
4. Drives lock_n HIGH and then floats
5. Drives den_n, rd_n, and wr_n HIGH for one clock cycle, then floats them
6. Drives s0_n, s1_n and s2_n to the inactive state (all HIGH) and then floats them

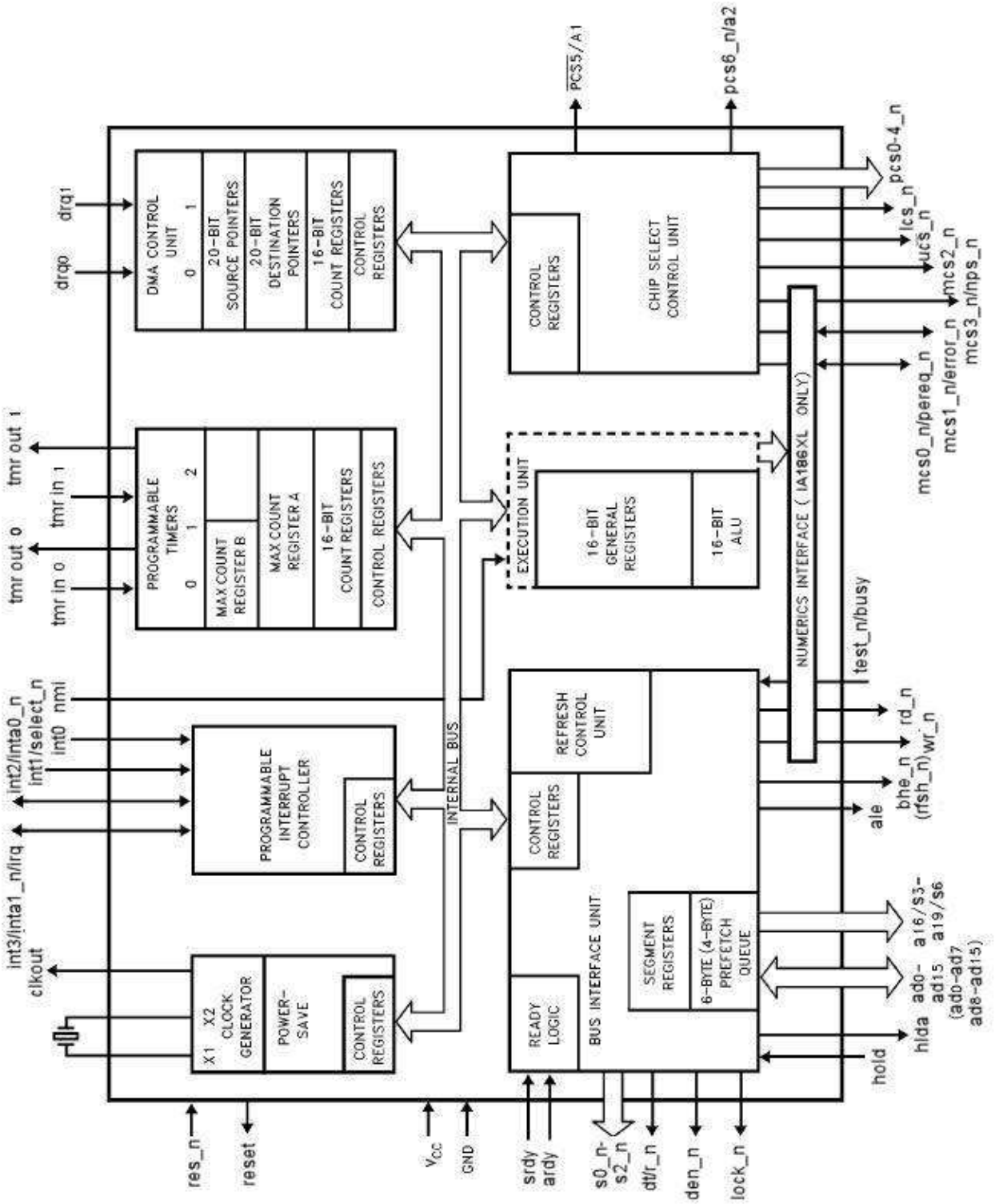


Figure 10. IA186XL/IA188XL Functional Block Diagram

The rd_n/qsmd_n, ucs_n, lcs_n, mcs0_n/pereq, mcs1_n/error_n, and test_n/busy pins include internal pull-ups that are active while res_n is applied. The state of these pins during reset controls invoking various alternative operating modes as described below:

1 ONCE Mode – ucs_n and lcs_n driven low.
2 Enhanced Mode – test_n/busy driven low then high.
3 Queue Status Mode – rd_n/qsmd_n driven low.

4.1.2 Clock Generator

The IA186XL/IA188XL uses an on-chip clock generator to supply internal and external clocks. The clock generator makes use of a crystal oscillator and includes a divide-by-two counter.

Figure 11 shows the various operating modes of the clock circuit. The clock circuit can use either a parallel resonant fundamental mode crystal network (A) or a third-overtone mode crystal network (B), or it can be driven by an external clock source (C).

The following parameters are recommended when choosing a crystal:

- Temperature Range: Application Specific
- ESR (Equivalent Series Resistance): 60Ω max
- C0 (Shunt Capacitance of Crystal): 7.0 pF max
- CL (Load Capacitance): 20 pF ± 2 pF
- Drive Level: 2 mW max

4.1.3 Interrupt Control Unit

The IA186XL operates with several interrupt sources. A separate Interrupt Control Unit manages all sources based on priority to be individually handled by the CPU. The DMA and Timers produce internally generated requests. There are five externally generated interrupts - a single NMI and 4 others.

4.1.4 Timer/Counter Unit

There are three programmable internal timers in the IA186XL. Two are very flexible and can be configured for many tasks. Each of these has a single input used for either control or clocking, and a single output to generate waveforms. The third timer is simpler and can only be clocked from an internal source. It can be used for simple timing applications. It can also be used as a prescaler to the other two timers or as a trigger for DMA requests.

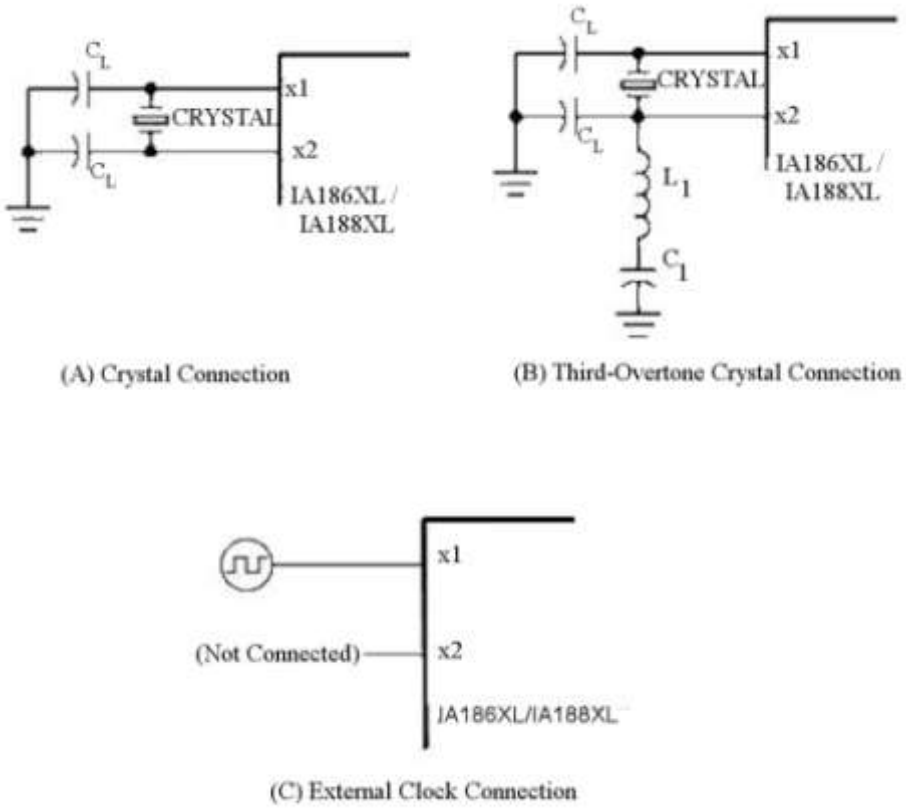


Figure 11. Clock Circuit Connection Options

4.1.5 Chip-Select/Ready Generation Logic

The IA186XL provides programmable chip-select generation for memories and peripherals. The chip can be programmed to provide READY or WAIT state generation. It can also provide latched address bits A1 and A2. Chip select behavior is the same whether the access is generated by the CPU or the DMA.

A total of 6 chip selects are dedicated for different memory ranges. A single select for upper memory (ucs_n), with a fixed end address of 0FFFFH, is good for use as system memory since the reset vector points to FFFF0H. A single select for lower memory (lcs_n), with a fixed start address of 0H, is good for interrupt vectors which reside beginning at address 00000H. There are also four selects for anywhere else (exclusive of ucs_n and lcs_n areas) in the 1 Mbyte memory in the user-locatable memory block. For the middle chip selects, the base address and block size are programmable, while only the block size for the upper and lower chip selects are programmable.

Seven additional chip selects can be programmed to access either peripherals or memory in seven contiguous fixed blocks of 128 bytes each. A single base address is programmable for these chip selects.

A programmable number of wait states (0 - 3) can be used to generate an internal ready for each chip select range. The IA186XL can be programmed to use or not use the external ready signal with or without the internal wait states from the internal ready being factored in.

At reset, the Chip-Select/Ready Logic will be configured as follows:

1. All chip-select outputs will be driven HIGH
2. Exiting RESET, the UCS control register (UMCS) is set to FFFBH, providing chip select to a 1-Kbyte block of memory with 3 wait states in combined with external ready.
3. All other chip select control registers are undefined after reset. The CPU must configure these control registers before the corresponding chips selects will become active.

4.1.6 DMA

The IA186XL includes a DMA controller with two channels. Transfers can occur between any combination of Memory and I/O space, to either odd or even address. Data size can be either 8 or 16 bits, except on the IA188XL it can only be 8 bits.

There are separate 20-bit source and destination pointers for each channel. These pointers can be configured to increment, decrement or stay static after each transfer. For word transfers, pointers are incremented or decrement by two and for byte transfers, by one. One bus cycle is required to fetch data and one cycle to deposit it.

4.1.7 DRAM Refresh Control Unit

When in Enhanced Mode, the IA186XL supports DRAM refresh cycles. Reads are automatically generated at a programmable time interval. If enabled, chip selects are active for these reads.

4.1.8 Power-Save Control

When in Enhanced Mode, the IA186XL supports a power save mode of operation. The internal clock frequency is divided by a programmable amount. This affects all internal logic including, timers, the refresh control unit and clkout generation. Timers and the refresh control unit need to be reprogrammed accordingly when going in and out of power save if you wish to maintain the same real time references.

4.2 Operating Modes

During reset the IA186XL can be configured to enable special operating modes described as follows.

4.2.1 Enhanced Mode

If Enhanced Mode is enabled, the IA186XL has DRAM refresh, Power-Save and coprocessor support available in addition to the normal features available in Compatible Mode. Enhanced Mode will be invoked automatically if a coprocessor is attached. It can also be entered by tying the reset output to the test_n/busy input. An internal pull-up keeps the part from entering Enhanced mode during normal operation.

When not in Enhanced Mode, none of the Enhanced Mode registers can be accessed. Queue-Status functions, except for the coprocessor support, will be available when not in Enhanced Mode.

4.2.2 Queue Status Mode

When Queue Status Mode is enabled, information about the instruction queue is output on the ale/qs0 and wr_n/qs1 pins. To enter Queue Status Mode, the rd_n input should be tied low. It is sampled at reset, and if low, Queue Status Mode is entered. An internal pull-up keeps the part from entering Queue Status mode during normal operation.

4.2.3 ONCE Mode

ONCE mode is a special test mode where all pins are set to a high impedance state. ONCE mode is entered by forcing lcs_n and ucs_n low during reset. These pins are sampled on the rising edge of res but should be held low for at least a full clock cycle after res goes high. ONCE mode is exited by reseting the part with lcs_n and ucs_n high. Internal pull-ups keep the part from entering ONCE mode during normal operation.

4.2.4 Math Coprocessor (IA186XL Only)

When Enhanced mode is enabled, the IA186XL is configured to interface with a math coprocessor via three of the middle chip select pins. Pin mcs0/pereq is used for Processor Extension Request. Pin mcs1/error is used for coprocessor error indication. Pin mcs3/nps is used for Numeric Processor Select.

Table 12. Internal Register Map

PCB Offset	Function	PCB Offset	Function	PCB Offset	Function	PCB Offset	Function
00H	Reserved	40H	Reserved	80H	Reserved	C0H	D0SRCL
02H	Reserved	42H	Reserved	82H	Reserved	C2H	D0SRCH
04H	Reserved	44H	Reserved	84H	Reserved	C4H	D0DSTL
06H	Reserved	46H	Reserved	86H	Reserved	C6H	D0DSTH
08H	Reserved	48H	Reserved	88H	Reserved	C8H	D0TC
0AH	Reserved	4AH	Reserved	8AH	Reserved	CAH	D0CON
0CH	Reserved	4CH	Reserved	8CH	Reserved	CCH	Reserved
0EH	Reserved	4EH	Reserved	8EH	Reserved	CEH	Reserved
10H	Reserved	50H	T0CNT	90H	Reserved	D0H	D1SRCL
12H	Reserved	52H	T0CMPA	92H	Reserved	D2H	D1SRCH
14H	Reserved	54H	T0CMPB	94H	Reserved	D4H	D1DSTL
16H	Reserved	56H	T0CON	96H	Reserved	D6H	D1DSTH
18H	Reserved	58H	T1CNT	98H	Reserved	D8H	D1TC
1AH	Reserved	5AH	T1CMPA	9AH	Reserved	DAH	D1CON
1CH	Reserved	5CH	T1CMPB	9CH	Reserved	DCH	Reserved
1EH	Reserved	5EH	T1CON	9EH	Reserved	DEH	Reserved
20H	Reserved	60H	T2CNT	A0H	UMCS	E0H	RFBASE
22H	EOI	62H	T2CMPA	A2H	LMCS	E2H	RFTIME
24H	POLL	64H	Reserved	A4H	PACS	E4H	RFCON
26H	POLLSTS	66H	T2CON	A6H	MMCS	E6H	Reserved
28H	IMASK	68H	Reserved	A8H	MPCS	E8H	Reserved
2AH	PRIMSK	6AH	Reserved	AAH	Reserved	EAH	Reserved
2CH	INSERV	6CH	Reserved	ACH	Reserved	ECH	Reserved
2EH	REQST	6EH	Reserved	AEH	Reserved	EEH	Reserved
30H	INSTS	70H	Reserved	B0H	Reserved	F0H	PWRSAV
32H	TCUCON	72H	Reserved	B2H	Reserved	F2H	PWRCON
34H	DMA0CON	74H	Reserved	B4H	Reserved	F4H	Reserved
36H	DMA1CON	76H	Reserved	B6H	Reserved	F6H	Step ID[1]
38H	I0CON	78H	Reserved	B8H	Reserved	F8H	Reserved
3AH	I1CON	7AH	Reserved	BAH	Reserved	FAH	Reserved
3CH	I2CON	7CH	Reserved	BCH	Reserved	FCH	Reserved
3EH	I3CON	7EH	Reserved	BEH	Reserved	FEH	RELREG

Note:

[1] The **Step ID** register (offset 0xF6) for Revision 1 of the Innovasic device is read-only, and is uniquely identified in software by having a value of 0x0081. The original Intel device established a value between 0x0000 and 0x0003, depending on the revision of the part.

5. AC Specifications

5.1 Major Cycle Timings – Read Cycle

- T_A = -40°C to +85°C, V_{CC} = 5V ± 10%
- All timings are measured at 1.5V and 50 pF loading on CLKOUT unless otherwise noted.
- All output test conditions are with C_L = 50 pF.
- For AC tests, input V_{IL} = 0.45V and V_{IH} = 2.4V except at X1 where $V_{IH} = V_{CC} – 0.5V$.

Table 13. Major Cycle Timings – Read Cycle

Symbol	Parameter	Values		Unit	Test Conditions
		Min	Max		
T_{DVCL}	Data in Setup (A/D)	8		ns	
T_{CLDX}	Data in Hold (A/D)	3		ns	
T_{CHSV}	Status Active Delay	3	20	ns	
T_{CHSH}	Status Inactive Delay	3	20	ns	
T_{CLAV}	Address Valid Delay	3	20	ns	
T_{CLAX}	Address Hold	0		ns	
T_{CLDV}	Data Valid Delay	3	20	ns	
T_{CHDX}	Status Hold Time	10		ns	
T_{CHLH}	ALE Active Delay		20	ns	
T_{LHLL}	ALE Width	T_{CLCL} - 15		ns	
T_{CHLL}	ALE Inactive Delay		20	ns	
T_{AVLL}	Address Valid to ALE Low	T_{CLCH} - 10		ns	Equal Loading
T_{LLAX}	Address Hold from ALE Inactive	T_{CHCL} - 8		ns	Equal Loading
T_{AVCH}	Address Valid to Clock High	0		ns	
T_{CLAZ}	Address Float Delay	T_{CLAX}	20	ns	
T_{CLCSV}	Chip-Select Active Delay	3	20	ns	
T_{CXCSX}	Chip-Select Hold from Command Inactive	T_{CLCH} - 10		ns	Equal Loading
T_{CHCSX}	Chip-Select Inactive Delay	3	17	ns	
T_{DXDL}	DEN Inactive to DT/R Low	0		ns	Equal Loading
T_{CVCTV}	Control Active Delay 1	3	17	ns	
T_{CVDEX}	DEN Inactive Delay	3	17	ns	
T_{CHCTV}	Control Active Delay 2	3	20	ns	
T_{CLLV}	LOCK Valid/Invalid Delay	3	17	ns	
T_{AZRL}	Address Float to RD Active	0		ns	
T_{CLRL}	RD Active Delay	3	20	ns	
T_{RLRH}	RD Pulse Width	$2T_{CLCL}$ - 15		ns	
T_{CLRH}	RD Inactive Delay	3	20	ns	
T_{RHLH}	RD Inactive to ALE High	T_{CLCH} - 14		ns	Equal Loading

T_{RHAV}	RD Inactive to Address Active	T_{CLCL} - 15		ns	Equal Loading

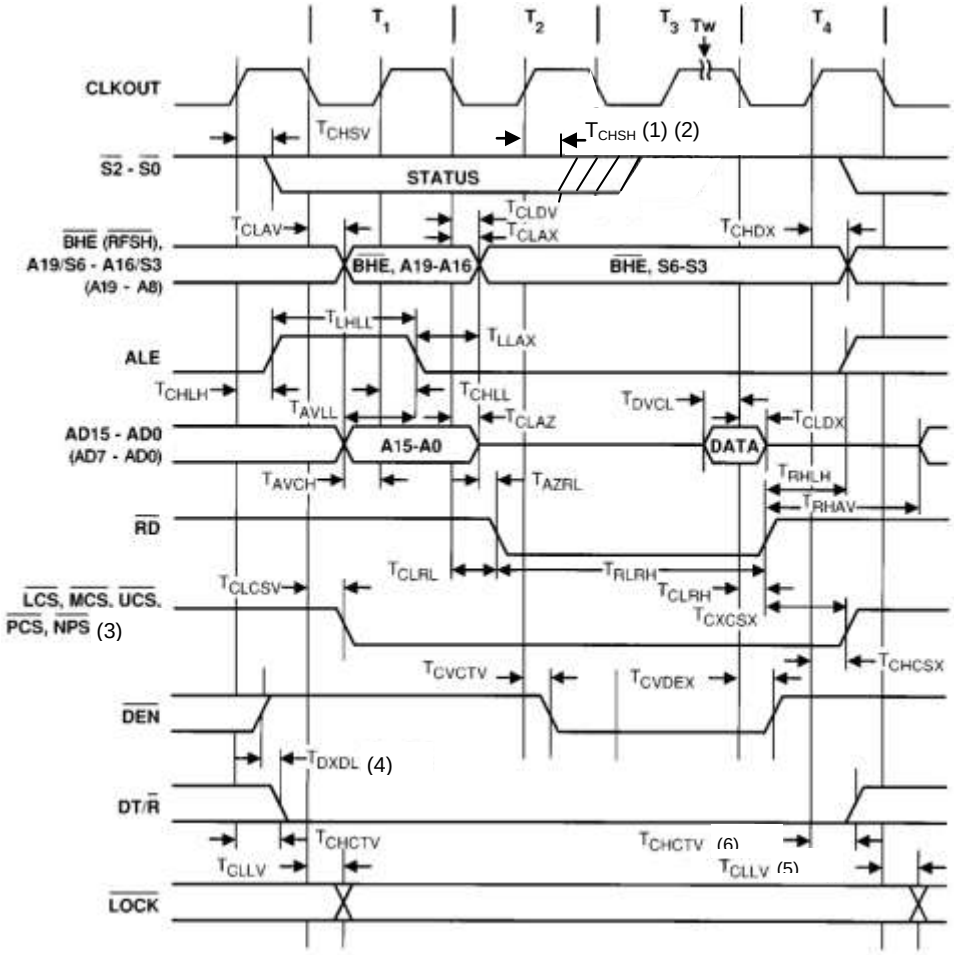


Figure 12. Read Cycle Waveforms

Please note that pins indicated in the parentheses are for the IA188XL version.

Notes:

(1) The OEM part (80C186XL) operates differently in that it deasserts on the falling edge of CLKOUT.
(2) Status is inactive in the state preceding T4.
(3) Only TCLCSV is applicable if latched A1 and A2 are selected instead of PCS5 and PCS6.
(4) This applies when a write cycle is followed by read cycle.
(5) This is T1 of next bus cycle.
(6) This changes in the T-state preceding the next bus cycle if followed by a write.

5.2 Major Cycle Timings – Write Cycle

- T_A = -40°C to +85°C, V_{CC} = 5V ± 10%
- All timings are measured at 1.5V and 50 pF loading on CLKOUT unless otherwise noted.
- All output test conditions are with C_L = 50 pF.
- For AC tests, input V_{IL} = 0.45V and V_{IH} = 2.4V except at X1 where $V_{IH} = V_{CC} – 0.5V$.

Table 14. Major Cycle Timings – Write Cycle

Symbol	Parameter	Values		Unit	Test Conditions
		Min	Max		
T_{CHSV}	Status Active Delay	3	20	ns	
T_{CHSH}	Status Inactive Delay	3	20	ns	
T_{CLAV}	Address Valid Delay	3	20	ns	
T_{CLAX}	Address Hold	0		ns	
T_{CLDV}	Data Valid Delay	3	20	ns	
T_{CHDX}	Status Hold Time	10		ns	
T_{CHLH}	ALE Active Delay		20	ns	
T_{LHLL}	ALE Width	T_{CLCL} - 15		ns	
T_{CHLL}	ALE Inactive Delay		20	ns	
T_{AVLL}	Address Valid to ALE Low	T_{CLCH} - 10		ns	Equal Loading
T_{LLAX}	Address Hold from ALE Inactive	T_{CHCL} - 10		ns	Equal Loading
T_{AVCH}	Address Valid to Clock High	0		ns	
T_{CLDOX}	Data Hold Time	3		ns	
T_{CVCTV}	Control Active Delay 1	3	20	ns	
T_{CVCTX}	Control Inactive Delay	3	17	ns	
T_{CLCSV}	Chip-Select Active Delay	3	20	ns	
T_{CXCSX}	Chip-Select Hold from Command Inactive	T_{CLCH} - 10		ns	Equal Loading
T_{CHCSX}	Chip-Select Inactive Delay	3	17	ns	
T_{DXDL}	DEN Inactive to DT/R Low	0		ns	Equal Loading
T_{CLLV}	LOCK Valid/Invalid Delay	3	17	ns	
T_{WLWH}	WR Pulse Width	2_{TCLCL} - 15		ns	
T_{WHLH}	WR Inactive to ALE High	T_{CLCH} - 14		ns	Equal Loading
T_{WHDX}	Data Hold after WR	T_{CLCL} - 10		ns	Equal Loading
T_{WHDEX}	WR Inactive to DEN Inactive	T_{CLCH} - 10		ns	Equal Loading

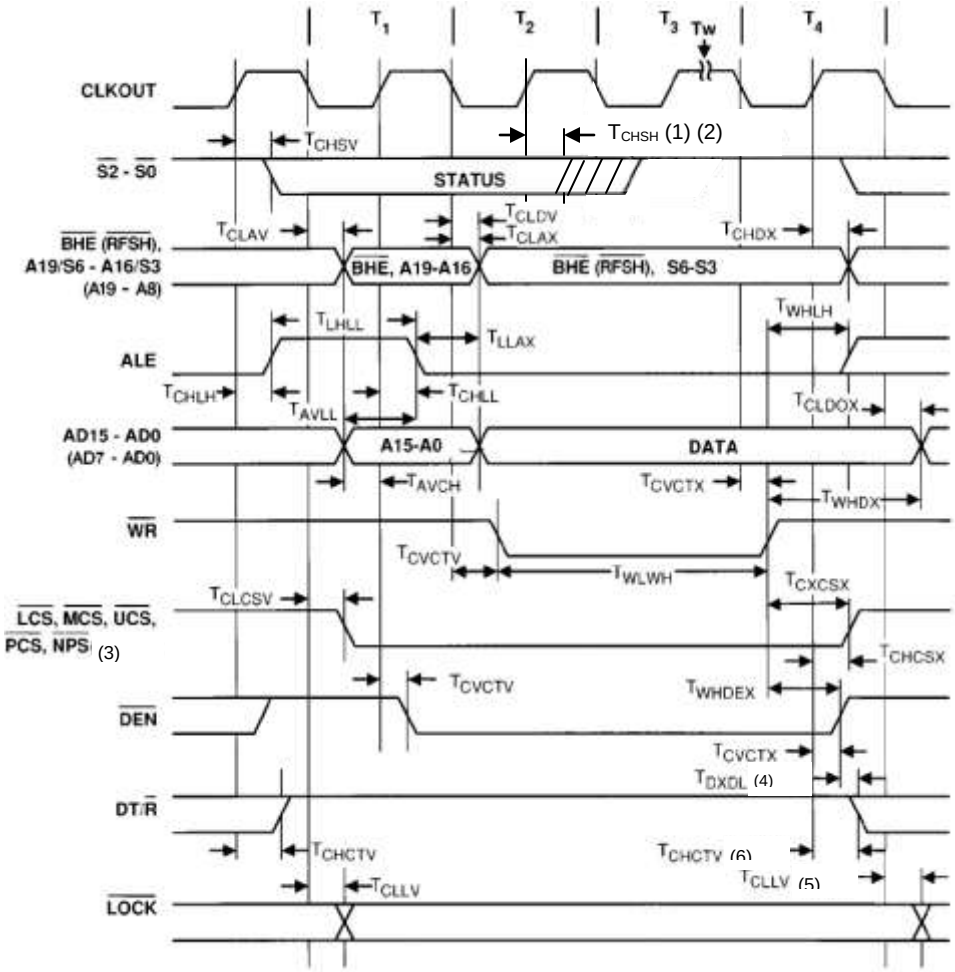


Figure 13. Write Cycle Waveforms

Please note that pins indicated in the parentheses are for the IA188XL version.

Notes:

(1) The OEM part (80C186XL) operates differently in that it deasserts on the falling edge of CLKOUT.
(2) Status is inactive in the state preceding T4.
(3) Only TCLCSV is applicable if latched A1 and A2 are selected instead of PCS5 and PCS6.
(4) This applies when a write cycle is followed by a read cycle.
(5) This is T1 of next bus cycle.
(6) This changes in the T-state preceding the next bus cycle if followed by a read, INTA or halt.

5.3 Major Cycle Timings – Interrupt Acknowledge Cycle

- T_A = -40°C to +85°C, V_{CC} = 5V ± 10%
- All timings are measured at 1.5V and 50 pF loading on CLKOUT unless otherwise noted.
- All output test conditions are with C_L = 50 pF.
- For AC tests, input V_{IL} = 0.45V and V_{IH} = 2.4V except at X1 where $V_{IH} = V_{CC} – 0.5V$.

Table 15. Major Cycle Timings – Interrupt Acknowledge Cycle

Symbol	Parameter	Values		Unit	Test Conditions
		Min	Max		
T_{DVCL}	Data in Setup (A/D)	8		ns	
T_{CLDX}	Data in Hold (A/D)	3		ns	
T_{CHSV}	Status Active Delay	3	20	ns	
T_{CHSH}	Status Inactive Delay	3	20	ns	
T_{CLAV}	Address Valid Delay	3	20	ns	
T_{AVCH}	Address Valid to Clock High	0		ns	
T_{CLAX}	Address Hold	0		ns	
T_{CLDV}	Data Valid Delay	3	20	ns	
T_{CHDX}	Status Hold Time	10		ns	
T_{CHLH}	ALE Active Delay		20	ns	
T_{LHLL}	ALE Width	T_{CLCL} - 15		ns	
T_{CHLL}	ALE Inactive Delay		20	ns	
T_{AVLL}	Address Valid to ALE Low	T_{CLCH} - 10		ns	Equal Loading
T_{LLAX}	Address Hold to ALE Inactive	T_{CHCL} - 10		ns	Equal Loading
T_{CLAZ}	Address Float Delay	T_{CLAX}	20	ns	
T_{CVCTV}	Control Active Delay 1	3	17	ns	
T_{CVCTX}	Control Inactive Delay	3	17	ns	
T_{DXDL}	DEN Inactive to DT/R Low	0		ns	Equal Loading
T_{CHCTV}	Control Active Delay 2	3	20	ns	
T_{CVDEX}	DEN Inactive Delay (Non-Write Cycles)	3	17	ns	
T_{CLLV}	LOCK Valid/Invalid Delay	3	17	ns	

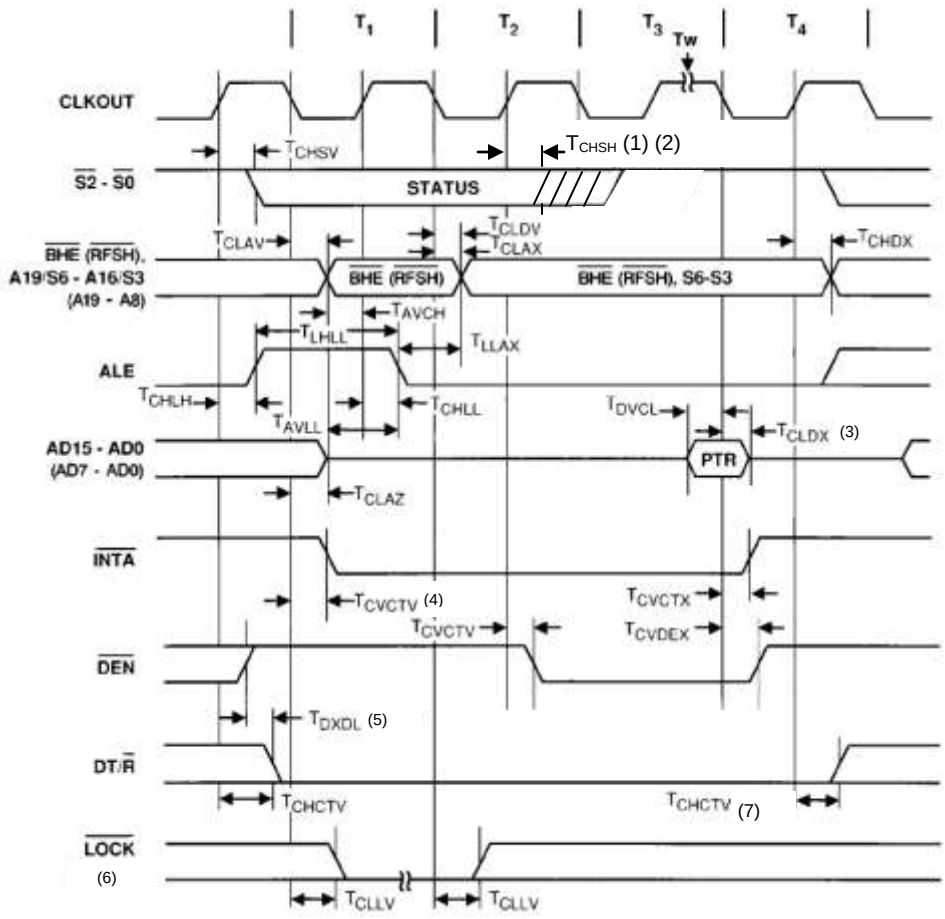


Figure 14. Interrupt Acknowledge Cycle Waveforms

Please note that pins indicated in the parentheses are for the IA188XL version.

Notes:

(1) The OEM part (80C186XL) operates differently in that it deasserts on the falling edge of CLKOUT.
(2) Status is inactive in the state preceding T4.
(3) The data hold time lasts only until INTA goes inactive, even if the INTA transition occurs prior to TCLDX (min).
(4) INTA occurs one clock later in Slave Mode.
(5) This applies when a write cycle is followed by an interrupt acknowledge cycle.
(6) LOCK is active upon T1 of the first interrupt acknowledge cycle, and inactive upon T2 of the second interrupt acknowledge cycle.
(7) Changes in T-state preceding next bus cycle if followed by write.

5.4 Software Halt Cycle Timings

- T_A = -40°C to +85°C, V_{CC} = 5V ± 10%
- All timings are measured at 1.5V and 50 pF loading on CLKOUT unless otherwise noted.
- All output test conditions are with C_L = 50 pF.
- For AC tests, input V_{IL} = 0.45V and V_{IH} = 2.4V except at X1 where $V_{IH} = V_{CC} – 0.5V$.

Table 16. Software Halt Cycle Timings

Symbol	Parameter	Values		Unit	Test Conditions
		Min	Max		
T_{CHSV}	Status Active Delay	3	20	ns	
T_{CHSH}	Status Inactive Delay	3	20	ns	
T_{CLAV}	Address Valid Delay	3	20	ns	
T_{CHLH}	ALE Active Delay		20	ns	
T_{LHLL}	ALE Width	T_{CLCL} - 15		ns	
T_{CHLL}	ALE Inactive Delay		20	ns	
T_{DXDL}	DEN Inactive to DT/R Low		0	ns	Equal Loading
T_{CHCTV}	Control Active Delay 2	3	20	ns	

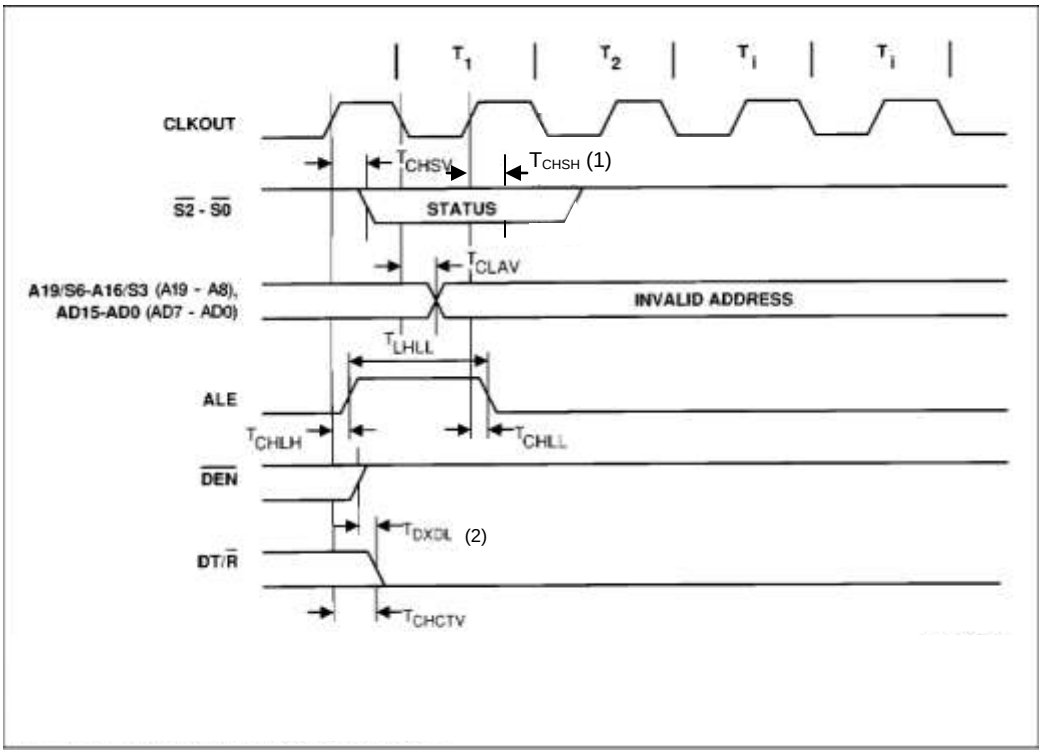


Figure 15. Software Halt Cycle Waveforms

Please note that pins indicated in the parentheses are for the IA188XL version.

Notes:
(1) The OEM part (80C186XL) operates differently in that it deasserts on the falling edge of CLKOUT.
(2) This applies when a write cycle is followed by a halt cycle.

5.5 Clock Timings

- T_A = -40°C to +85°C, V_{CC} = 5V ± 10%
- All timings are measured at 1.5V and 50 pF loading on CLKOUT unless otherwise noted.
- All output test conditions are with C_L = 50 pF.
- For AC tests, input V_{IL} = 0.45V and V_{IH} = 2.4V except at X1 where $V_{IH} = V_{CC} – 0.5V$.

Table 17. Clock Timings

Symbol	Parameter	Values		Unit	Test Conditions
		Min	Max		
T_{CKIN}	CLKIN Period	20	∞	ns	
T_{CLCK}	CLKIN Low Time	8	∞	ns	1.5V(2)
T_{CHCK}	CLKIN High Time	8	∞	ns	1.5V(2)
T_{CKHL}	CLKIN Fall Time		5	ns	3.5 to 1.0V
T_{CKLH}	CLKIN Rise Time		5	ns	1.0 to 3.5V
T_{CICO}	CLKIN to CLKOUT Skew		17	ns	
T_{CLCL}	CLKOUT Period	40	∞	ns	
T_{CLCH}	CLKOUT Low Time	0.5 T_{CLCL} - 5		ns	C_L = 100 pF(3)
T_{CHCL}	CLKOUT High Time	0.5 T_{CLCL} - 5		ns	C_L = 100 pF(4)
T_{CH1CH2}	CLKOUT Rise Time		6	ns	1.0 to 3.5V
T_{CL2CL1}	CLKOUT Fall Time		6	ns	3.5 to 1.0V

NOTES:
1. External clock applied to X1 and X2 not connected.
2. T_{CLCK} and T_{CHCK} (CLKIN Low and High times) should not have a duration less than 40% of T_{CKIN}.
3. Tested under worst case conditions: V_{CC} = 5.5V. T_A = 70°C.
4. Tested under worst case conditions: V_{CC} = 4.5V. T_A = 0°C.

5.6 Ready, Peripheral and Queue Status Timings

- T_A = -40°C to +85°C, V_{CC} = 5V ± 10%
- All timings are measured at 1.5V and 50 pF loading on CLKOUT unless otherwise noted.
- All output test conditions are with C_L = 50 pF.
- For AC tests, input V_{IL} = 0.45V and V_{IH} = 2.4V except at X1 where $V_{IH} = V_{CC} – 0.5V$.

Table 18. Ready, Peripheral and Queue Status Timings

Symbol	Parameter	Values		Unit	Test Conditions
		Min	Max		
T_{SRYCL}	Synchronous Ready (SRDY) Transition Setup Time(1)	8		ns	
T_{CLSRY}	SRDY Transition Hold Time(1)	8		ns	
T_{ARYCH}	ARDY Resolution Transition Setup Time(2)	8		ns	
T_{CLARX}	ARDY Active Hold Time(1)	8		ns	
T_{ARYCHL}	ARDY Inactive Holding Time	8		ns	
T_{ARYLCL}	Asynchronous Ready (ARDY) Setup Time(1)	10		ns	
T_{INVCH}	INTx, NMI, TEST, BUSY, TMR IN Setup Time(2)	8		ns	
T_{INVCL}	DRQ0, DRQ1 Setup Time(2)	8		ns	
T_{CLTMV}	Timer Output Delay		17	ns	
T_{CHQSV}	Queue Status Delay		22	ns	

NOTES:
1. To guarantee proper operation.
2. To guarantee recognition at clock edge.

5.7 Reset and HOLD/HLDA Timings

- T_A = -40°C to +85°C, V_{CC} = 5V ± 10%
- All timings are measured at 1.5V and 50 pF loading on CLKOUT unless otherwise noted.
- All output test conditions are with C_L = 50 pF.
- For AC tests, input V_{IL} = 0.45V and V_{IH} = 2.4V except at X1 where $V_{IH} = V_{CC} – 0.5V$.

Table 19. Reset and HOLD/HLDA Timings

Symbol	Parameter	Values		Unit	Test Conditions
		Min	Max		
T_{RESIN}	RES Setup	15		ns	
T_{HVCL}	HOLD Setup(1)	8		ns	
T_{CLAZ}	Address Float Delay	T_{CLAX}	20	ns	
T_{CLAV}	Address Valid Delay	3	20	ns	
T_{CLRO}	Reset Delay		17	ns	
T_{CLHAV}	HLDA Valid Delay	3	17	ns	
T_{CHCZ}	Command Lines Float Delay		22	ns	
T_{CHCV}	Command Lines Valid Delay (after Float)		20	ns	

NOTE:
1. To guarantee recognition at next clock.

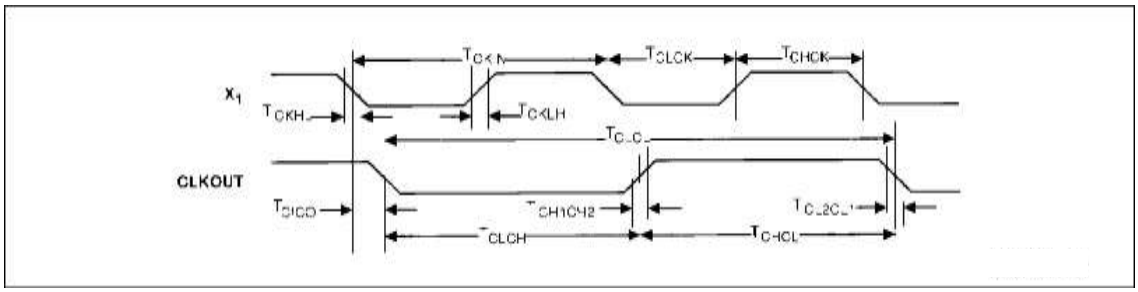


Figure 16. Clock Waveforms

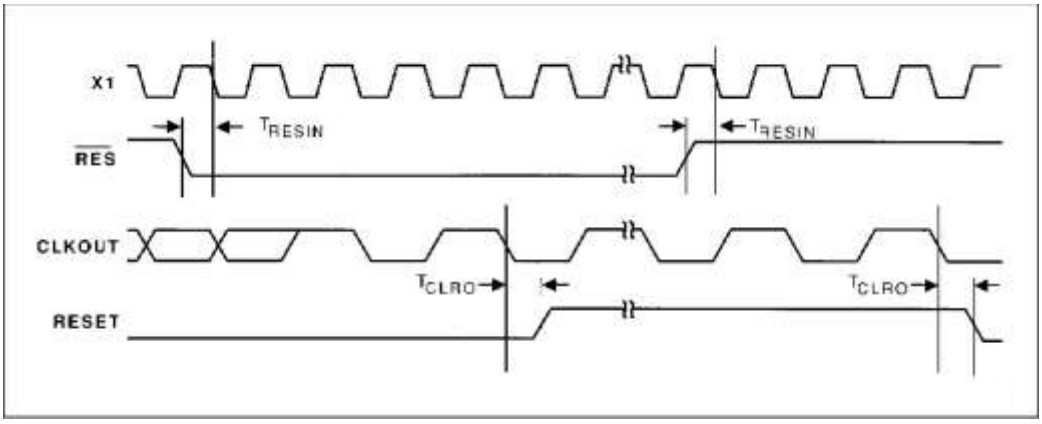


Figure 17. Reset Waveforms

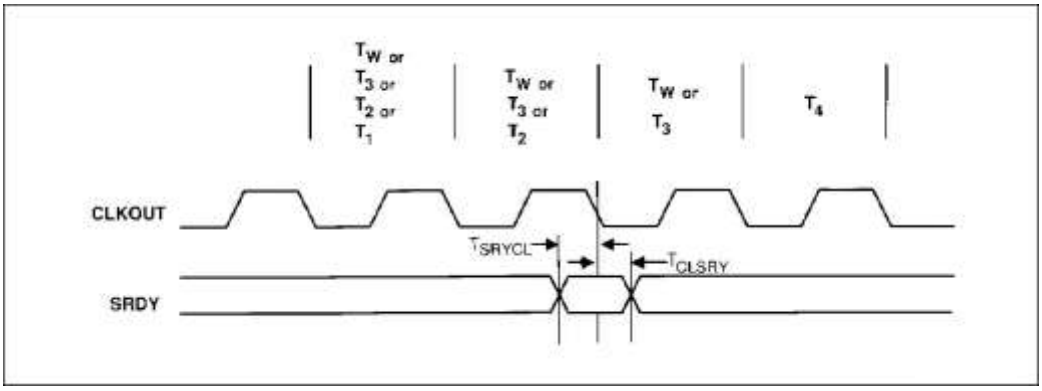


Figure 18. Synchronous Ready (SRDY) Waveforms

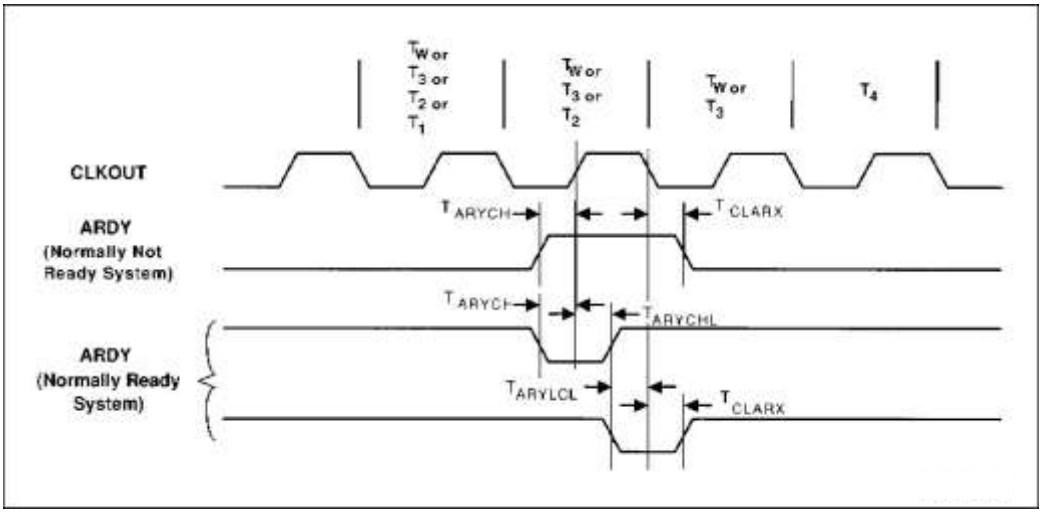


Figure 19. Asynchronous Ready (ARDY) Waveforms

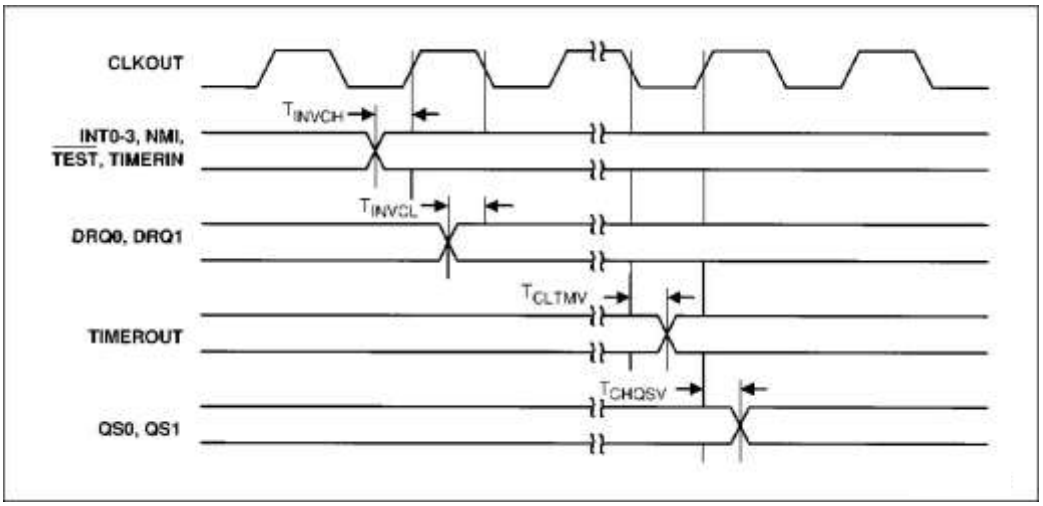


Figure 20. Peripheral and Queue Status Waveforms

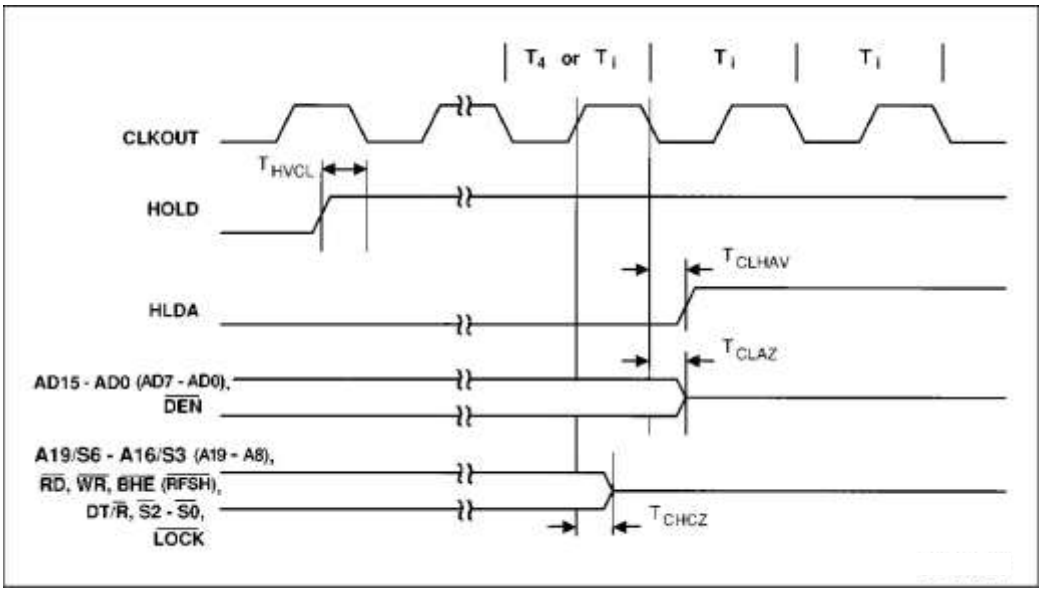


Figure 21. HOLDA/HLDA Waveforms (Entering Hold)

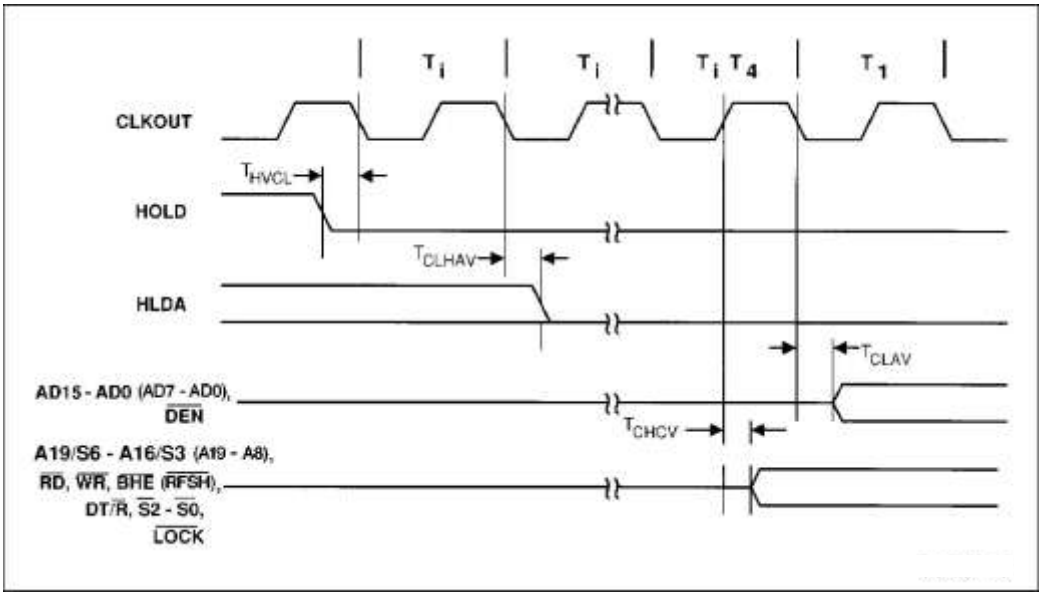


Figure 22. HOLD/HLDA Waveforms (Leaving Hold)

6. Instruction Execution Times

Table 20 provides IA186XL and IA188XL execution times, mnemonic instruction, and additional information on execution, if required.

Table 20. Instruction Set Timing

Instruction	Clock Cycles		Comments
	IA186XL	IA188XL	
AAA	3	3	–
AAD	6	6	–
AAM	40	40	–
AAS	3	3	–
ADC Immediate to accumulator	1	1	–
ADC Immediate to register/memory	3	13	–
ADC Register/memory with register to either	1/16	1/24	register/memory
ADD Immediate to accumulator	1	1	–
ADD Immediate to register/memory	1/19	1/32	register/memory
ADD Register/memory with register either	1/20	1/28	
AND Immediate to accumulator	1	1	–
AND Immediate to register/memory	1/24	1/33	register/memory
AND Register/memory and register to either	1/12	1/15	
BOUND	20/40	24/64	Interrupt not taken/Interrupt taken
CBW	1	4	–
CLC	1	1	–
CLD	1	1	–
CLI	1	1	–
CMC	2	2	–
CMPS	9	20	–
CS	1	1	–
CWD	1	1	–
DAA	4	4	–
DAS	2	2	–
DEC Register	1	1	–
DEC Register/memory	1/24	1/32	register/memory

Table 20. Instruction Set Timing *(Continued)*

Instruction	Clock Cycles		Comments
	IA186XL	IA188XL	
DIV Memory-Byte	46	46	–
DIV Memory-Word	49	51	–
DIV Register-Byte	39	39	–
DIV Register-Word	39	39	–
IDIV Memory-Byte	46	46	–
IDIV Memory-Word	49	51	–
IDIV Register-Byte	39	39	–
IDIV Register-Word	39	39	–
IMUL Immediate (signed)	5/24	5/33	register/memory
IMUL Memory-Byte	4	20	–
IMUL Memory-Word	13	28	–
IMUL Register-Byte	5	5	–
IMUL Register-Word	5	5	–
INC Register	1	1	–
INS	8	16	–
INS (repeated *n* times)	8+8*n*	16+16*n*	–
INT Type specified	33	41	–
INT Type 3	33	41	–
INTO	33	48	–
IRET	30	30	–
JA	3/5	3/5	Jump not taken/Jump taken
JAE	3/5	3/5	
JB	3/5	3/5	
JBE	3/5	3/5	
JCXZ	3/4	3/4	Jump not taken/Jump taken
JE	3/5	3/5	Jump not taken/Jump taken
JG	3/5	3/5	
JGE	3/5	3/5	
JL	3/5	3/5	
JLE	3/5	3/5	
JMP Direct intersegment	3	3	–
JMP Direct within segment	3	3	–
JMP Short/long	4	4	–
JNA	3/5	3/5	Jump not taken/Jump taken
JNAE	3/5	3/5	
JNB	3/5	3/5	
JNBE	3/5	3/5	
JNE	3/5	3/5	
JNG	3/5	3/5	
JNGE	3/5	3/5	
JNL	3/5	3/5	
JNLE	3/5	3/5	
JNO	3/5	3/5	
JNP	3/5	3/5	

Table 20. Instruction Set Timing *(Continued)*

Instruction	Clock Cycles		Comments
	IA186XL	IA188XL	
JNS	3/5	3/5	Jump not taken/Jump taken
JNZ	3/5	3/5	
JO	3/5	3/5	
JP	3/5	3/5	
JPE	3/5	3/5	
JPO	3/5	3/5	
JS	3/5	3/5	
JZ	3/5	3/5	
LAHF	2	2	–
LDS	1/24	1/33	register/memory
LEA	3	3	–
LEAVE	12	12	–
LES	12	32	–
LOCK	1	1	–
LODS	8	12	–
LODS (repeated *n* times)	8+8*n*	12+12*n*	–
LOOP	3/4	3/4	Loop not taken/Loop taken
LOOPE	3/4	3/4	Loop not taken/Loop taken
LOOPNE	3/4	3/4	
LOOPNZ	3/4	3/4	
LOOPZ	3/4	3/4	
MOV Accumulator to memory	5	8/12	8-bit/16-bit
MOV Immediate to register	1	1	-
MOV Immediate to register/memory	1/5	1/12	register/memory
MOV Memory to accumulator	5	8/12	8-bit/16-bit
MOV Register to Register/Memory	2/5	2/20	register/memory
MOV Register/memory to register	2/5	2/20	
MOV Register/memory to segment register	2/5	2/20	
MOV Segment register to register/memory	2/5	2/20	
MOVS	24	32	–
MOVS (repeated *n* times)	24+24*n*	32+32*n*	–
MUL Memory-Byte	16	20	–
MUL Memory-Word	15	25	–
MUL Register-Byte	5	5	–
MUL Register-Word	5	5	–
NEG	1/32	1/15	register/memory
NOP	1	1	–
NOT	1/24	1/24	register/memory
OR Immediate to accumulator	1	1	–

Table 20. Instruction Set Timing *(Continued)*

Instruction	Clock Cycles		Comments
	IA186XL	IA188XL	
OR Immediate to register/memory	1/32	1/32	register/memory
OR Register/memory and register to either	1/32	1/24	
OUT Fixed port	5	8/12	8-bit/16-bit
OUT Variable port	5	12	–
OUTS	8	12/20	8-bit/16-bit
OUTS (repeated *n* times)	8+8*n*	12/20+12/20*n*	8-bit/16-bit
POP Memory	10	20	–
POP Register	10	12	–
POP Segment register	16	12	–
POPA	80	93	–
POPF	13	13	–
PUSH Immediate	8	12	–
PUSH Memory	15	28	–
PUSH Register	4	12	–
PUSH Segment register	4	12	–
PUSHA	64	72	–
PUSHF	4	16	–
RET Inter-segment	14	21	–
RET Inter-segment adding immediate to SP	25	21	–
RET Within segment	14	13	–
RET Within segment adding immediate to SP	16	13	–
ROL Register/Memory by 1	1/8	1/16	register/memory
ROL Register/Memory by CL	1/8	1/16	
ROL Register/Memory by Count	1/8	1/24	
ROR Register/Memory by 1	1/8	1/16	
ROR Register/Memory by CL	1/8	1/16	
ROR Register/Memory by Count	1/8	1/24	
SAHF	2	2	–
SBB Immediate from accumulator	1	1	–
SBB Immediate from register/memory	1/15	1/28	register/memory
SBB Register/memory and register to either	1/11	1/40	register/memory
SCAS	11	8/12	8-bit/16-bit
SCAS (repeated *n* times)	11+8*n*	8/12+8/12*n*	8-bit/16-bit
SHL Register/Memory by 1	5	1/32	register/memory

Table 20. Instruction Set Timing *(Continued)*

Instruction	Clock Cycles		Comments
	IA186XL	IA188XL	
SHL Register/Memory by CL	1/20	1/24	register/memory
SHL Register/Memory by Count	1/11	1/24	
SHR Register/Memory by 1	1/5	1/24	
SHR Register/Memory by CL	1/20	1/28	
SHR Register/Memory by Count	1/11	1/24	
SS	1	1	–
STC	1	1	–
SUB Immediate from accumulator	1	1	-
SUB Immediate from register/memory	1/11	1/28	register/memory
SUB Register/memory and register to either	1/15	1/40	
STD	1	1	–
STI	1	1	–
STOS	6	8	–
STOS (repeated n times)	6+4n	8+8n	–
TEST Immediate data and accumulator	1	1	–
TEST Immediate data and register/memory	1/16	1/16	register/memory
TEST Register/memory and register	1/12	1/20	register/memory
WAIT	1	1	test_n = 0
XCHG Register with accumulator	2	2	–
XCHG Register/memory with register	3/16	3/20	register/memory
XLAT	16	8	–
XOR Immediate to accumulator	1	1	–
XOR Immediate to register/memory	1/11	1/32	register/memory
XOR Register/memory and register to either	1/16	1/32	register/memory

7. Innovasic Part Number Cross-Reference

Tables 21 through 23 cross-reference the Innovasic part number with the corresponding Intel part number.

Table 21. Innovasic Part Number Cross-Reference for the PLCC

Innovasic Part Number	Intel Part Number	Package Type	Temperature Range
IA186XLPLC68IR1 (lead free–RoHS)	N80C186XL25 N80C186XL20 N80C186XL12 TN80C186XL25 TN80C186XL20 TN80C186XL12 EE80C186XL25 EE80C186XL20 EE80C186XL12 EN80C186XL20 EN80C186XL12	68-Lead PLCC	Industrial
IA188XLPLC68IR1 (lead free–RoHS)	N80C188XL25 N80C188XL20 N80C188XL12 TN80C188XL25 TN80C188XL20 TN80C188XL12 EE80C188XL25 EE80C188XL20 EE80C188XL12 EN80C188XL20 EN80C188XL12	68-Lead PLCC	Industrial

Table 22. Innovasic Part Number Cross-Reference for the PQFP (Special Order only)

Innovasic Part Number	Intel Part Number	Package Type	Temperature Range
IA186XLPQF80IR1 (lead free–RoHS)	S80C186XL25 S80C186XL20 S80C186XL12 TS80C186XL25 TS80C186XL20 TS80C186XL12 EG80C186XL25 EG80C186XL20 ES80C186XL20	80-Lead PQFP	Industrial
IA188XLPQF80IR1 (lead free–RoHS)	S80C188XL25 S80C188XL20 S80C188XL12 TS80C188XL25 TS80C188XL20 TS80C188XL12 EG80C188XL25 EG80C188XL20 ES80C188XL20	80-Lead PQFP	Industrial

Table 23. Innovasic Part Number Cross-Reference for the LQFP (Special Order only)

Innovasic Part Number	Intel Part Number	Package Type	Temperature Range
IA186XLPLQ80IR1 (lead free–RoHS)	SB80C186XL25 SB80C186XL20 SB80C186XL12 YW80C186XL25 YW80C186XL20	80-Lead LQFP	Industrial
IA188XLPLQ80IR1 (lead free–RoHS)	SB80C188XL25 SB80C188XL20 SB80C188XL12 YW80C188XL25 YW80C188XL20	80-Lead LQFP	Industrial

8. Errata

The following errata are associated with the IA186XL/IA188XL. A workaround to the identified problem has been provided where possible.

8.1 Summary

Table 24 presents a summary of errata.

Table 24. Summary of Errata

Errata No.	Problem	Ver. 0	Ver. 1	Ver. 2
1	Pin LOCK_n does not have an internal pullup and will float during reset and bus hold.	Exists	Exists	Exists
2	When the timer compare register for any of the timers is set to x0000, the max count is xFFFF instead of x10000 as in the OEM part.	Exists	Fixed	Fixed
3	When using external interrupts IRQ0 or IRQ1 in Cascade Mode, the acknowledge signal on INTA0 or INTA1 may be lost or truncated.	Exists	Fixed	Fixed
4	Memory->Memory moves interrupted by two DMA cycles can corrupt data.	Exists	Fixed	Fixed
5	Bit 15 of RELREG (offset 0xFE) behaves differently than Intel device.	Exists	Fixed	Fixed
6	Enhanced mode makes bit 15 of RELREG (offset 0xFE) read-only.	Exists	Fixed	Fixed
7	Sbus deasserts on the wrong edge of CLKOUT.	Exists	Fixed	Fixed
8	Timer2 count register must be written to enable counting.	Exists	Exists	Fixed
9	Non-maskable interrupt (NMI) can be pre-empted by maskable interrupt.	Exists	Exists	Fixed
10	DMA can hang.	Exists	Exists	Fixed

Errata No.	Problem	Ver. 0	Ver. 1	Ver. 2
11	MOVS/POP/PUSH instructions interrupted by DMA can corrupt data.	Exists	Exists	Fixed
12	MOVS/POP/PUSH instructions interrupted by DMA can corrupt data.	Exists	Exists	Fixed

8.2 Detail

Errata No. 1

Problem: Pin LOCK_n does not have an internal pullup.

Description: Because Pin LOCK_n does not have an internal pullup, it will float during reset and bus hold.

Workaround: An external pullup may be necessary if there is high external load on the signal.

Errata No. 2

Problem:
When the timer compare register for any of the timers is set to x0000, the max count is xFFFF instead of x10000 as in the OEM part.

Description: The timer output will change one count earlier than it should when the max count is set to x0000.

Workaround: The workaround is application dependent. Please contact Innovasic Technical Support if this erratum is an issue.

Errata No. 3

Problem:
When using external interrupts IRQ0 or IRQ1 in Cascade Mode, the acknowledge signal on INTA0 or INTA1 may be lost or truncated.

Description: The acknowledge for IRQ0 or IRQ1 will be lost or truncated in Cascade Mode if another interrupt, with a higher priority setting (as configured in the interrupt control registers), occurs just before or during the acknowledge. This does not apply to interrupts generated by the DMA. This also does not apply when using the inherent priority settings (all interrupts configured with the same priority).

Workaround: When using external interrupts in cascade mode, do not program other interrupts to have a high priority (except DMAs). When using both IRQ0 and IRQ1 in Cascade Mode they must be programmed to have the same priority level.

Errata No. 4

Problem:
Memory->Memory moves interrupted by two DMA cycles can corrupt data.

Description:

This problem occurs if Memory->Memory operation is interrupted by
2 DMA cycles with the following sequence:

1. The instruction reads data from memory.
2. The first DMA cycle occurs.
3. The second DMA request occurs between 1 and 4 clocks after the falling edge of ALE for the deposit phase of the first DMA.
4. An instruction fetch occurs (this will be the data that shows up later).
5. The second DMA cycle occurs.
6. The write phase of the instruction happens with bad data (from step 4).

If the second DMA request occurs earlier than 1 clock after ALE for the first DMA's deposit phase, step 4 will be preempted by the second DMA, and operation is correct.

If the second DMA request occurs later than 4 clocks after ALE for the first DMA's deposit phase, the write phase will follow step 4 immediately, and operation is correct.

Of the total 163 instructions, the following 8 are impacted by this issue, with both the 8 & 16 bit versions of the first 7 on the list being affected.

1. MOVS
2. PUSH mem
3. POP mem
4. INS
5. IN
6. OUTS
7. OUT
8. ENTER

Workaround: If the conditions described above occur, there is no workaround. However, this DMA issue will be corrected in Revision 1 of the device.

Errata No. 5

Problem:
Bit 15 of RELREG (offset 0xFE) behaves differently than Intel device.

Description: For both 188 and 186 devices, an ESC opcode will generate a type 7 interrupt only when RELREG[15] is a 0.

Workaround: Initialize RELREG[15] to 0 if a type 7 interrupt is desired.

Errata No. 6

Problem:
Enhanced mode makes bit 15 of RELREG (offset 0xFE) read-only.

Description: If the device comes out of reset in enhanced mode, RELREG[15] will be set to a 1.

Workaround: Avoid enhanced mode if a type 7 interrupt is desired.

Errata No. 7

Problem:
Sbus deasserts on the wrong edge of CLKOUT.

Description: The sbus goes inactive (high) at the end of a bus cycle on the falling edge of CLKOUT. It should be on the rising edge of CLKOUT.

Workaround: None.

Errata No. 8

Problem:
Timer2 count register must be written to enable counting.

Description: If timer 2 count register is not explicitly written timer 2 will not count; this can also prevent timers 0 & 1 from counting if timer 2 is used as a prescaler.

Workaround: Write timer 2 count register before enabling timer 2.

Errata No. 9

Problem:
Non-maskable interrupt (NMI) can be pre-empted by maskable interrupt.

Description: When instruction execution unit is in Decode state for 2 or more consecutive cycles and an NMI is recognized, it could be pre-empted by a maskable interrupt.

Workaround: None.

Errata No. 10

Problem:
DMA can hang.

Description: DMA to a region of memory using destination synchronization and a chip select with extra wait states can hang.

Workaround: Do not use wait states and destination synchronization together.

Errata No. 11

Problem:
MOVS/POP/PUSH instructions interrupted by DMA can corrupt data.

Description: MOVS/POP/PUSH instructions interrupted by both a DMA transaction and an instruction fetch bus cycle can corrupt data. *This affects the IA186XL only.*

Workaround: None.

Errata No. 12

Problem:
MOVS/POP/PUSH instructions interrupted by DMA can corrupt data.

Description: MOVS/PUSH/POP instructions with 16-bit, non-aligned destination address interrupted by DMA can corrupt data. *This affects the IA186XL only.*

Workaround: None.

9. Data Sheet Revision History

Table 25 presents the sequence of revisions to document IA211080711.

Table 25. Data Sheet Revision History

Date	Revision	Description	Page(s)
September 30, 2008	00	Initial release	NA
August 5, 2009	01	Updated DC Parameters; Updated AC Specifications and timing diagrams; Updated Instruction Set Timing; Added errata.	Multiple pages throughout the document
August 19, 2009	02	Final version of the data sheet released to support production of Version 0 of the IA186/188 XL. Release date changed, "Preliminary" removed from heading and document number revised to reflect final release. No other changes.	Headers and Footers on all pages
September 4, 2009	03	Updated the package dimensions table for the 68 PLCC; Added a note to Table 12 regarding the Step ID register; Updated Errata 4 to include more recent information.	14, 46, 69, 71
January 15, 2010	04	Updated AC and DC table notes to show T_A at industrial temperature instead of commercial; Updated Errata information for Version 1of the device; Updated note regarding StepID register.	46, 47, 49, 51, 53, 55, 56, 57, 69
January 12, 2011	05	Updated to add Errata 8.	69, 72
January 13, 2011	06	Updated to add Errata 9 – 12.	69 - 73
March 23, 2011	07	Updated Instruction Set Timing Table to incorporate DIV and IDIV values.	62
June 30, 2011	08	Updated Errata table to note fixes in Ver. 2.	69, 70
July 6, 2011	09	Updated pin descriptions for inputs/outputs.	25, 28, 31, 32, 34

10. For Additional Information

The Innovasic Semiconductor IA186XL and IA188XL microcontrollers are form, fit, and function replacements for the original Intel 80C186XL and 80C188XL 16-bit high-integration embedded processors.

The Innovasic Support Team wants our information to be complete, accurate, useful, and easy to understand. Please feel free to contact our experts at Innovasic at any time with suggestions, comments, or questions.

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