SEEQ®
Technology, Incorporated

28C256A

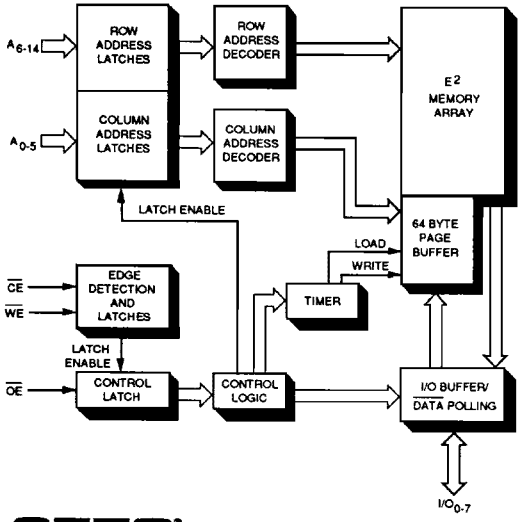
256K High Speed EEPROM

August 1992

FEATURES

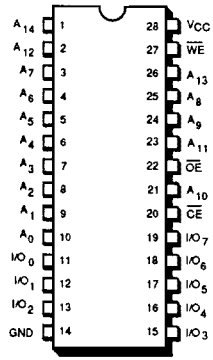
- **Military, Extended and Commercial Temperature Range**
  - –55° C to +125° C Operation (Military)
  - –40° C to +85° C Operation (Extended)
  - 0° C to +70° C Operation (Commercial)
- **High Speed**
  - 150 nsec Maximum Access Time
- **Low Power CMOS Technology**
  - 80 mA Active Current
  - 350 µA Standby Current
- **Fast Write Cycle Times**
  - 64 Byte Page Write Operation
  - 5 ms Typical Byte/Page Write Time
  - 80 µsec Average Byte Write Time
  - 3 ms byte/page Write Time Option Available
- **On-Chip Timer**
  - Automatic Erase before Write
- **End of Write Detection**
  - $\overline{DATA}$ Polling
  - Toggle Bit
- **Software Accessible Control Register**
  - Enable/Disable Software Protection Mode
  - 5VChip Erase
  - Disable Automatic Erase before Write
- **Data Protection**
  - Hardware: Power Up/Down Protection Circuitry
  - JEDEC Approved Software Write Protection
- **High Endurance**
  - 10,000 Cycles/Byte
  - 10 Year Data Retention
- **5V +/- 10% Power Supply**
- **CMOS & TTL Compatible I/O**
- **MIL - STD - 883 Class B Compliant 5962 SMD Compliant**

Block Diagram

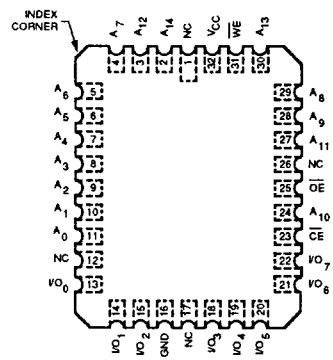


Pin Configuration

DUAL-IN-LINE, FLAT PACK TOP VIEW



LEADLESS CHIP CARRIER TOP VIEW



NOTE: The PLCC package has the same pin configuration as the LCC except pin 1 and pin 17 are don't connects

Pin Names

A_0-A_5	ADDRESSES – COLUMN
A_6-A_{14}	ADDRESSES – ROW
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
$\overline{WE}$	WRITE ENABLE
I/O_{0-7}	DATA INPUT (WRITE)/DATA OUTPUT (READ)

DESCRIPTION

The SEEQ 28C256A is a high performance 5V only, 32Kx8 Electrically Erasable Programmable Read Only Memory (EEPROM). It is manufactured using SEEQ's advanced 1.0 micron CMOS process and is available in most popular thru hole and surface mount package options as listed under "ordering Information." The 28C256A is ideal for high speed applications which require low power consumption, non-volatility, and in-system reprogrammability. The endurance, the number of times which a byte may be written, is specified at 10,000 cycles per byte minimum.

The 150 ns maximum access time meets or exceeds the requirements of most of today's high performance microprocessors. To allow the system designer maximum flexibility, the following features have been added to the device. The 28C256A has an internal timer which automatically times out the write time. The on-chip timer, along with the high speed input latches, frees the microprocessor for other tasks during the write time. The 28C256A's write cycle time is 5 msec typical. An automatic byte erase is performed before each byte/page write. The DATA Polling/Toggle Bit feature can be used to determine the end of a write cycle. A built-in control register allows a software controlled chip erase as well as the ability to disable the autoerase feature. This permits the user to effectively shorten the write time by half. Once the write cycle has been completed, data can be read in a maximum of 150 nsec. All inputs are CMOS/TTL for both write and read modes. Data retention is specified to be greater than 10 years.

DEVICE OPERATION

Operational Modes

There are five operational modes (see Table 1) and, except for the hardware chip erase mode, only CMOS/TTL inputs are required. A write cycle can only be initiated under the conditions shown. Any other conditions for $\overline{CE}$, $\overline{OE}$, and $\overline{WE}$ will inhibit writing and the I/O lines will either be in a high impedance state or have data, depending on the state of the aforementioned three input lines.

Table 1 Mode Selection

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Standby	V_{IH}	X	X	High Z
Write	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Write Inhibit	X	X	V_{IH}	High Z/D_{OUT}
	V_{IH}	X	X	High Z
	X	V_{IL}	X	High Z/D_{OUT}
	V_{IL}	V_{IL}	V_{IL}	No Operation (High Z)
Chip Erase	V_{IL}	V_H	V_{IL}	X

X: Any CMOS/TTL level
V_H: 12V ± 10%

Reads

A read is accomplished by presenting the addresses of the desired byte to the address inputs. Once the address is stable, $\overline{CE}$ is brought to a CMOS/TTL low in order to enable the chip. The $\overline{WE}$ pin must be at a CMOS/TTL high during the entire read cycle. The ouput drivers are made active by bringing output enable, $\overline{OE}$, to a CMOS/TTL low. During read, the addresses, $\overline{CE}$, $\overline{OE}$, and I/O latches are transparent.

Writes

To write into a particular location, addresses must be valid and a CMOS/TTL low is applied to the write enable, $\overline{WE}$, pin of a selected ($\overline{CE}$ low) device. This combined with the output enable, $\overline{OE}$, being high, initiates a write cycle. During a byte write cycle, all inputs except data are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever one occurred last. Write enable needs to be at a CMOS/TTL low only for the specified t_{WP} time. Data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever one occurred first. An automatic erase is performed before data is written. Automatic erase before write can be disabled to shorten the write cycle time.

The 28C256A can write both bytes or a page of up to 64 bytes. The write mode is discussed below.

Write Cycle Control Pins

For system design simplification, the 28C256A is designed such that either the $\overline{CE}$ or $\overline{WE}$ pin can be used to initiate a write cycle. The device uses the latest high-to-low transition of either $\overline{CE}$ or $\overline{WE}$ signal to latch addresses and the earliest low-to-high transition to latch the data. Address and $\overline{OE}$ set up and hold are with respect to the later of $\overline{CE}$ or $\overline{WE}$; data set up and hold is with respect to the earlier of $\overline{WE}$ or $\overline{CE}$.

To simplify the following discussion, the $\overline{WE}$ pin is used as the control pin throughout the rest of this document.

Write Mode

One to 64 bytes of data can be loaded randomly into the 28C256A. Addresses A6-A14 select the page address and must remain the same throughout the page load cycle. These addresses are latched on the falling edge of the $\overline{WE}$ signal (assuming $\overline{WE}$ controlled write cycle).

The column addresses, A0-A5, which are used to write into different locations of the page, are latched every time a

new write is initiated. These addresses along with $\overline{OE}$ state (high) are latched on the falling edge of $\overline{WE}$ signal. For proper write initiation and latching, the $\overline{WE}$ pin has to stay low for a minimum of t_{WP} ns. Data is latched on the rising edge of $\overline{WE}$, allowing easy microprocessor interface.

Upon a low to high $\overline{WE}$ transition, the 28C256A latches data and starts the internal page load timer. The timer is reset on the falling edge of $\overline{WE}$ signal if another write is initiated before the timer has timed out. The timer stays reset while the $\overline{WE}$ pin is kept low. If no additional write cycles have been initiated in (t_{BLC}) after the last $\overline{WE}$ low to high transition, the part terminates the page load cycle and starts the internal write. During this time, which takes a maximum of t_{WC} the device ignores any additional load attempts. The part can now be read to determine the end of write cycle ($\overline{DATA}$ Polling/Toggle Bit). A 80 µs average byte write time can be achieved if the page is fully utilized. The write time can be further optimized to 40 µs average by disabling automatic erase before write.

Extended Page Load

In order to take advantage of the page mode's faster average byte write time, data must be loaded within the page load cycle time ($t_{BLC\,max}$). Since some applications may not be able to sustain transfers at this minimum rate, the 28C256A permits an extended page load cycle. To do this, the write cycle must be "stretched" by maintaining $\overline{WE}$ low, assuming a write enable controlled cycle and leaving all other control inputs ($\overline{CE}$, $\overline{OE}$) in the proper page load cycle state. Since the page load timer is reset on the falling edge of $\overline{WE}$, keeping this signal low will prevent the page load cycle timer from beginning. In a $\overline{CE}$ controlled write the same is true, with $\overline{CE}$ holding the timer reset instead of $\overline{WE}$.

$\overline{DATA}$ Polling

I/O7 $\overline{DATA}$ Polling

The 28C256A has a maximum write cycle time of t_{WC}. However, a write will typically be completed in less than the specified maximum cycle time. $\overline{DATA}$ polling is a method of minimizing write times by determining the actual end point of a write cycle. If a read is performed to any address while the 28C256A is still writing, the device will present the ones-complement of data bit I/O7. When the 28C256A has completed its write cycle, a read from the last address written will result in valid data. Thus, software can simply read from the part until the last data byte written is read correctly. A $\overline{DATA}$ polling read should not be initiated until a minimum of t_{LP} nanoseconds after the last byte is written. $\overline{DATA}$ polling attempted during the middle of a page load cycle will present a ones-complement of the most recent data bit I/O7 loaded into the page. Timing for a $\overline{DATA}$ polling read is the same as a normal read once the t_{LP} specification has been met.

I/O6 Toggle Bit Polling

In addition to the polling method described above, the 28C256A provides I/O6 Toggle Bit to determine the end of the internal write cycle. While the internal write cycle is in progress, I/O6 toggles from 1 to 0 and 0 to 1 on sequential polling reads. When the internal write cycle is complete the toggling stops and the 28C256A is ready for additional read or write operations. This feature is particularly useful when writing to multiple devices simultaneously.

Hardware Chip Erase[1]

Certain applications may require all bytes to be erased simultaneously. This can be achieved by clearing one byte at a time, however, this would require a clock cycle for each byte or page clear. The high voltage chip erase function completes this task with a single clock cycle, thus reducing the total erase time considerably. Please refer to the Hardware Chip Erase waveforms for timing specifics.

Write Data Protection

Hardware Feature

There is internal circuitry to minimize a false write during Vcc power up or down. This circuitry prevents writing under any one of the following conditions:

1) V_{CC} is less than V_{WI}.
2) A high to low Write Enable ($\overline{WE}$) transition has not occurred when the V_{CC} supply is between V_{WI} and V_{CC} with $\overline{CE}$ low and $\overline{OE}$ high.

Writing will also be inhibited when $\overline{WE}$, $\overline{CE}$, or $\overline{OE}$ are in logical states other than that specified for a byte write in the Mode Selection Table.

Software Write Protect (SWP)

The 28C256A has the ability to enable and disable write operations under software control by accessing an internal control register. Software control of write operations can reduce the probability of inadvertant writes resulting from power up, power down, or momentary power disturbances. The 28C256A is shipped with the software write protect mode deactivated (default power-up mode) to provide compatibility with parts not having this mode. The software write protection mode is set by performing a page write operation (using page mode write timing) using specific addresses and data.

Set Software Write Protect

A three step write sequence shown below in TABLE 2 is used to set the protect mode. Page mode write timing is

Note: 1. Hardware chip clear is an optional feature and guaranteed on SMD product only.

to be used. A violation of this sequence or the time-out of the page timer (t_{BLC}) will abort the set protection mode (see note). Reads attempted during the access sequence will be assumed to be a $\overline{DATA}$ polling read and result in the device presenting a ones complement of the last data bit I/O7 written.

Protected Write Operation

Once the software protect mode is set, the software algorithm shown in TABLE 3 must be used for every byte write or page write cycle. The write operation uses the same three sequential steps shown in TABLE 2 to unlock the write protection for each byte/page write. The first three bytes unlock write protection while the fourth and successive bytes if any are written into the device.

Only single byte or page loads can be performed. After completion of internal write cycle, the device returns to the protected mode. The access sequence shown in TABLE 3 must be repeated to write an additional byte or page.

Disable Software Write Protection

The software protection can be disabled by following the six step sequence shown in TABLE 4. The device will be reconfigured to hardware protect mode only after this sequence. Page mode write timing is to be used. A violation of this sequence or the time-out of the page timer (t_{BLC}) will abort the reset protection mode. Reads attempted during the access sequence will be assumed to be $\overline{DATA}$ polling read.

SOFTWARE CONTROLLED SPECIAL FUNCTIONS

Chip erase and disable autoerase functions are accessed using the six step sequence shown in TABLES 5 & 6. The six step access sequence need not be followed by a non-volatile write cycle. The features are available for use both in the protected and unprotected (standard) modes. Page mode write timing is to be used. A violation of this sequence or the time-out of the page timer (t_{BLC}) will abort the access sequence and undesired writes could occur if the part is not software protected. Reads attempted during the access sequence will be assumed to be $\overline{DATA}$ polling read.

Software Chip Erase [1]

5 V only software chip erase is performed by executing the six step access sequence shown in TABLE 5. Control data word 10 hex should be written to the secondary control register. $\overline{DATA}$ polling can be done during chip erase to determine the completion of chip erase. The six step write need not be followed by a byte or page data load. At the end of the six step access sequence, the device begins and completes chip erase internally. Chip erase command can only be issued with the autoerase before write function enabled.

Disable Autoerase

This command disables the automatic erase before write cycle and is used typically after a chip erase operation to reduce the programming time of the device. The six step write sequence shown in TABLE 6 is used to perform the operation. Control data word 40 hex should be written to the secondary control register on the sixth step. At the end of the six step sequence autoerase before write is disabled for the current byte or page write sequence. At end of the internal byte or page write cycle automatic erase before write is re-enabled. Autoerase before write is always enabled on power-up/reset (default).

TABLE 2 Set Software Write Protect Operation Sequence

Step	Mode	Address A14-A0	Data I/O 7-0	Comment
1	Write	5555 Hex	AA Hex	Dummy write.
2	Write	2AAA Hex	55 Hex	Dummy write.
3	Write	5555 Hex	A0 Hex	Dummy write. SWP state activated.
4-67	Write	Address	Data	Write data to address. Byte or Page write.

NOTE: SWP protected state will be activated at the end of write even if a byte or page data load is NOT attempted after the three step access sequence. In such a case, after the three step access sequence AND t_{BLC} timeout, SWP bit is set by performing a non-volatile write cycle. The SWP non-volatile bit is set for protected mode operation during the first access sequence to the part. Once the SWP non-volatile bit is set, subsequent writes require the 3 step sequence to enable byte or page writes. Undesired writes could occur as a result of first access sequence violation while attempting to set SWP.

Note: 1. Software chip clear is an optional feature.

TABLE 3 Protected Mode Write Operation Sequence

Step	Mode	Address A14-A0	Data I/O 7-0	Comment
1	Write	5555 Hex	AA Hex	Dummy write.
2	Write	2AAA Hex	55 Hex	Dummy write.
3	Write	5555 Hex	A0 Hex	Dummy write. Enable byte/page writes.
4-67	Write	Address	Data	Write data to address. Byte or page write.

TABLE 4 Disable Protected Mode Operation Sequence

Step	Mode	Address A14-A0	Data I/O 7-0	Comment
1	Write	5555 Hex	AA Hex	Dummy write.
2	Write	2AAA Hex	55 Hex	Dummy write.
3	Write	5555 Hex	80 Hex	Dummy write.
4	Write	5555 Hex	AA Hex	Dummy write.
5	Write	2AAA Hex	55 Hex	Dummy write.
6	Write	5555 Hex	20 Hex	SWP state deactivated.
7-70	Write	Address	Data	Write data to address. Byte or Page Write.

NOTE: The SWP protected mode will be reset at the end of the write even if the six step access sequence is not followed by a byte or page data load. An internal non-volatile write cycle is performed to reset SWP bit after the six step access sequence AND t_{BLC} timeout.

TABLE 5 Chip Erase Operation Sequence

Step	Mode	Address A14-A0	Data I/O 7-0	Comment
1	Write	5555 Hex	AA Hex	Dummy write.
2	Write	2AAA Hex	55 Hex	Dummy write.
3	Write	5555 Hex	80 Hex	Dummy write register.
4	Write	5555 Hex	AA Hex	Dummy write.
5	Write	2AAA Hex	55 Hex	Dummy write.
6	Write	5555 Hex	10 Hex	Chip Erase

TABLE 6 Disable Autoerase Operation Sequence

Step	Mode	Address A14-A0	Data I/O 7-0	Comment
1	Write	5555 Hex	AA Hex	Dummy write.
2	Write	2AAA Hex	55 Hex	Dummy write.
3	Write	5555 Hex	80 Hex	Dummy write register.
4	Write	5555 Hex	AA Hex	Dummy write.
5	Write	2AAA Hex	55 Hex	Dummy write.
6	Write	5555 Hex	40 Hex	Disable Autoerase
7-70	Write	Address	Data	Load Page

Absolute Maximum Stress Range*

Temperature
Storage ..... –65°C to +150°C
Under Bias
Military / Extended ..... –65°C to +135°C
Commercial Temperature ..... –10°C to +80°C

D.C. Voltage applied to all Inputs or Outputs with respect to ground ..... +7.0 V to –3.0 V

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Recommended Operating Conditions

		28C256A - 150	28C256A - 200	28C256A - 250
Temperature Range	Commercial	0°C to +70°C	0°C to +70°C	0°C to +70°C
	Extended	–40°C to +85°C	–40°C to +85°C	–40°C to +85°C
	Military	–55°C to +125°C	–55°C to +125°C	–55°C to +125°C
Vcc Supply Voltage		5V ± 10%	5V ± 10%	5V ± 10%

Endurance and Data Retention

Symbol	Parameter	Value	Units	Condition
N	Minimum Endurance	10,000	Cycles/Byte	MIL-STD 883 Test Method 1033
T_{DR}	Data Retention	>10	Years	MIL-STD 883 Test Method 1008

DC Characteristics (Over operating temperature and V_{CC} range, unless otherwise specified)

Symbol	Parameter	Limits		Units	Test Condition
		Min.	Max.		
I_{CC}	Active V_{CC} Current		60	mA	$\overline{CE}$ = $\overline{OE}$ = V_{IL}: All I/O open; $\overline{WE}$ = V_{IH} Other Inputs = V_{CC} Max.
I_{SB1}	Standby V_{CC} Current (TTL Inputs)		3	mA	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL}; All I/O Open;
I_{SB2}	Standby V_{CC}Current (CMOS Inputs)		350	µA	$\overline{CE}$ = V_{CC} –0.3 Other Inputs = V_{IL} to V_{IH} All I/O Open
I_{IL}[1]	Input Leakage Current		1	µA	V_{IN} = V_{CC} Max.
I_{OL}[2]	Output Leakage Current		10	µA	V_{OUT} = V_{CC} Max.
V_{IL}	Input Low Voltage	–1.0	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} + 1.5	V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 6 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = –4 mA
V_{WI}	Write Inhibit Voltage	3.8		V	

NOTES:
1. Inputs only. Does not include I/O.
2. For I/O only.

Capacitance [1] T_A = 25°C, f = 1 MHz

Symbol	Parameter	Max.	Conditions
C_{IN}	Input Capacitance	6 pF	V_{IN} = OV
C_{OUT}	Data (I/O) Capacitance	12 pF	$V_{I/O}$ = OV

A.C. Test Conditions [2]

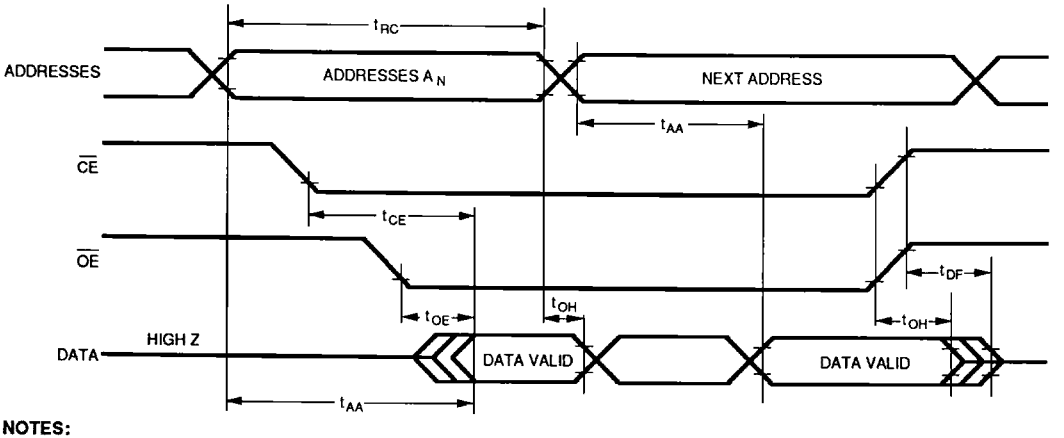
Output Load: 1 TTL gate and C_L = 100 pF
Input Rise and Fall Times: < 10 ns
Input Pulse Levels: 0.0 V to 3.0 V
Timing Measurement Reference Level: 1.5 V

AC Characteristics

Read Operation (Over operating temperature and V_{CC} range, unless otherwise specified)

Symbol	Parameter	Limits						Units	Test Conditions
		28C256A-150		28C256A-200		28C256A-250			
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{RC}	Read Cycle Time	150		200		250		ns	$\overline{CE}$ = $\overline{OE}$ =V_{IL}
t_{CE}	Chip Enable Access Time		150		200		250	ns	$\overline{OE}$ = V_{IL}
t_{AA}	Address Access Time		150		200		250	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
t_{OE}	Output Enable Access Time		35		35		35	ns	$\overline{CE}$ = V_{IL}
t_{DF}	Output or Chip Enable High to output in Hi-Z	0	35	0	35	0	35	ns	$\overline{CE}$ = V_{IL}
t_{OH}	Output Hold from Address Change, Chip Enable, or Output Enable, whichever occurs first	0		0		0		ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}

Read /$\overline{DATA}$ Polling Cycle



NOTES:
1. This parameter is measured only for the initial qualification and after process or design changes which may affect it.
2. Military compliant product tested per applicable military specification.

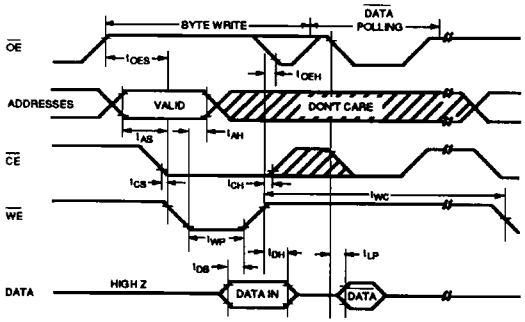
AC Characteristics

Write Operation (Over the operating temperature and V_{CC} range, unless otherwise specified)

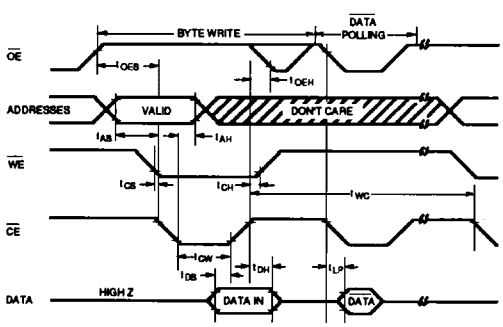
Symbol	Parameter	Limits						Units
		28C256A-150		28C256A-200		28C256A-250		
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{WC}	Write Cycle Time 28C256A		10		10		10	ms
	28C256AH		3		3		3	ms
t_{AS}	Address Set-up Time	0		0		0		ns
t_{AH}	Address Hold Time (see note 1)	50		50		50		ns
t_{CS}	Write Set-up Time	0		0		0		ns
t_{CH}	Write Hold Time	0		0		0		ns
t_{CW}	$\overline{CE}$ Pulse Width (note 2)	50		50		50		ns
t_{OES}	$\overline{OE}$ High Set-up Time	0		0		0		ns
t_{OEH}	$\overline{OE}$ High Hold Time	0		0		0		ns
t_{WP}	$\overline{WE}$ Pulse Width (note 2)	50		50		50		ns
t_{DS}	Data Set-up Time	40		40		40		ns
t_{DH}	Data Hold Time	0		0		0		ns
t_{BLC}	Byte Load Timer Cycle (Page Mode Only) (note 3)	0.2	150	0.2	150	0.2	150	µs
t_{LP}	Last Byte Loaded to $\overline{DATA}$ Polling Output		150		200		200	ns

Byte Write Timing

$\overline{WE}$ CONTROLLED WRITE CYCLE



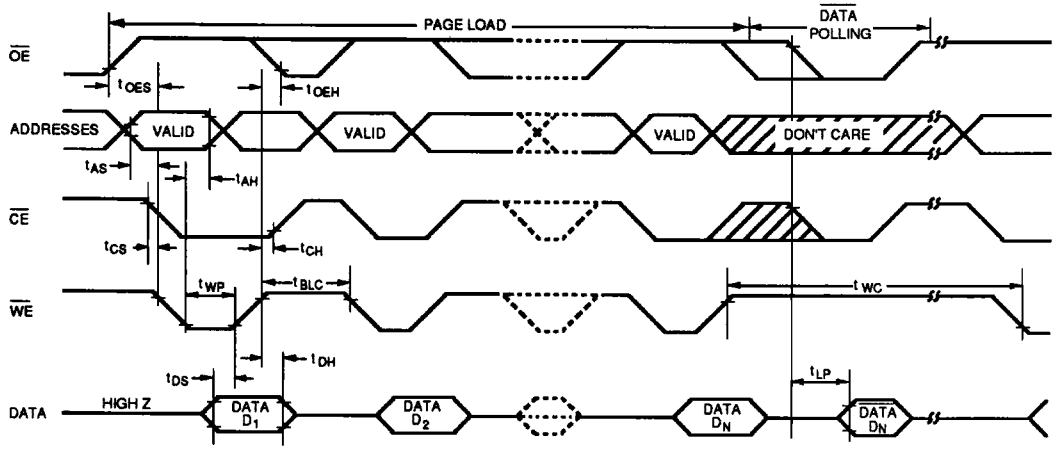
$\overline{CE}$ CONTROLLED WRITE CYCLE



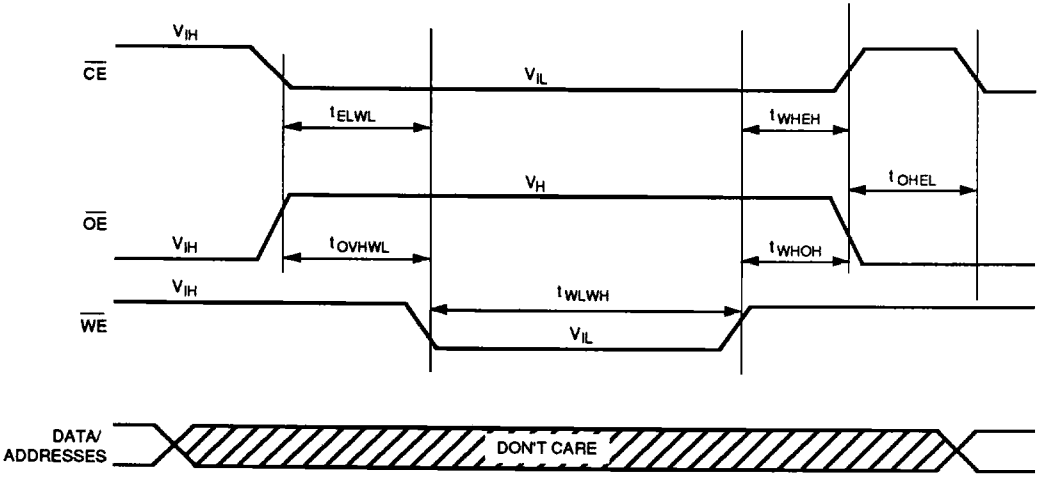
NOTES:

1. Address hold time is with respect to the falling edge of the control signal $\overline{WE}$ or $\overline{CE}$.
2. $\overline{WE}$ and $\overline{CE}$ are noise protected. Less than a 10 nsec write pulse will not activate a write cycle.
3. t_{BLC} min. is the minimum time before the next byte can be loaded. t_{BLC} max. is the minimum time the byte load timer waits before initiating internal write cycle.

Page Write Timing/$\overline{WE}$ Controlled



Hardware Chip Erase



Hardware Chip Erase

Parameter	Description	Min.	Max.	Units
t_{ELWL}	Chip Enable Setup Time	5		µs
t_{OVHWL}	Output Enable Setup Time	5		µs
t_{WLWH}	Write Enable Pulse Width	10		ms
t_{WHEH}	Chip Enable Hold Time	5		µs
t_{WHOH}	Output Enable Hold Time	5		µs
t_{OHEL}	Erase Recovery Time		50	ms
V_H	High Voltage	10.8	13.2	V

Ordering Information