Signetics

FAST 74F1762
Memory Address Multiplexer

Product Specification

Fast Products

FEATURES

- **Provides refresh and multiplexed row and column addresses for DRAMs**
- **Addressing up to 4MBit DRAMs**
- **Compatible with 74F1761 DIVC and other DRAM controllers**
- **High-performance outputs**
- **High-speed address multiplexing**
- **On-chip 11-bit refresh counter**

TYPE	TYPICAL DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
N74F1762	5.3ns	90mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
Plastic DIP	N74F1762N
PLCC 44	N74F1762A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L) HIGH/LOW	LOAD VALUE HIGH/LOW
RA_0 - RA_{10}	Row address inputs	1.0/1.0	20µA/0.6mA
CA_0 - CA_{10}	Column address inputs	1.0/1.0	20µA/0.6mA
$\overline{MA}_0$ - $\overline{MA}_{10}$	DRAM address outputs	N/A	15mA/20mA
$\overline{REFEN}$	Refresh enable input	1.0/1.0	20µA/0.6mA
MUX	Row/column select input	1.0/1.0	20µA/0.6mA
COUNT	Refresh address count input	1.0/1.0	20µA/0.6mA
MR	Refresh counter reset input	1.0/1.0	20µA/0.6mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state. FAST Unit Loads do not correspond to DRAM Input Loads. See Functional Description for details.

PRODUCT DESCRIPTION:

The Signetics Memory Address Multiplexer is designed for use in very high performance dynamic RAM applications. In addition to multiplexing row and column addresses, the device also generates and multiplexes refresh addresses. Though specifically designed to be used with the 74F1761, DRAM and Interrupt Vector Controller, it may be used with any other custom or standard DRAM timing controller chip.

The 'F1762 contains 22 address inputs (RA_0 - RA_{10}) and (CA_0 - CA_{10}), an 11-bit refresh counter, and eleven 3-to-1 multiplexers. The multiplexed row, column or refresh address is output on the eleven high-performance outputs ($\overline{MA}_0$ - $\overline{MA}_{10}$). This enables direct addressing of up to 4MBit dynamic RAMs. Combined with the 'F1761, the 'F1762 provides a complete 4MBit DRAM and interrupt control solution. This solution can control dynamic RAMs with access times down to 40ns.

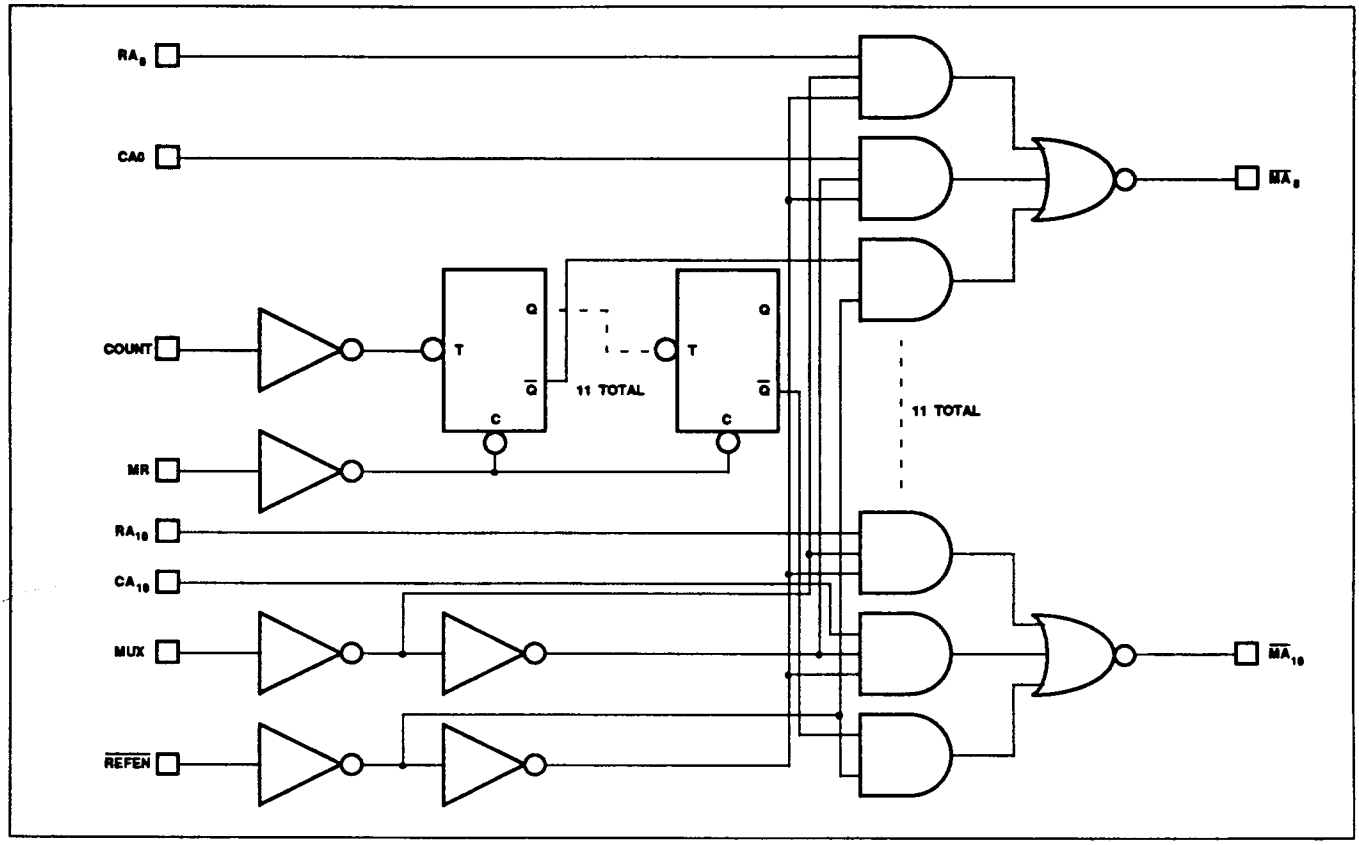
FUNCTIONAL DESCRIPTION:

Functionally, the 'F1762 Memory Address Multiplexer is quite simple. Referring to the logic diagram, the 11-bit Refresh Counter is controlled by the COUNT input, which increments the value stored in the refresh counter on every Low to High transition. When the 'F1762 is used with the 'F1761, this pin is usually connected to the $\overline{REFEN}$ input, so that at the end of every refresh cycle, the refresh counter will be incremented. The Master Reset (MR) input clears the contents of the refresh counter, and may be used for diagnostic testing or initializing after power-up. The eleven 3-to-1 multiplexers are controlled by the MUX and $\overline{REFEN}$ inputs. When $\overline{REFEN}$ is asserted, regardless of the state of the MUX signal, the contents of the internal refresh counter are inverted and asserted at the $\overline{MA}_0$ - $\overline{MA}_{10}$ outputs. When $\overline{REFEN}$ is negated, the MUX signal controls which set of address inputs will be propagated to the outputs. With MUX Low, the Row Address inputs (RA_0 - RA_{10}) will be inverted and asserted at the $\overline{MA}_0$ - $\overline{MA}_{10}$ outputs. When MUX is High, the Column Addresses (CA_0 - CA_{10}) will be correspondingly asserted.

The $\overline{MA}_0$ - $\overline{MA}_{10}$ outputs have specialized drivers to switch 70 ohm transmission lines (typical of DRAM arrays) on the incident edge, thus improving overall system performance. For more information on the driving characteristics, please refer to the DC electrical characteristics and also Signetics application note number AN218.

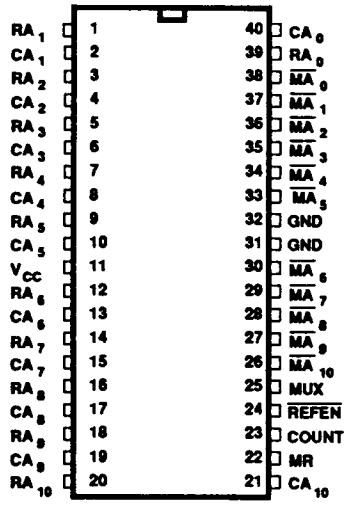
Memory Address Multiplexer | FAST 74F1762

LOGIC DIAGRAM

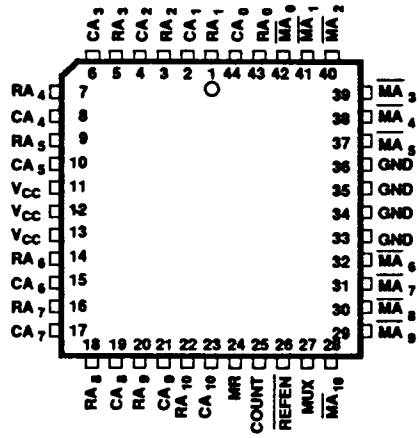


PIN CONFIGURATION

N Package



A Package



PIN DESCRIPTION

SYMBOL	PINS		TYPE	NAME AND FUNCTION
	DIP	PLCC		
RA_0 - RA_{10}	39, 1, 3, 5, 7, 9, 12, 14, 16, 18, 20	43, 1, 3, 5, 7, 9, 14, 16, 18, 20, 22	I	Row Address Inputs. When $\overline{REFEN}$ is negated and MUX is Low, these inputs are inverted and propogated to the $\overline{MA}_0$ - $\overline{MA}_{10}$ outputs.
CA_0 - CA_{10}	40, 2, 4, 6, 8, 10, 13, 15, 17, 19, 21	44, 2, 4, 6, 8, 10, 15, 17, 19, 21, 23	I	Column Address Inputs. When $\overline{REFEN}$ is negated and MUX is High, these inputs are inverted and propogated to the $\overline{MA}_0$ - $\overline{MA}_{10}$ outputs.
$\overline{MA}_0$ - $\overline{MA}_{10}$	38, 37, 36, 35, 34, 33, 30, 29, 28, 27, 26	42, 41, 40, 39, 38, 37, 32, 31, 30, 29, 28	O	Active Low Memory Address Outputs. These outputs contain the address from either the internal refresh counter, the Row Address inputs, or the Column Address inputs depending on the state of the $\overline{REFEN}$ and MUX signal inputs.
$\overline{REFEN}$	24	26	I	Active Low Refresh Enable Input. When asserted, the address contained in the internal refresh counter is asserted on the $\overline{MA}_0$ - $\overline{MA}_{10}$ outputs.
MUX	25	27	I	Row / Column Address Multiplex Input. If $\overline{REFEN}$ is High, this signal will multiplex the inverted Row or Column address inputs on the $\overline{MA}_0$ - $\overline{MA}_{10}$ outputs when it is asserted Low or High respectively.
COUNT	23	25	I	Refresh Counter Count Clock Input. A Low to High transition on this input will increment the internal refresh counter by one regardless of the state of $\overline{REFEN}$ input.
MR	22	24	I	Active High Refresh Counter Master Reset Input. A High level on this input will reset the internal refresh counter to all zeros.
V_{CC}	11	11, 12, 13		+5V ± 10% Supply input.
GND	31, 32	33, 34, 35, 36		Ground.

FUNCTION TABLE

INPUTS						OUTPUTS	COUNTER
MR	COUNT	MUX	$\overline{REFEN}$	RA_n	CA_n	$\overline{MA}_n$	COUNTER CONTENTS
H	X	X	X	X	X	UN*	Reset to 0
L	↑	X	X	X	X	UN*	Increment by 1
H	X	X	L	X	X	L	Reset to 0
L	X	X	L	X	X	COUNTER CONTENTS	Unchanged
L	X	L	H	L	X	H	Unchanged
L	X	L	H	H	X	L	Unchanged
L	X	H	H	X	L	H	Unchanged
L	X	H	H	X	H	L	Unchanged

*The state of the outputs is dependant on the state of the MUX and $\overline{REFEN}$ inputs. The Counter is reset any time MR is High, and if MR is Low, it is incremented on every low to high transistion of COUNT.

UN = Unspecified

H = High level voltage

L = Low level voltage

X = Don't care

↑ = Low-to-High transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	120	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-15	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

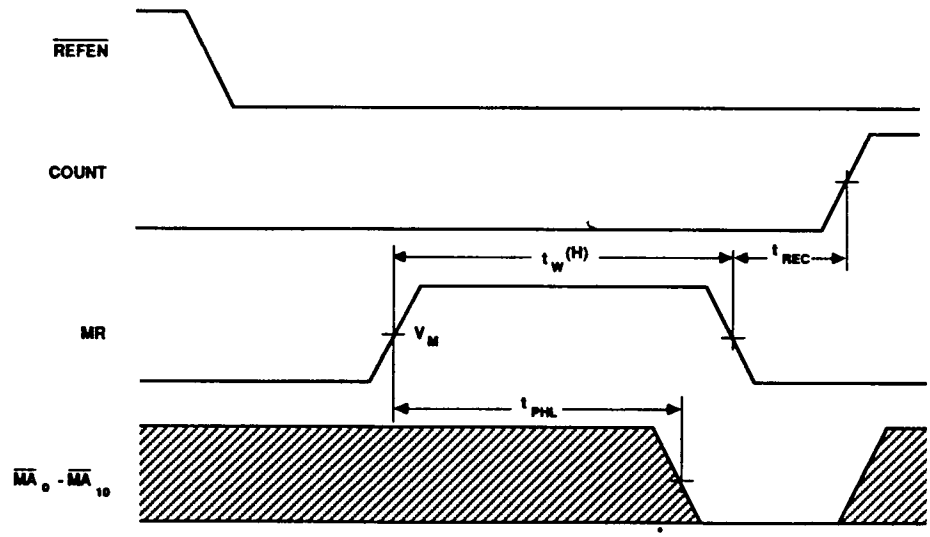
SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage[3]		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = -15mA	±10%V_{CC}	2.5	3.2		V
					±5%V_{CC}	2.7	3.4		V
				I_{OH2} = -35mA	±5%V_{CC}	2.4			V
V_{OL}	Low-level output voltage[4]		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 24mA	±10%V_{CC}		0.35	0.5	V
					±5%V_{CC}		0.35	0.5	V
				I_{OL2} = 60mA	±5%V_{CC}		0.45	0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Low-level output voltage		V_{CC} = 0.0V, V_I = 7.0V					100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					-0.6	mA
I_{IO}[5]	Output current		V_{CC} = MAX, V_{OUT} = 2.25V			-30		-120	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				55	80	mA
		I_{CCL}					90	120	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OH2} is the current necessary to guarantee a Low-to-High transition in a 70Ω transmission line.
4. I_{OL2} is the current necessary to guarantee a High-to-Low transition in a 70Ω transmission line.
5. The output conditions have been chosen to produce a current that closely approximates one-half of the short circuit current, I_{OS}.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 300pF, R_L = 70Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 300pF, R_L = 70Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay, MUX(↑) to $\overline{MA}_0$ - $\overline{MA}_{10}$, (column address) valid	Waveform 1	2.0 2.5	4.5 5.0	7.5 8.0	2.0 2.5	8.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay, MUX(↓) to $\overline{MA}_0$ - $\overline{MA}_{10}$, (row address) valid	Waveform 3	4.0 2.0	6.5 4.5	9.5 7.5	3.0 2.0	10.5 7.5	ns
t_{PLH} t_{PHL}	Propagation delay, $\overline{REFEN}$ (↑) to $\overline{MA}_0$ - $\overline{MA}_{10}$		2.0 2.0	4.3 4.5	7.5 8.0	2.0 2.0	8.5 11.0	ns
t_{PLH} t_{PHL}	$\overline{REFEN}$ (↓) to $\overline{MA}_0$ - $\overline{MA}_{10}$ (refresh address) valid	Waveform 2	4.0 2.0	6.9 4.7	10.5 7.5	3.5 2.0	11.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay, RA_0 - RA_{10} to $\overline{MA}_0$ - $\overline{MA}_{10}$	Waveform 4	1.0 0.5	3.0 2.2	6.0 5.0	1.0 0.5	6.5 5.5	ns
t_{PLH} t_{PHL}	Propagation delay, CA_0 - CA_{10} to $\overline{MA}_0$ - $\overline{MA}_{10}$	Waveform 5	1.0 0.5	3.0 2.2	6.0 5.0	1.0 0.5	6.5 5.5	ns
t_{PLH} t_{PHL}	COUNT (↑) to $\overline{MA}_0$ - $\overline{MA}_{10}$ (refresh address) valid	Waveform 2	2.0	15.0	35.0	2.0	40.0	ns
t_{PHL}	Propagation delay, MR(↑) to $\overline{MA}_0$ - $\overline{MA}_{10}$	Waveform 1	3.0	5.8	10.5	2.5	11.0	ns
t_w(H)	COUNT pulse width, High	Waveform 2	5.0			5.0		ns
t_w(L)	COUNT pulse width, Low	Waveform 2	5.0			5.0		ns
t_w(H)	MR Pulse width	Waveform 1	5.0			5.0		ns
t_{rec}	Recovery time, MR (↓) to COUNT (↑)	Waveform 1	5.0			5.0		ns

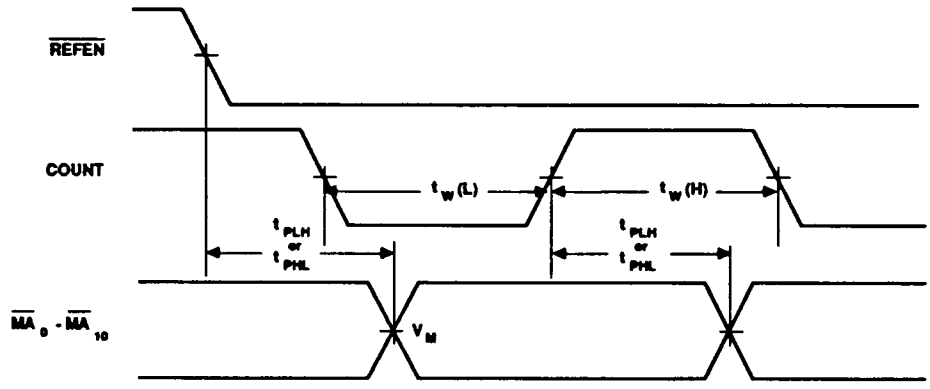
AC WAVEFORMS



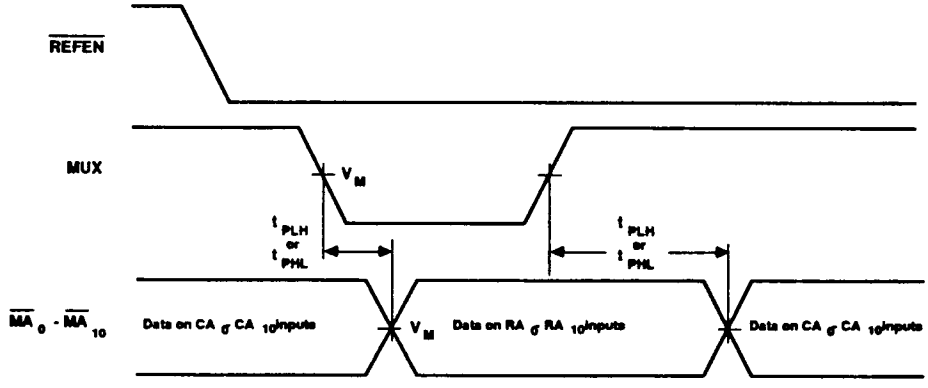
Waveform 1. Waveforms Showing Master Reset Timing

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

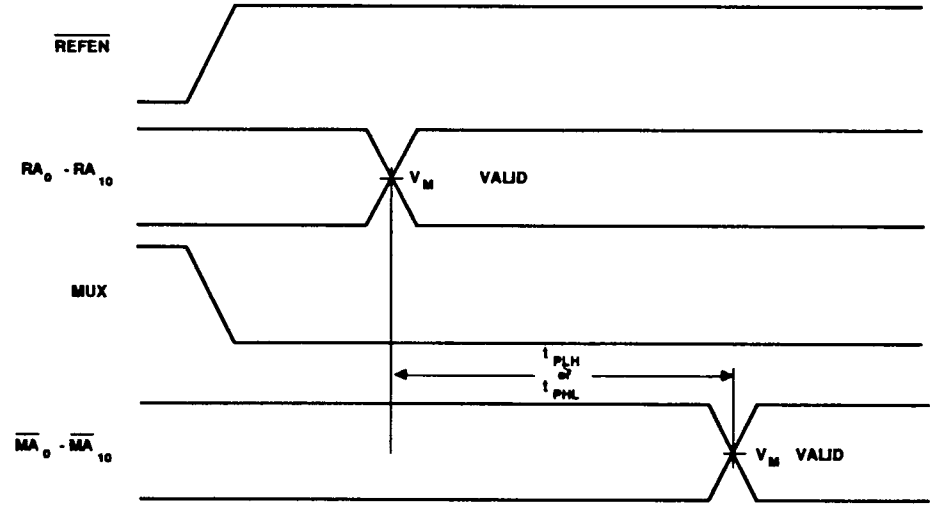
AC WAVEFORMS



Waveform 2. Waveforms Showing Refresh Timing



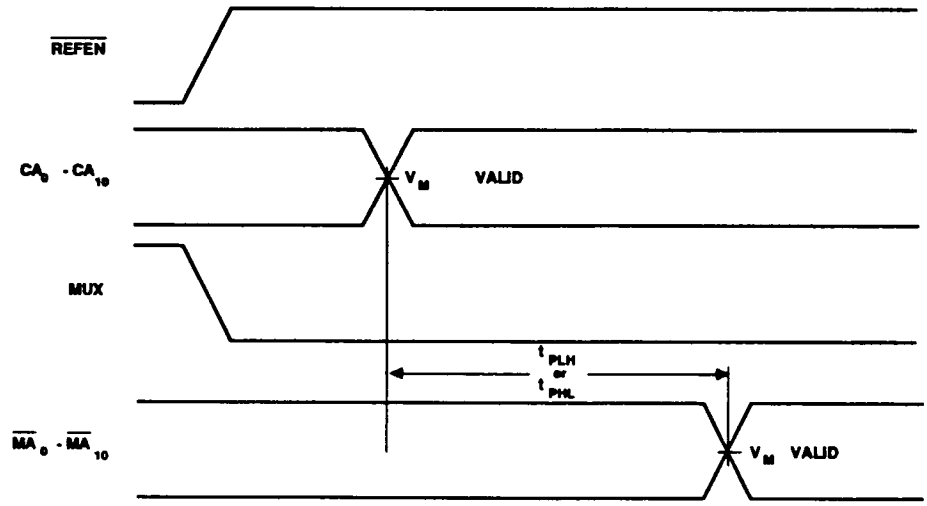
Waveform 3. Waveforms Showing Address Multiplexing Timing



Waveform 4. Waveforms Showing RA_0 - RA_{10} to $\underline{MA}_0$ - to $\underline{MA}_{10}$ Propagation Delay

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

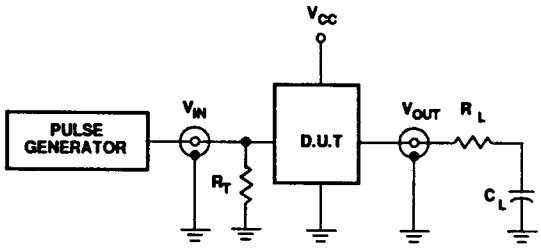
AC WAVEFORMS



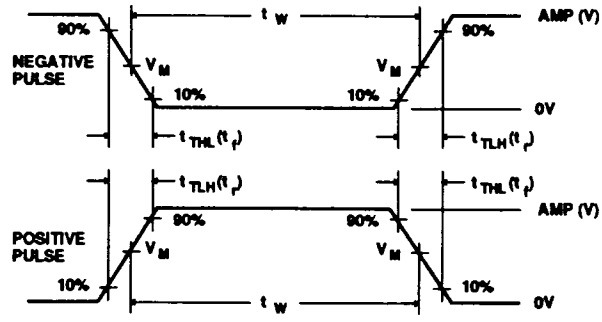
Waveform 5. Waveforms Showing CA0 - CA10 to $\overline{MA}_0$ - $\overline{MA}_{10}$ Propagation Delay

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.