Integrated Device Technology, Inc.

1024K x 1 CMOS STATIC RAM MODULE

IDT7MC4001

FEATURES:

- High-density separate I/O, 1 megabit CMOS static RAM module
- Fast access times: 35ns (max.)
- Surface mounted LCC components mounted on a co-fired ceramic substrate
- Available in low profile 30-pin ceramic SIP (Single In-line Package)
- Low power consumption
- Single 5V(±10%) power supply
- Inputs and outputs directly TTL-compatible

DESCRIPTION:

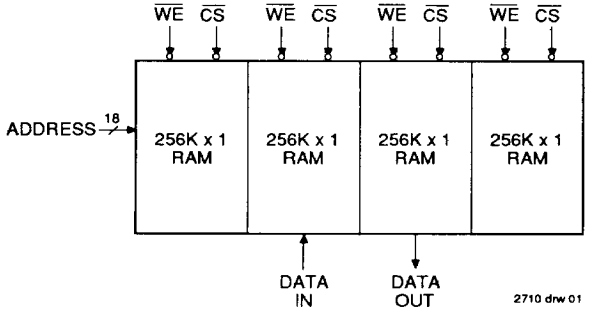
The IDT7MC4001 is a 1024K x 1 high-speed static RAM module with separate I/O. The module is constructed on a co-fired ceramic substrate using four 256K x 1 static RAMs in surface mount packages. Extremely fast speeds can be achieved by using RAMs fabricated in IDT's high-performance, high-reliability CEMOS™ technology.

The IDT7MC family of ceramic SIPs offers the optimum in packing density and profile height. The IDT7MC4001 is offered in a 30-pin ceramic SIP (Single In-line Package). At only 420 mils high, this low profile package is ideal for systems with minimal board spacing.

The IDT7MC4001 is available with maximum access times as fast as 35ns, with maximum power consumption of 1.35 watts. The module also offers a full standby mode of 330mW (max.).

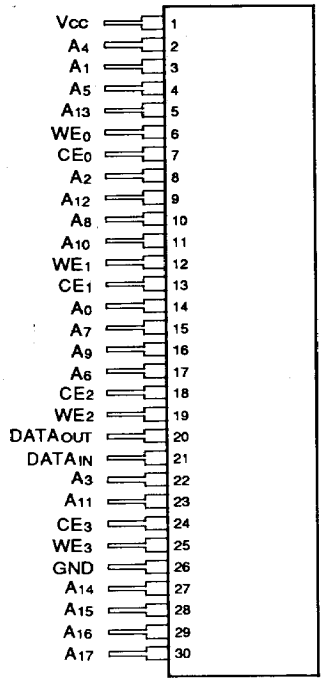
All inputs and outputs of the IDT7MC4001 are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation.

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATION[1]



2710 drw 02

SIP
FRONT VIEW

NOTE:
1. For module dimensions, please refer to module drawing M35 in the packaging section.

PIN NAMES

A0–A17	Address
DATAIN	Data Input
DATAOUT	Data Output
$\overline{CS}_{0-3}$	Chip Select
$\overline{WE}_{0-3}$	Write Enable
Vcc	Power
GND	Ground

2710 tbl 01

TRUTH TABLE

Mode	$\overline{CS}$	$\overline{WE}$	Output	Power
Standby	H	X	HighZ	Standby
Read	L	H	DOUT	Active
Write	L	L	High Z	Active

2710 tbl 02

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Value	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	°C
TBIAS	TemperatureUnder Bias	-55 to +125	°C
TSTG	Storage Temperature	-55 to +125	°C
IOUT	DC Output Current	50	mA

2710 tbl 03

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE[1] (TA = +25°C, f = 1.0MHz)

Symbol	Test	Conditions	Typ.	Unit
CIN	Input Capacitance	VIN = 0V	35	pF
COUT	Output Capacitance	VOUT = 0V	20	pF

2710 tbl 04

NOTE:
1. This parameter is guaranteed by design but not tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6.0	V
VIL	Input Low Voltage	-0.5[1]	—	0.8	V

2710 tbl 05

NOTE:
1. VIL = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 10%

2710 tbl 06

8

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	20	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	20	µA
I_{CC1}	Operating Power Supply Current	f = 0, $\overline{CS}$ = V_{IL}, V_{CC} = Max., Output Open	—	225	mA
I_{CC2}	Dynamic Operating Current	V_{CC} = Max., $\overline{CS}$ = V_{IL}, f = f_{MAX}, Output Open	—	245	mA
I_{SB}	Standby Power Supply Current	$\overline{CS}$ ≥ V_{IH} or TTL Level, V_{CC} = Max., f=f_{MAX}, Output Open	—	180	mA
I_{SB1}	Full Standby Power Supply Current	$\overline{CS}$ ≥ V_{HC}, V_{IN} ≥ V_{HC} or ≤ V_{LC} V_{CS} = Max., Output Open	—	60	mA
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8mA	—	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -4mA	2.4	—	V

2710 tbl 07

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2710 tbl 08

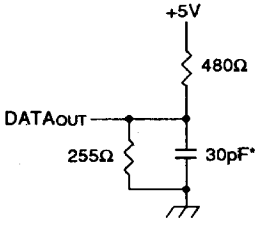


Figure 1. Output Load

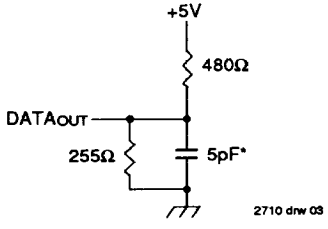


Figure 2. Output Load (for t_{CLZ}, t_{CHZ}, t_{OW}, and t_{WHZ})

*Including scope and jig.

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C)

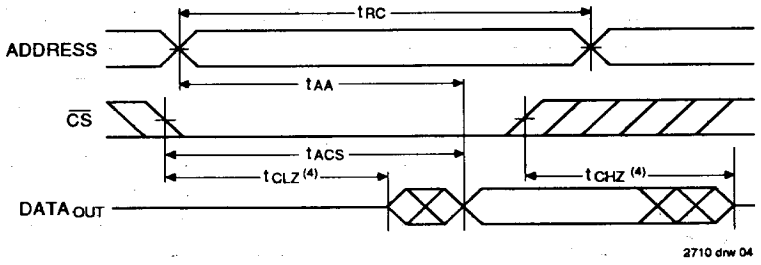
Symbol	Parameters	IDT7MC4001S35		IDT7MC4001S45		IDT7MC4001S55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t_{RC}	Read Cycle Time	35	—	45	—	55	—	ns
t_{AA}	Address Access Time	—	35	—	45	—	55	ns
t_{ACS}	Chip Select Access Time	—	35	—	45	—	55	ns
t_{CLZ}[1]	Chip Select to Output in Low Z	10	—	10	—	10	—	ns
t_{CHZ}[1]	Chip Deselect to Output in High Z	—	25	—	35	—	45	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	ns
t_{PU}[1]	Chip Select to Power Up Time	0	—	0	—	0	—	ns
t_{PD}[1]	Chip Deselect to Power Down Time	—	35	—	45	—	55	ns
Write Cycle								
t_{WC}	Write Cycle Time	35	—	45	—	55	—	ns
t_{CW}	Chip Selection to End of Write	30	—	40	—	50	—	ns
t_{AW}	Address Valid to End of Write	30	—	40	—	50	—	ns
t_{AS}	Address Set-up Time	5	—	5	—	5	—	ns
t_{WP}	Write Pulse Width	25	—	35	—	45	—	ns
t_{WR}	Write Recovery Time	5	—	5	—	5	—	ns
t_{WHZ}[1]	Write Enable to Ouput in High Z	—	25	—	30	—	40	ns
t_{DW}	Data Valid to End of Write	20	—	25	—	35	—	ns
t_{DH}	Data Hold from Write Time	5	—	5	—	5	—	ns
t_{OW}[1]	Output Active from End of Write	5	—	5	—	5	—	ns

2710 tbl 09

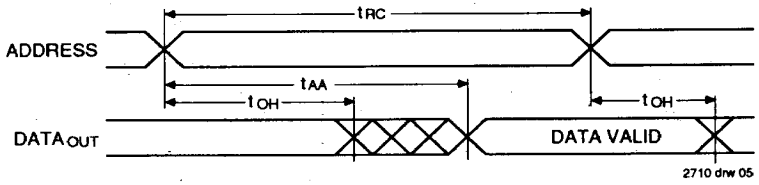
NOTE:
1. This parameter is guaranteed by design but not tested.

8

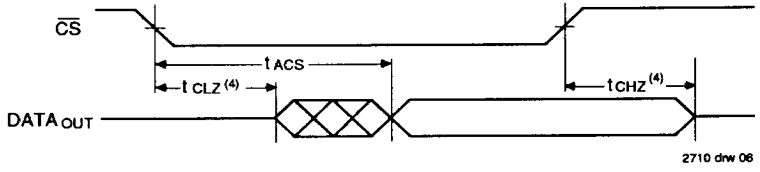
TIMING WAVEFORM OF READ CYCLE NO. 1(1)



TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2)

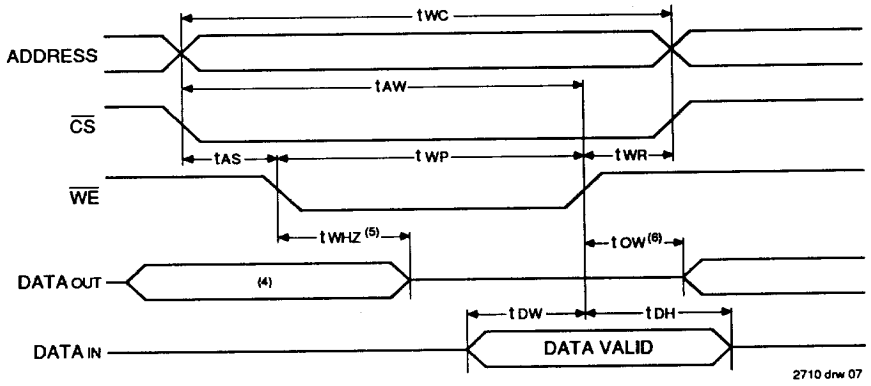


TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3)

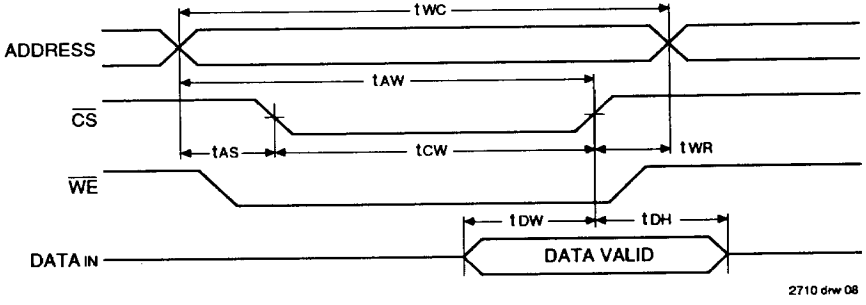


NOTES:
1. $\overline{WE}$ is high for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = VIL.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. Transition is measured ±200mV from steady state. This parameter is guaranteed by design but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 3, 7)



TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 3, 5)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (tWP) of a low $\overline{CS}$and a low $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going High to the end of write cycle.
4. During this period, I/O pins are in the output state and inputs signals must not be applied.
5. If the $\overline{CS}$ Low transition occurs simultaneously with or after the $\overline{WE}$ Low transitions, the outputs remain in a high impedance state.
6. Transition is measured ±500mV from steady state. This parameter is graranteed by design, but not tested.

8

ORDERING INFORMATION