TISP3070H3SLL, TISP3250H3SLL, TISP3290H3SLL

DUAL BIDIRECTIONAL THYRISTOR OVERVOLTAGE PROTECTORS

TISP3xxxH3SLL Overvoltage Protector Series

ITU-T K.20/21 Rating .....8 kV 10/700, 200 A 5/310

Low Differential Capacitance .....< 67 pF

3-Pin Through-Hole Packaging
- Compatible with TO-220AB pin-out

Ion-Implanted Breakdown Region
- Precise and Stable Voltage

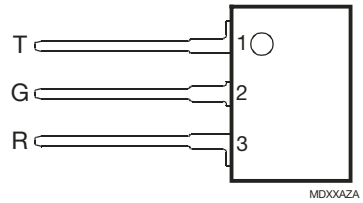
Low Voltage Overshoot Under Surge

Device Name	V_{DRM} V	$V_{(BO)}$ V
TISP3070H3SLL	58	70
TISP3250H3SLL	190	250
TISP3290H3SLL	220	290

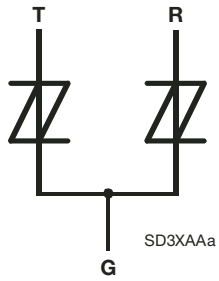
Rated for International Surge Wave Shapes
- Single and Simultaneous Impulses

Wave Shape	Standard	I_{PPSM} A
2/10	GR-1089-CORE	500
8/20	IEC 61000-4-5	300
10/160	TIA-968-A	250
10/700	TIA-968-A ITU-T K.20/21	200
10/560	TIA-968-A	160
10/1000	GR-1089-CORE	100

3-SIP (Long Lead) Package (Top View)



Device Symbol



.....UL Recognized Component

Description

The TISP3xxxH3SLL limits overvoltages between the telephone line Ring and Tip conductors and Ground. Overvoltages are normally caused by a.c. power system or lightning flash disturbances which are induced or conducted on to the telephone line.

The protector consists of two symmetrical voltage-triggered bidirectional thyristors. Overvoltages are initially clipped by breakdown clamping until the voltage rises to the breakover level, which causes the device to crowbar into a low-voltage on state. This low-voltage on state causes the current resulting from the overvoltage to be safely diverted through the device. The high crowbar holding current prevents d.c. latchup as the diverted current subsides.

The TISP3xxxH3SLL range is designed to voltage limit and withstand the listed international lightning surges in both polarities. These high current protection devices are in a 3-pin long-lead single-in-line (SLL) plastic package and are supplied in tube pack. These monolithic protection devices are fabricated in ion-implanted planar structures to ensure precise and matched breakover control and are virtually transparent to the system in normal operation.

How to Order

Device	Package	Carrier	Order As	Marking Code	Tube Qty.	Std. Qty.
TISP3xxxH3SLL	3-SIP (Long Lead)	Tube	TISP3xxxH3SLL-S	SP3xxxH3	50	1000

*RoHS Directive 2002/95/EC Jan 27 2003 including Annex
JANUARY 2005 - REVISED MAY 2007
Specifications are subject to change without notice.
Customers should verify actual device performance in their specific applications.

Absolute Maximum Ratings, T_A = 25 °C (Unless Otherwise Noted)

Rating		Symbol	Value	Unit
Repetitive peak off-state voltage	'3070 '3250 '3290	V_{DRM}	±58 ±190 ±220	V
Non-repetitive peak impulse current (see Notes 1, 2 and 3)				
2/10 µs (GR-1089-CORE, 2/10 µs voltage wave shape)		I_{PPSM}	±500	A
8/20 µs (IEC 61000-4-5, 1.2/50 µs voltage wave shape, 8/20 µs current combination wave generator)			±300	
10/160 µs (TIA-968-A, 10/160 µs voltage wave shape)			±250	
5/200 µs (VDE 0433, 10/700 µs voltage waveshape)			±220	
0.2/310 µs (I 31-24, 0.5/700 µs voltage waveshape)			±200	
5/310 µs (ITU-T K.20/21, 10/700 µs voltage wave shape)			±200	
5/310 µs (FTZ R12, 10/700 µs voltage waveshape)			±200	
5/320 µs (TIA-968-A, 9/720 µs voltage wave shape)			±200	
10/560 µs (TIA-968-A, 10/560 µs voltage wave shape)			±160	
10/1000 µs (GR-1089-CORE, 10/1000 µs voltage wave shape)			±100	
Non-repetitive peak on-state current (see Notes 1, 2 and 4)				
20 ms, 50 Hz (full sine wave)		I_{TSM}	55	A
16.7 ms 60 Hz (full sine wave)			60	
1000 s, 50 Hz a.c.			1	
Initial rate of rise of on-state current, exponential current ramp, maximum ramp value < 200 A		di_T/dt	400	A/µs
Junction temperature		T_J	-40 to +150	°C
Storage temperature range		T_{stg}	-65 to +150	°C

NOTES: 1. Initially the device must be in thermal equilibrium with T_J = 25 °C.
2. These non-repetitive rated currents are peak values of either polarity. The rated current values may be applied to the R or T terminals. Additionally, both R and T terminals may have their rated current values applied simultaneously (in this case the G terminal return current will be the sum of the currents applied to the R and T terminals). The surge may be repeated after the device returns to its initial conditions.
3. Above 85 °C, derate linearly to zero at 150 °C lead temperature.
4. EIA/JESD51-2 environment and EIA/JESD51-3 PCB with standard footprint dimensions connected with 5 A rated printed wiring track widths. Derate current values at -0.61%/°C for ambient tempeartures above 25 °C.

Electrical Characteristics for the R and G or T and G Terminals, T_A = 25 °C (Unless Otherwise Noted)

Parameter		Test Conditions		Min	Typ	Max	Unit
I_{DRM}	Repetitive peak off-state current	$V_D = V_{DRM}$	T_A = 25 °C T_A = 85 °C			±5 ±10	µA
$V_{(BO)}$	Breakover voltage	dv/dt = ±750 V/ms, R_{SOURCE} = 300 Ω	'3070 '3250 '3290			±70 ±250 ±290	V
$V_{(BO)}$	Impulse breakover voltage	dv/dt ≤ ±1000 V/µs, Linear voltage ramp, Maximum ramp value = ±500 V di/dt = ±20 A/µs, Linear current ramp, Maximum ramp value = ±10 A	'3070 '3250 '3290			±78 ±261 ±302	V
$I_{(BO)}$	Breakover current	dv/dt = ±750 V/ms, R_{SOURCE} = 300 Ω		±150		±600	mA
V_T	On-state voltage	I_T = ±5 A, t_w = 100 µs				±3	V
I_H	Holding current	I_T = ±5 A, di/dt = ±30 mA/ms		±150		±600	mA
dv/dt	Critical rate of rise of off-state voltage	Linear voltage ramp, maximum ramp value < 0.85V_{DRM}		±5			kV/µs
I_D	Off-state current	V_D = ±50 V	T_A = 85 °C			±10	µA

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Electrical Characteristics for the R and G or T and G Terminals, T_A = 25 °C (Unless Otherwise Noted) (Continued)

Parameter		Test Conditions		Min	Typ	Max	Unit
C_O	Off-state capacitance	f = 100 kHz, V_d = 1 V rms, V_D = 0 V	'3070			170	pF
			'3250 & '3290			84	
		f = 100 kHz, V_d = 1 V rms, V_D = -1 V	'3070			150	
			'3250 & '3290			67	
		f = 100 kHz, V_d = 1 V rms, V_D = -2 V	'3070			140	
			'3250 & '3290			62	
		f = 100 kHz, V_d = 1 V rms, V_D = -50 V	'3070			73	
			'3250 & '3290			28	
		f = 100 kHz, V_d = 1 V rms, V_D = -100 V	'3250 & '3290			26	

Electrical Characteristics for the R and T Terminals, T_A = 25 °C (Unless Otherwise Noted)

Parameter		Test Conditions		Min	Typ	Max	Unit
I_{DRM}	Repetitive peak off-state current	$V_D = 2V_{DRM}$				±5	μA
$V_{(BO)}$	Breakover voltage	dv/dt = ±750 V/ms, R_{SOURCE} = 300 Ω	'3070			±140	V
			'3250			±500	
			'3290			±580	
$V_{(BO)}$	Impulse breakover voltage	dv/dt ≤ ±1000 V/μs, Linear voltage ramp, Maximum ramp value = ±500 V di/dt = ±20 A/μs, Linear current ramp, Maximum ramp value = ±10 A	'3070			±156	V
			'3250			±522	
			'3290			±604	

Thermal Characteristics, T_A = 25 °C (Unless Otherwise Noted)

Parameter		Test Conditions	Min	Typ	Max	Unit
$R_{\theta JA}$	Junction to ambient thermal resistance	EIA/JESD51-3 PCB, $I_T = I_{TSM(1000)}$ (see Note 5)			50	°C/W

NOTE: 5. EIA/JESD51-2 environment and PCB has standard footprint dimensions connected with 5 A rated printed wiring track widths.

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Parameter Measurement Information

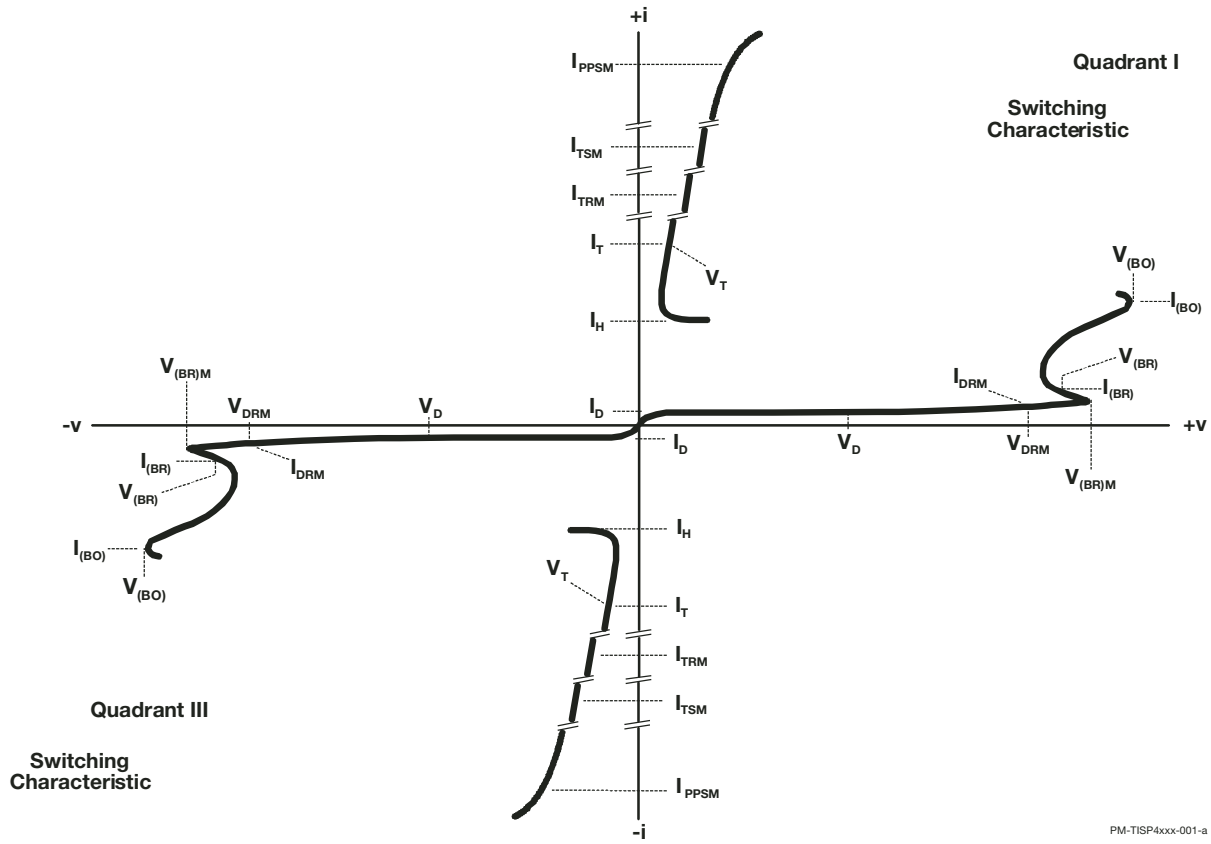

Figure 1. Voltage-Current Characteristic for Terminal Pairs

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