



GoldStar
GOLDSTAR ELECTRON CO., LTD.

GM76C256BL/BLL

32,768 WORDS × 8 BIT

CMOS STATIC RAM

Description

The GM76C256B is a 262,144 bits static random access memory organized as 32,768 words by 8 bits. Using a $0.8\mu\text{m}$ advanced CMOS technology, it provides high speed operation with minimum cycle time of 55/70/85ns. The device is placed in a low power standby mode with $\overline{\text{CS}}$ high and output enable ($\overline{\text{OE}}$) allows fast memory access. Thus it is suitable for high speed and low power applications, particularly where battery back-up is required. The GM76C256BL/BLL is offered in a 28-pin DIP(600mil), SOP(330mil) and TSOP I (0814).

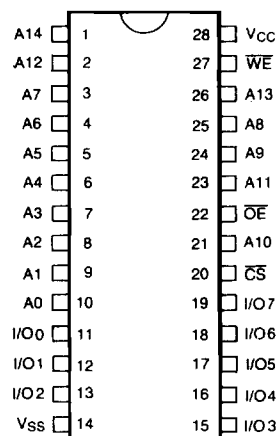
Features

- Fast access time and Cycle Time: 55/70/85ns
- Low Power Operation
 - Standby(CMOS) : 0.55mW (Max.) L-Version
 - : 0.11mW (Max.) LL-Version
 - Operation : 385mW (Max.)
- Completely Static RAM: No Clock or Timing Strobe Required.
- Equal Access and Cycle Time
- Capability of Battery Back-up Operation
- Single $5\text{V} \pm 10\%$ Operation
- Standard 28 DIP, SOP and TSOP I

Pin Description

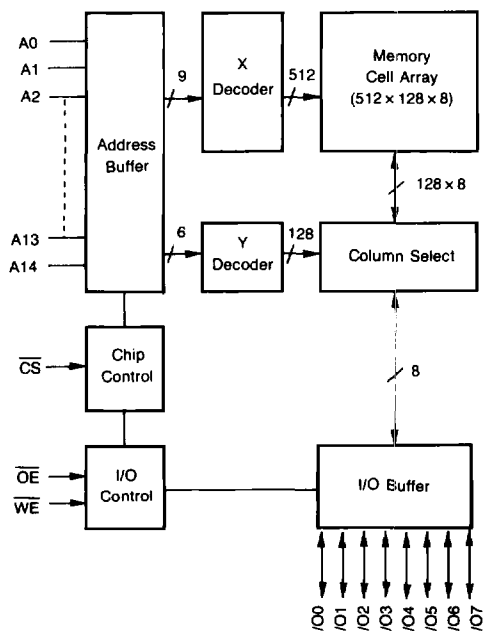
Pin	Function
A0 ~ A14	Address Inputs
$\overline{\text{WE}}$	Write Enable Input
$\overline{\text{OE}}$	Output Enable Input
$\overline{\text{CS}}$	Chip Select Input
I/O0 ~ I/O7	Data Input/Output
V _{CC}	Power Supply +5V
V _{SS}	Ground

Pin Configuration



(Top View)

Block Diagram



Absolute Maximum Ratings*

Symbol	Parameter	Rating	Unit
T _A	Ambient Temperature under Bias	0 ~ 70	°C
T _{STG}	Storage Temperature	-65 ~ 150	°C
T _{SOL}	Soldering Temperature and Time	260, 10 (at lead)	°C, S
V _{CC}	Supply Voltage	-0.3 ~ 7.0	V
V _{IN}	Input Voltage	-0.3* ~ 7.0	V
V _{I/O}	Input and Output Voltage	-0.5 ~ V _{CC} + 0.5	V
P _D	Power Dissipation	1.0	W

*: -3.0V at pulse width 50ns Max.

Recommended Operating Conditions (T_A = 0 ~ 70°C)

Symbol	Parameter	Min	Typ	Max	Unit
V _{CC}	Supply Voltage	4.5	5.0	5.5	V
V _{IH}	Input High Voltage	2.2	—	V _{CC} + 0.3	V
V _{IL}	Input Low Voltage	-0.3	—	0.8	V
V _{DR}	Data Retention Supply Voltage	2.0	—	5.5	V

Truth Table

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Input/Output	Mode
H	X	X	High Z	Deselect Power Down
L	H	L	Data Out	Read
L	L	X	Data In	Write
L	H	H	High Z	Deselect

Note: X means don't care

DC Electrical Characteristics: (V_{CC} = 5V ± 10%, T_A = 0 ~ 70°C)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V _{OH}	Output High Voltage	I _{OH} = -1.0mA	2.4	—	—	V
V _{OL}	Output Low Voltage	I _{OL} = 2.1mA	—	—	0.4	V
I _{I(L)}	Input Leakage Current	V _{SS} ≤ V _{IN} ≤ V _{CC}	-1	—	1	μA
I _{O(L)}	Output Leakage Current	$\overline{CS} = V_{IH}$ or $\overline{WE} = V_{IL}$ or $\overline{OE} = V_{IH}$, V _{SS} ≤ V _{OUT} ≤ V _{CC}	-1	—	1	μA
I _{CCS1}	Stand-by Power Supply Current	$\overline{CS} = V_{IH}$	—	—	3	mA
I _{CCS2}		$\overline{CS} \geq V_{CC} - 0.2V$ GM76C256BL GM76C256BLL	— —	2* 1*	100 20	μA μA
I _{CC}	Operating Supply Current	$\overline{CS} = V_{IL}$, V _{I/O} = 0mA	—	—	35	mA
I _{CC1}	Average Operating Power Supply Current	Min. Cycle, duty = 100% I _{I/O} = 0mA	—	—	70	mA

*TYP. Values are measured at 25°C, V_{CC} = 5V

AC Operating Characteristics ($V_{CC}=5V \pm 10\%$, $T_A=0 \sim 70^\circ C$)

Read Cycle

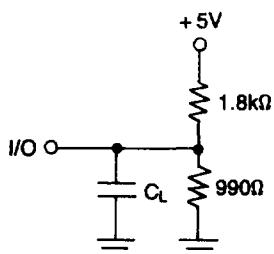
Symbol	Parameter	Condi- tions	GM76C256B-55		GM76C256B-70		GM76C256B-85		Unit
			Min	Max	Min	Max	Min	Max	
t_{RC}	Read Cycle Time	*1	55	—	70	—	85	—	ns
t_{AA}	Address Access Time		—	55	—	70	—	85	ns
t_{ACS}	Chip Select Access Time		—	55	—	70	—	85	ns
t_{OE}	Output Enable Access Time		—	25	—	35	—	45	ns
t_{OH}	Output Hold Time		10	—	10	—	10	—	ns
t_{CLZ}	Chip Deselection to Output in Low-Z	*2	10	—	10	—	10	—	ns
t_{OLZ}	Output Disable to Output in Low-Z		5	—	5	—	5	—	ns
t_{CHZ}	Chip Deselection to Output in High-Z		0	20	0	30	0	30	ns
t_{OHZ}	Output Disable to Output in High-Z		0	20	0	30	0	30	ns

Write Cycle

Symbol	Parameter	Condi- tions	GM76C256B-55		GM76C256B-70		GM76C256B-85		Unit
			Min	Max	Min	Max	Min	Max	
t_{WC}	Write Cycle Time	*1	55	—	70	—	85	—	ns
t_{CW}	Chip Select to End of Write		45	—	60	—	75	—	ns
t_{AW}	Address Set-up Time to End of Write		50	—	60	—	75	—	ns
t_{AS}	Address Set-up Time		0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width		40	—	50	—	60	—	ns
t_{WR}	Write Recovery Time		0	—	0	—	0	—	ns
t_{DW}	Data to Write Time Overlap		25	—	30	—	40	—	ns
t_{DH}	Data Hold Time		0	—	0	—	0	—	ns
t_{WHZ}	Write to Output in High-Z	*2	0	20	0	25	0	30	ns
t_{OW}	Output Active from End of Write		0	—	5	—	5	—	ns

***1 Test Conditions**

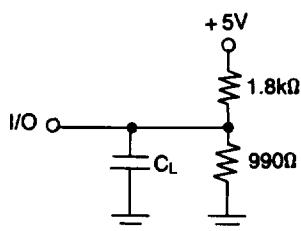
1. Input pulse level: 0.6V to 2.4V
2. $t_r = t_f = 5\text{ns}$
3. Input and output timing reference levels: 1.5V
4. Output load $C_L = 100\text{pF}$



$C_L = 100\text{pF}$ (Includes Jig Capacitance)

***2 Test Conditions**

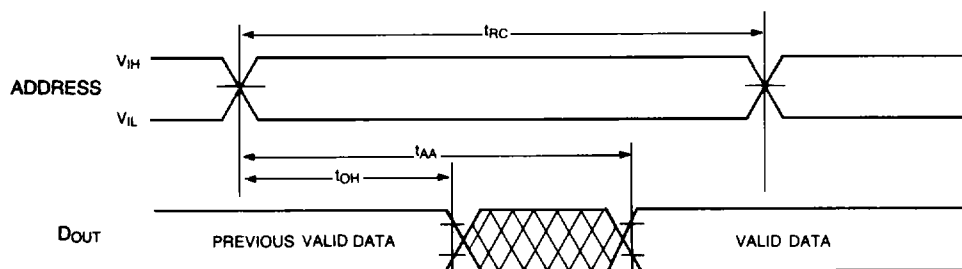
1. Input pulse level: 0.6V to 2.4V
2. $t_r = t_f = 5\text{ns}$
3. Input timing reference level: 0.8V to 2.2V.
4. Output timing reference levels:
 $\pm 200\text{mV}$ (the level displace from stable output voltage level)
5. Output load $C_L = 5\text{pF}$



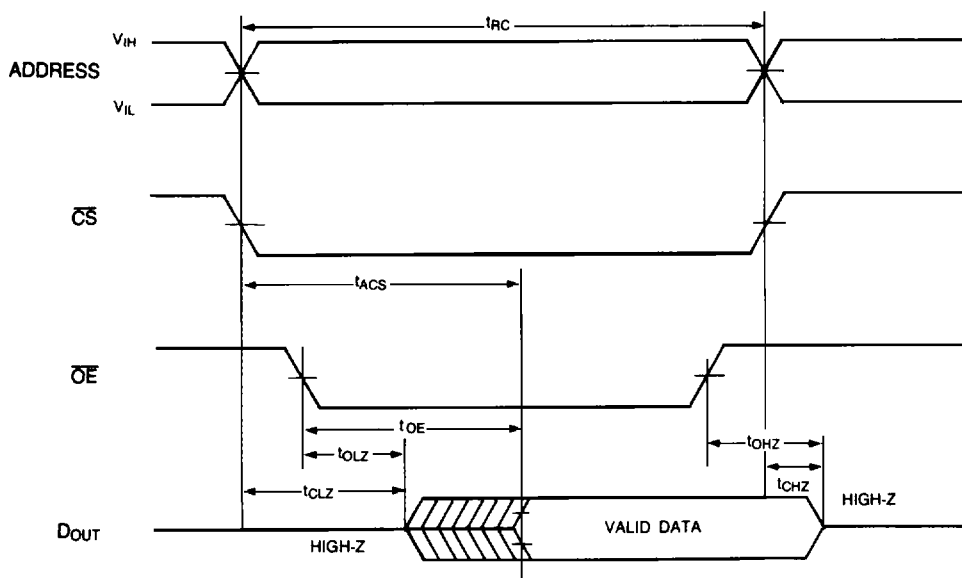
$C_L = 5\text{pF}$ (Includes Jig Capacitance)

TIMING WAVEFORMS

Read Cycle 1 (Notes 1, 3)

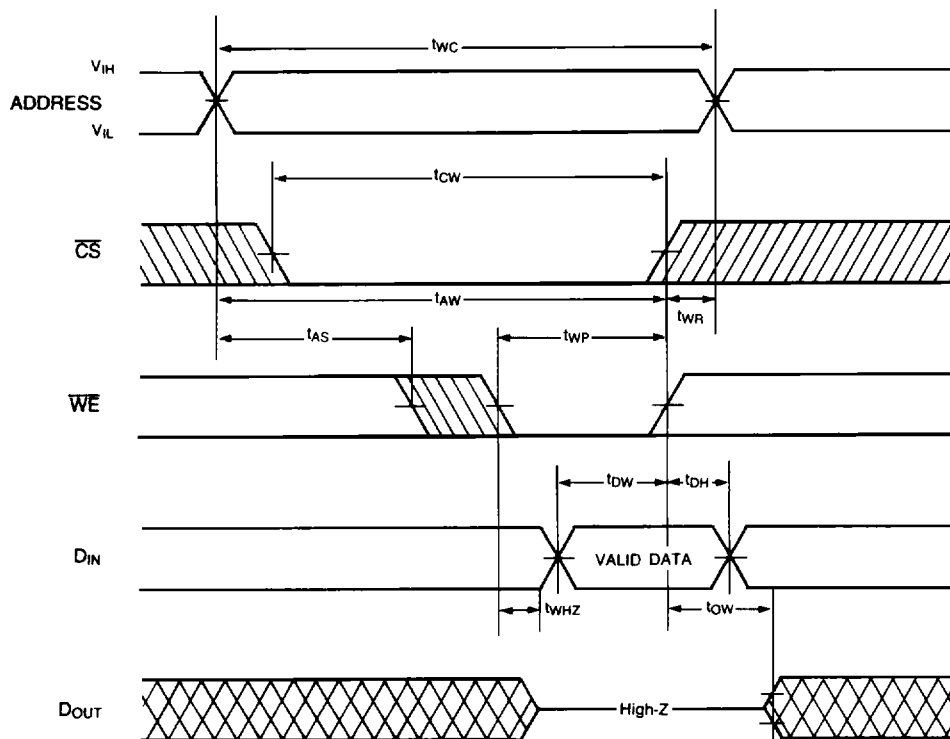


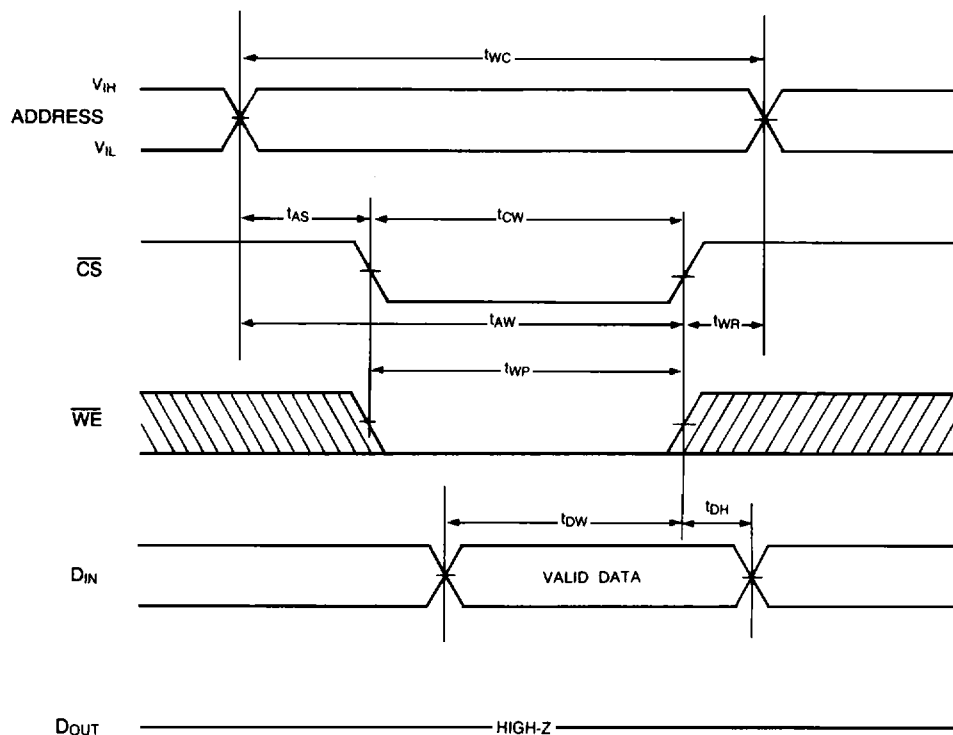
Read Cycle 2 (Notes 2, 3)



Notes:

1. Device is continuously selected. $\overline{OE}, \overline{CS} \leq V_{IL}$
2. Address valid prior to or coincident with $\overline{CS}$ transition low.
3. $\overline{WE}$ is high for read cycle.

Write Cycle 1 ($\overline{WE}$ Controlled) (Note 1, 2)

Write Cycle 2 ($\overline{CS}$ Controlled) (Note 1, 2, 3)

Notes:

1. The internal write time of the memory is defined by the overlap of $\overline{CS}$ low and $\overline{WE}$ low. Both signals must be low to initiate a write and either signal can terminate a write by going high. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
2. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
3. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.

Capacitance

Symbol	Parameter	Test Condition	Min	Max	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1MHz V _{CC} = 5.0V	—	6	pF
C _{OUT}	Output Capacitance		—	8	

Note: Tested on a sample basis

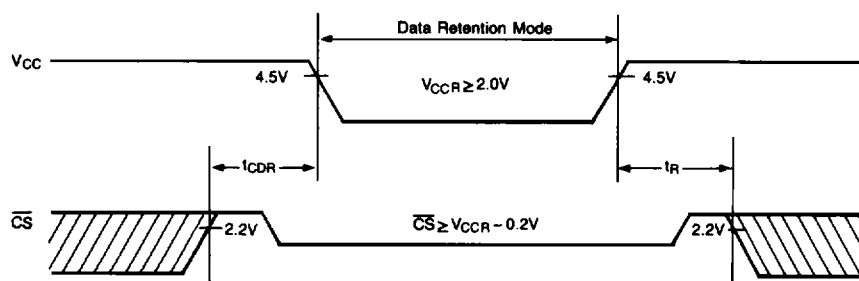
Data Retention Characteristics: (T_A = 0 ~ 70°C)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V _{CCR}	Data Retention Supply Voltage	$\overline{CS} \geq V_{CC} - 0.2V$	2.0	—	5.5	V
I _{CCR}	Data Retention Current	V _{CC} = 3.0V $\overline{CS} \geq 2.8V$	—	1**	50	μA
		BL	—	0.5**	10	
t _{CDR}	Chip Select Data Hold Time	Refer to the figure below	0	—	—	ns
t _R	Operation Recovery Time		t _{RC} *	—	—	ns

Note* : Read Cycle Time

Note**: Typ, Values are measured at 25°C.

Data Retention Timing

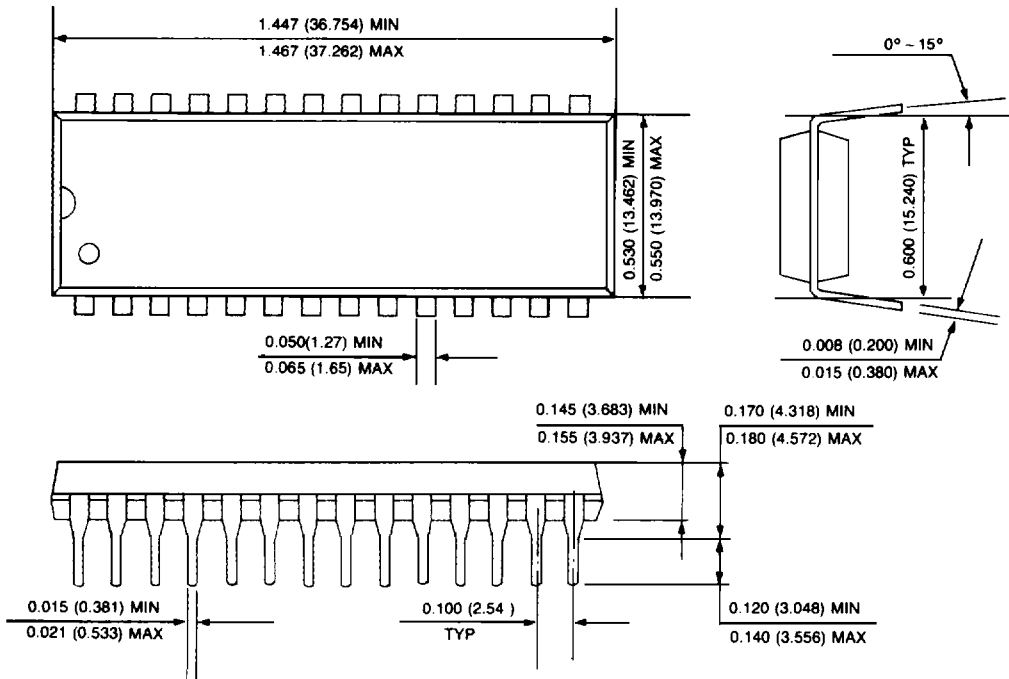


Note: When retaining data in standby mode, supply voltage can be lowered within a certain range. Read or write cycle cannot be performed while the supply voltage is low.

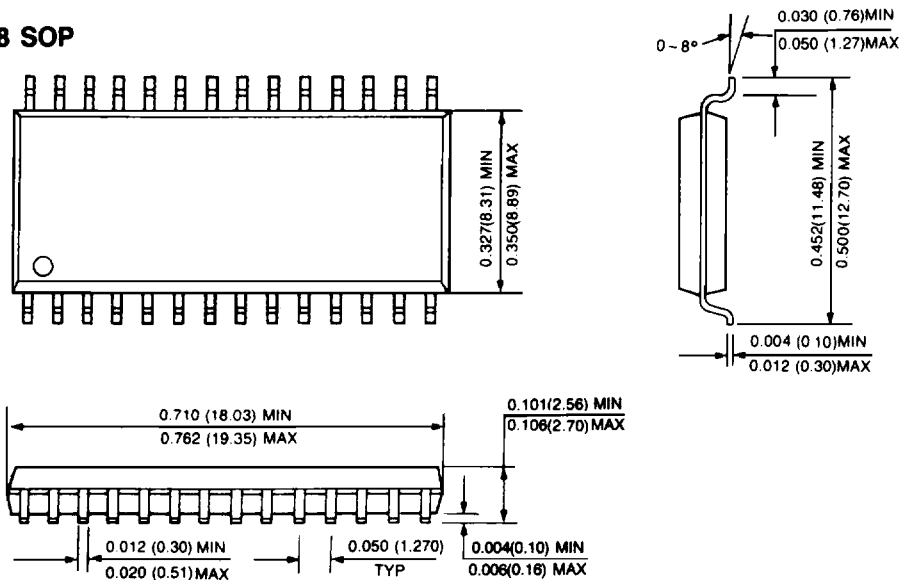
Package Dimensions

28 DIP

Unit: inches (mm)



28 SOP



28 TSOP

Unit: inches (mm)

