Edge622/624
Very High-Speed Dual and Quad Channel ECL Delay Lines

HIGH-PERFORMANCE PRODUCTS – ATE

Description

The Edge622 and Edge624 are dual and quad (respectively) delay and deskew elements. Manufactured in a high performance bipolar process, they are designed primarily for channel deskew applications in Memory Test Equipment.

The parts offer three distinct full scale delay ranges of 14 ns, 24 ns, and 34 ns. In the 14 ns and 24 ns ranges, independent adjustment of the rising edge vs. the falling edge is achievable.

The Edge622 and Edge624 have a drive mode, where one input signal is routed to all of the outputs. This mode is particularly useful in a fanout application.

The delay value (and resolution) is controlled via an external voltage DAC.

These deskew elements are designed specifically to be monotonic and stable while delaying a very narrow pulse over a wide delay range.

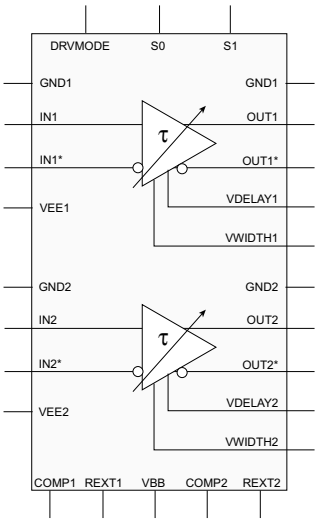
Features

- Pin and Functionally Compatible with the Bt622 and Bt624
- Independent Delay Adjustments for Positive and Negative Transitions
- Fanout Mode for One Input Distributed to All Channels
- 28-pin or 44-pin Plastic J-Lead (PLCC) Package with Internal Heat Spreader

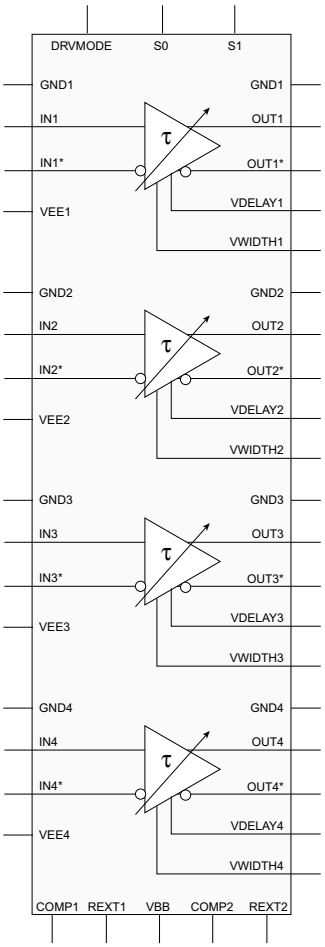
Applications

- Automatic Test Equipment
  - Memory Tester Drive Only Channel Deskew
  - I/O Channel Deskew

Functional Block Diagrams



Edge622 Dual Channel



Edge624 Quad Channel

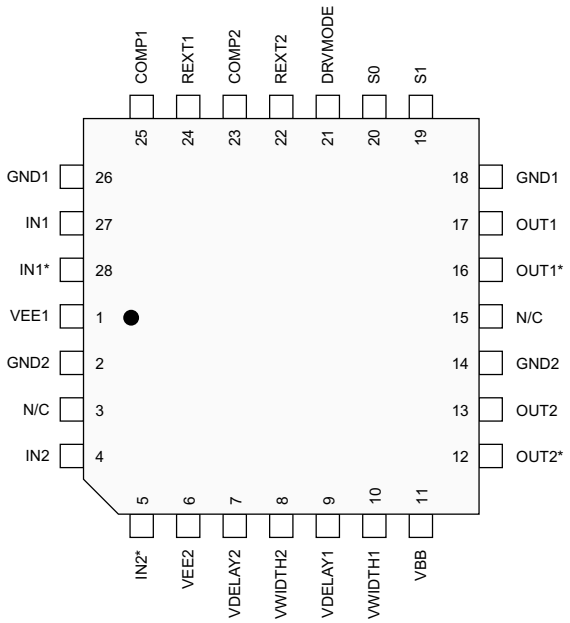
PIN Description

The signals that are individually assigned for each channel are suffixed by the channel number: 1 and 2 for the Edge622, and 1 through 4 for the Edge624.

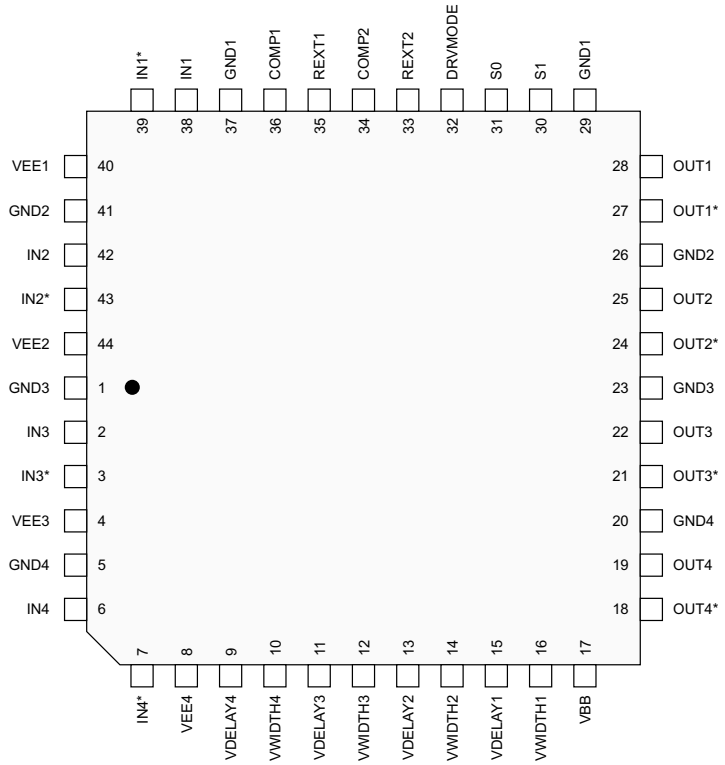
Pin Name	624 Pin #	622 Pin #	Description
Digital			
IN, IN*	38, 39, 42, 43, 2, 3, 6, 7	27, 28, 4, 5	The input signal to be delayed. (Differential digital inputs.)
OUT, OUT*	28, 27, 25, 24, 22, 21, 19, 18	17, 16, 13, 12	The corresponding delayed output signal. (Differential ECL compatible outputs.)
DRVMODE	32	21	Single-ended 10KH ECL compatible input which determines whether the part is in fanout mode.
S0, S1	31, 30	20, 19	Single-ended 10KH ECL compatible Inputs which define the operating mode.
Analog			
VDELAY	15, 13, 11, 19	9, 7	Analog voltage input which controls the amount of propagation delay for each channel.
VWIDTH	16, 14, 12, 10	10, 8	Analog voltage input which controls the amount of falling edge delay for each channel.
VBB	17	11	Analog voltage output, nominally equal to –1.3V, used as a reference for single-ended inputs.
REXT1	35	24	Analog input current used to establish the bias current for the VDELAY and VWIDTH inputs.
REXT2	33	22	Analog input current used to establish the bias level for the delay cells.
COMP1	36	25	Compensation pin. A 0.1 µF ceramic capacitor must be connected between COMP1 and VEE.
COMP2	34	23	Compensation pin. A 0.1 µF ceramic capacitor must be connected between COMP2 and VEE.
Power			
GND	1, 5, 20, 23, 26, 29, 37, 41	2, 14, 18, 26	Device ground.
VEE	4, 8, 40, 44	1, 6	Device power supply.
N/C		3, 15	No connect.

PIN Description *(continued)*

Edge622
28-pin Plastic J-Lead
w/Internal Heat Spreader



Edge624
44-pin Plastic J-Lead
w/Internal Heat Spreader



Circuit Description

Chip Overview

The Edge624 is a quad, and the Edge622 is a dual, delay line and deskew element. Each part offers three ranges of delay (Tspan); 14 ns, 24 ns, or 34 ns, where the VDELAY inputs adjust the overall propagation delay of the part. In addition, the parts support a separate rising and falling edge delay for the 14 ns and 24 ns ranges only, where the VWIDTH inputs control the falling edge delay. There is also a drive mode, where the channel 2 input drives all four Edge624 outputs (or channel 1 drives both Edge622 outputs), with all other inputs ignored.

The Edge622 and Edge624 are designed to be monotonic and very stable in all modes of operation.

Figures 1 and 2 show simplified block diagrams of the two parts.

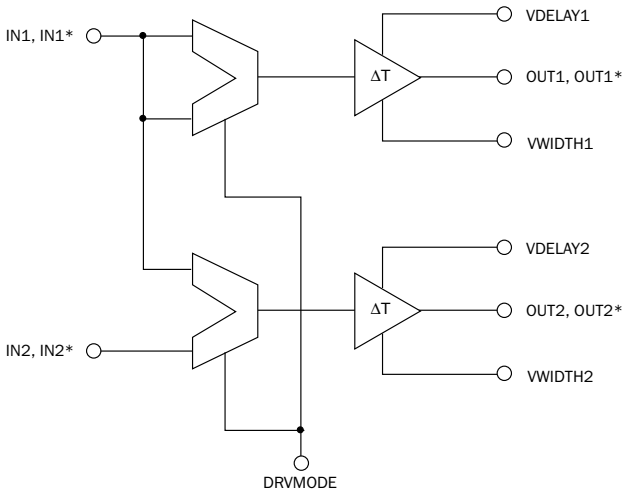


Figure 1. Edge622 Block Diagram

Data Sheet Nomenclature

The remainder of the data sheet will be written for the Edge624. All circuit descriptions also pertain to the Edge622, only channels 3 and 4 will not apply.

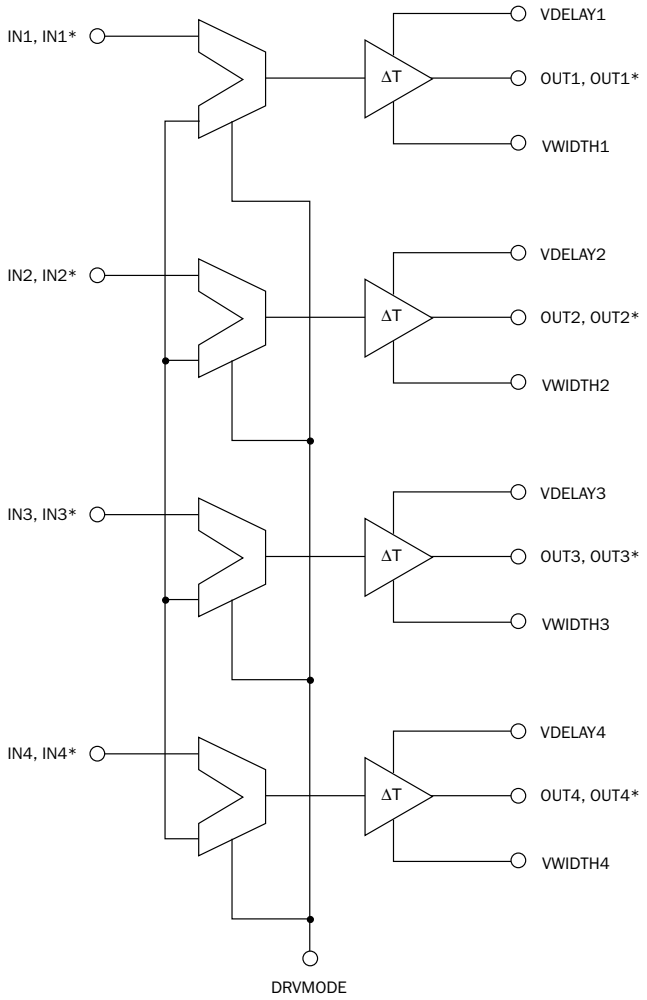


Figure 2. Edge624 Block Diagram

Circuit Description *(continued)*

Operating Modes

The Edge624 has 5 modes of operation, which are described in Table 1. (Mode 4 is not a valid mode.)

Mode	S1	S0	TSPAN	VWIDTH
0	0	0	14 ns	N/A
1	0	1	24 ns	N/A
2	1	0	14 ns	±5 ns
3	1	1	24 ns	±5 ns
4	VEE	0	N/A	N/A
5	VEE	1	34 ns	N/A

Table 1. Delay Ranges Versus Mode

Modes 0, 1, and 5

Modes 0, 1, and 5 are simple delay modes (see Figures 3 and 4). An input signal comes into each channel and is delayed by some programmable amount determined by the analog input VDELAY.

The rising and falling edges are delayed equally. The VWIDTH analog input has no function in modes 0 and 2, and VWIDTH must be connected to VDELAY in mode 5. The propagation delay for a rising and falling edge is defined as

$$Tpd+, Tpd- = Tpd(min) + Tspan$$

where Tpd(min) is the raw propagation delay of the part with minimum programmed delay, and Tspan is the additional delay programmed via the VDELAY input.

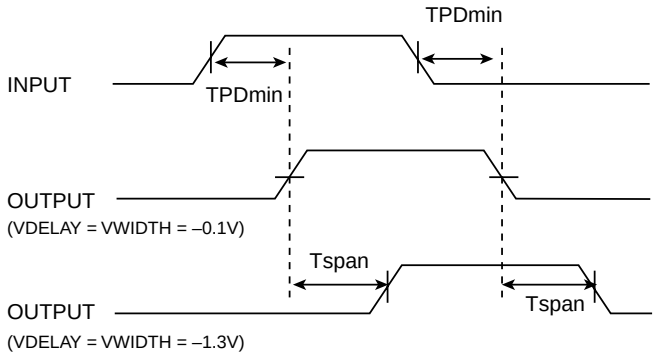


Figure 3. Modes 0, 1, and 5 VDELAY Control

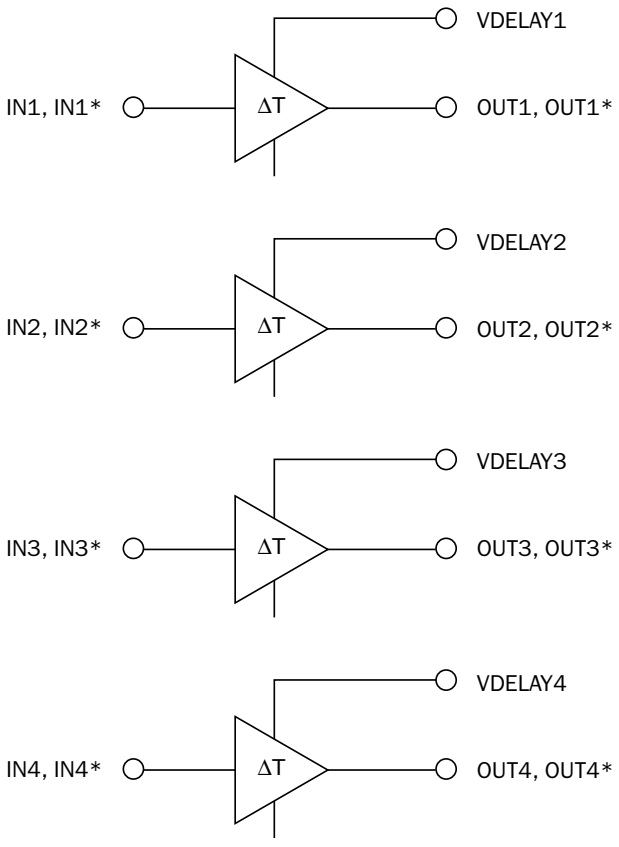


Figure 4. Modes 0, 1, and 5 Functional Diagram

Circuit Description *(continued)*

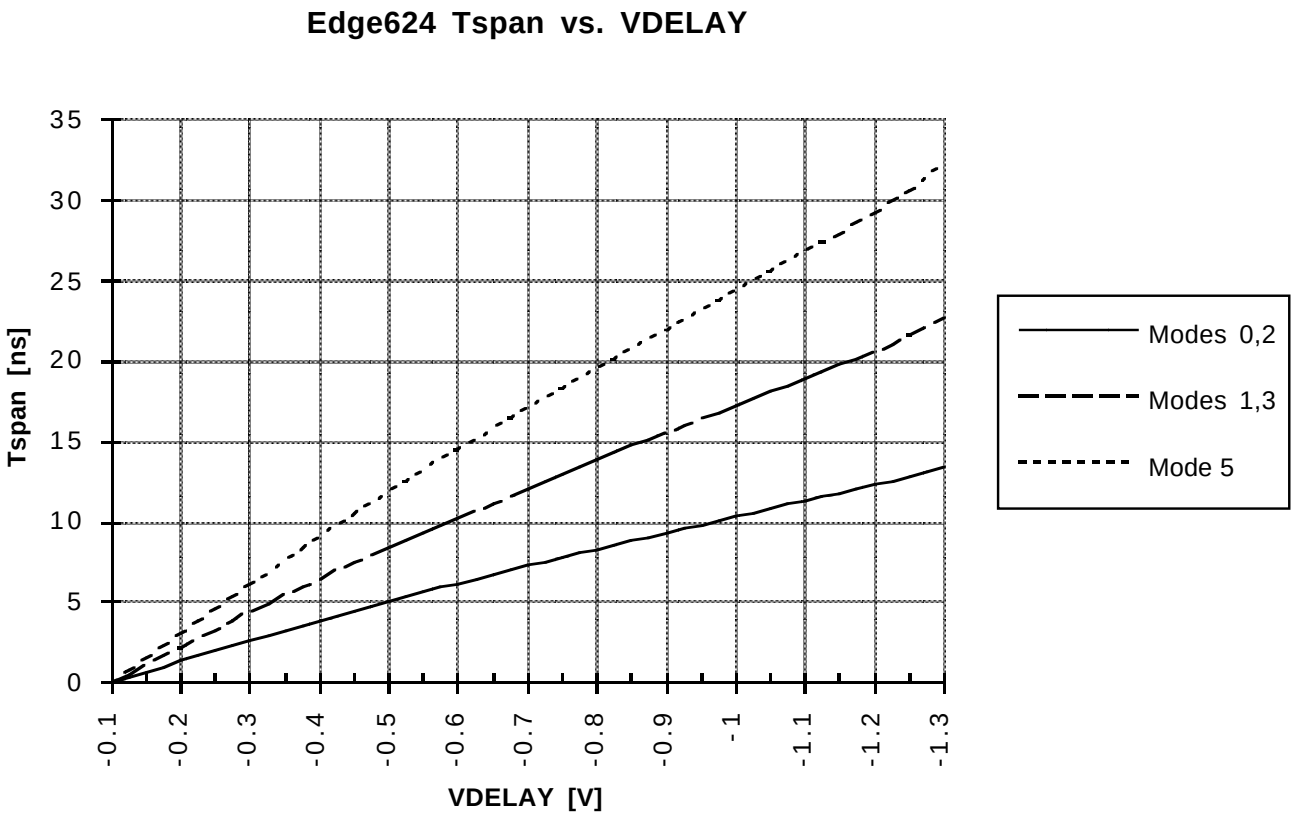


Figure 5. Tspan Transfer Function

Analog Delay Inputs

VDELAY and VWIDTH are analog voltage inputs which control the delay of the rising and falling edge. VDELAY and VWIDTH vary from -0.1V (minimum delay) to -1.3V (maximum delay).

These inputs are designed to sink a constant input current, typically 1.0 mA (with REXT1 = 1.3 KΩ), over their operating range from -0.1V to -1.3V. Any voltage DAC used to drive these inputs directly needs to source 1.0 mA. Any current DAC used needs to factor in the constant 1.0 mA input current.

The equation used to establish the VDELAY and VWIDTH input currents is:

$$I\,(VWIDTH, VDELAY) = 1.3V / REXT1.$$

The transfer function for Tspan vs. VDELAY is shown for all modes in Figure 5.

Circuit Description *(continued)*

Modes 2 and 3

Modes 2 and 3 allow independent adjustment of the rising and falling edges (see Figures 6 and 7). The propagation delay for a rising edge is defined as

$$Tpd+ = Tpd(min) + Tspan$$

where Tpd(min) is the raw propagation delay of the part with minimum programmed delay, and Tspan is the additional delay programmed via the VDELAY input.

The propagation delay for a falling edge is defined as

$$Tpd- = Tpd(min) + Tspan + Twidth$$

where Twidth is defined as the additional delay incurred by adjusting the VWIDTH input. Notice that Twidth can be either positive or negative over a ± 5 ns range. This flexibility allows the part the either expand or contract an input signal (see Figure 6).

Notice also that Tpd+ is a function of VDELAY only, while Tpd- is a function of VDELAY and VWIDTH. The transfer function for Tspan vs. VDELAY is shown for both modes in figure 5. The transfer function for Twidth vs. VWIDTH and VDELAY is shown in Figure 8.

Programming Sequence

VDELAY, in addition to affecting the placement of the rising edge, also affects the falling edge. Therefore, when calibrating a system, VDELAY should be adjusted first. As VWIDTH affects only the falling edge, it should be adjusted after VDELAY is established.

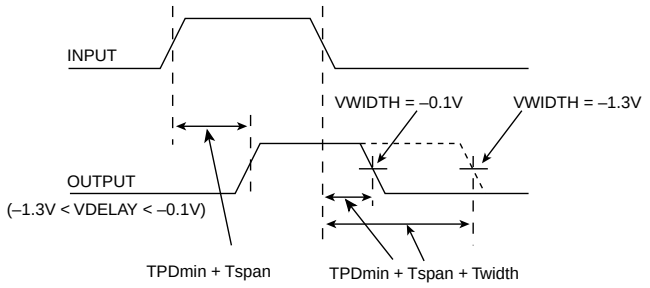


Figure 6. Mode 2 and 3 VDELAY and VWIDTH Controls

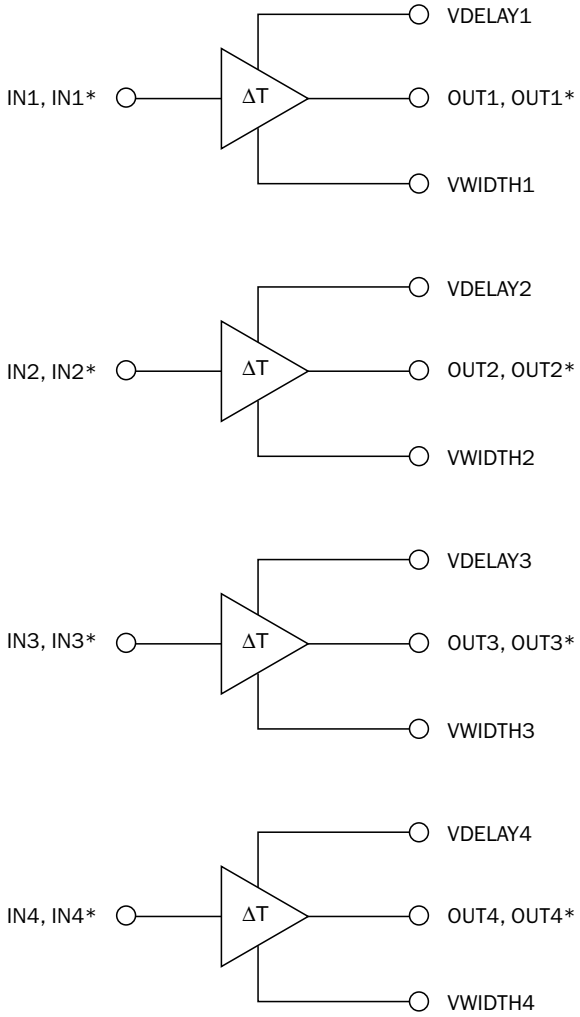


Figure 7. Functional Model in Modes 2 and 3

Circuit Description *(continued)*

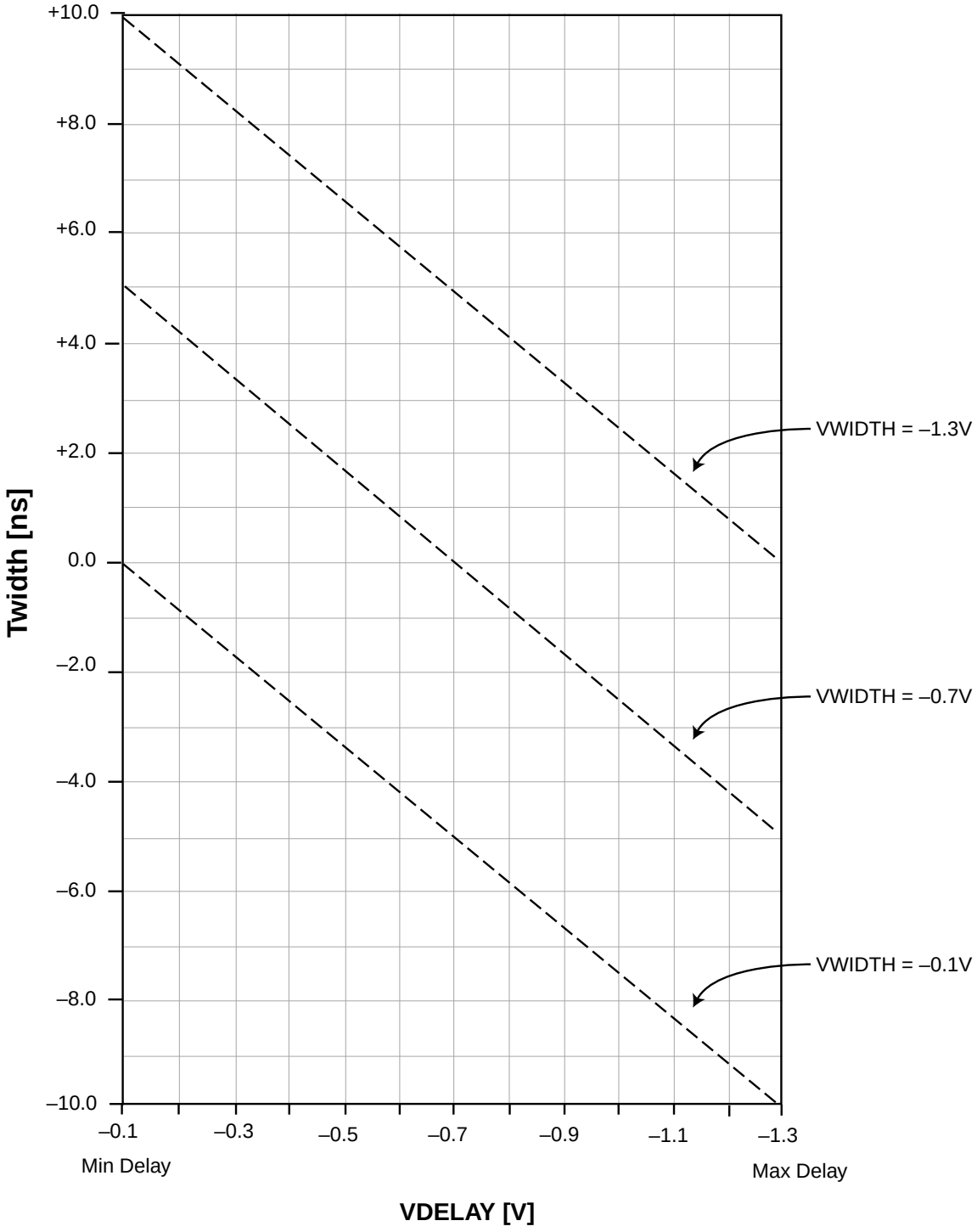


Figure 8. Mode 2 and 3 Transfer Function

Circuit Description *(continued)*

Drive Mode

With DRVMODE = 1, the input signal on channel 2 will be routed to all Edge624 delay paths. (Channel 1 will be routed to both Edge622 outputs.) In drive mode, all 5 operating modes still offer the same delay range and edge control features. The only difference is that the input signal now comes from channel 2, while all other inputs (In/In*) are ignored.

Figures 9 through 12 show a simplified model for drive mode.

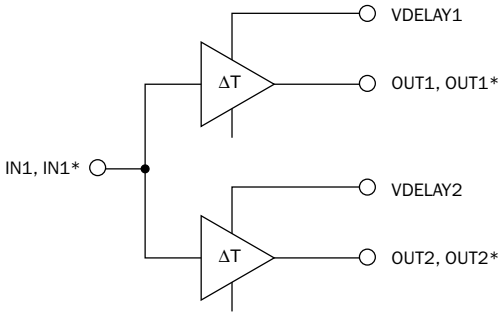


Figure 9. Edge622 Drive Mode for Operating Modes 0, 1, and 5.

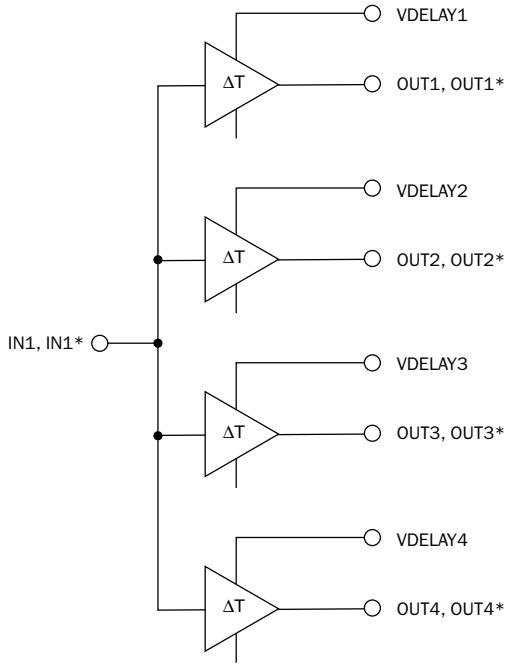


Figure 10. Edge624 Drive Mode for Operating Modes 0, 1, and 5

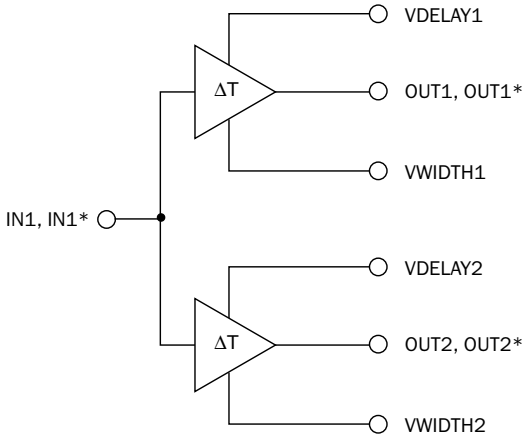


Figure 11. Edge622 Drive Mode for Operating Modes 2 and 3.

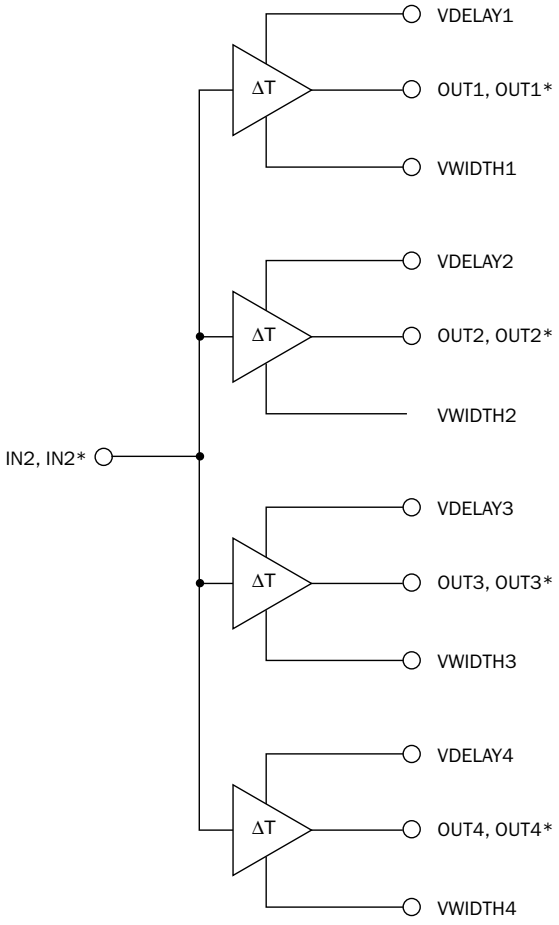


Figure 12. Edge624 Drive Mode for Operating Modes 2 and 3.

Application Information

Power Up Initialization

Note: Modes 2 and 3 use an SR flip-flop at the output stage; modes 0, 1, and 5 do not. Therefore, upon power up in modes 2 or 3, or when operating modes are being changed into modes 2 or 3, the SR flip-flop is in an indeterminate state and the output may not reflect the input condition. A rising or falling edge that propagates through the channel will correctly reset the part. Therefore, in mode 2 or 3, a dummy edge should be applied before calibration or real time execution.

Notice also that in modes 0, 1, and 5 there is no flip-flop. The output will therefore always reflect the status of the inputs.

Minimum Pulse Width

The minimum pulse width that the part can support is a function of the operating mode and the programmed delay value. Figures 13, 14, and 15 document the maximum usably delay for all modes and ranges.

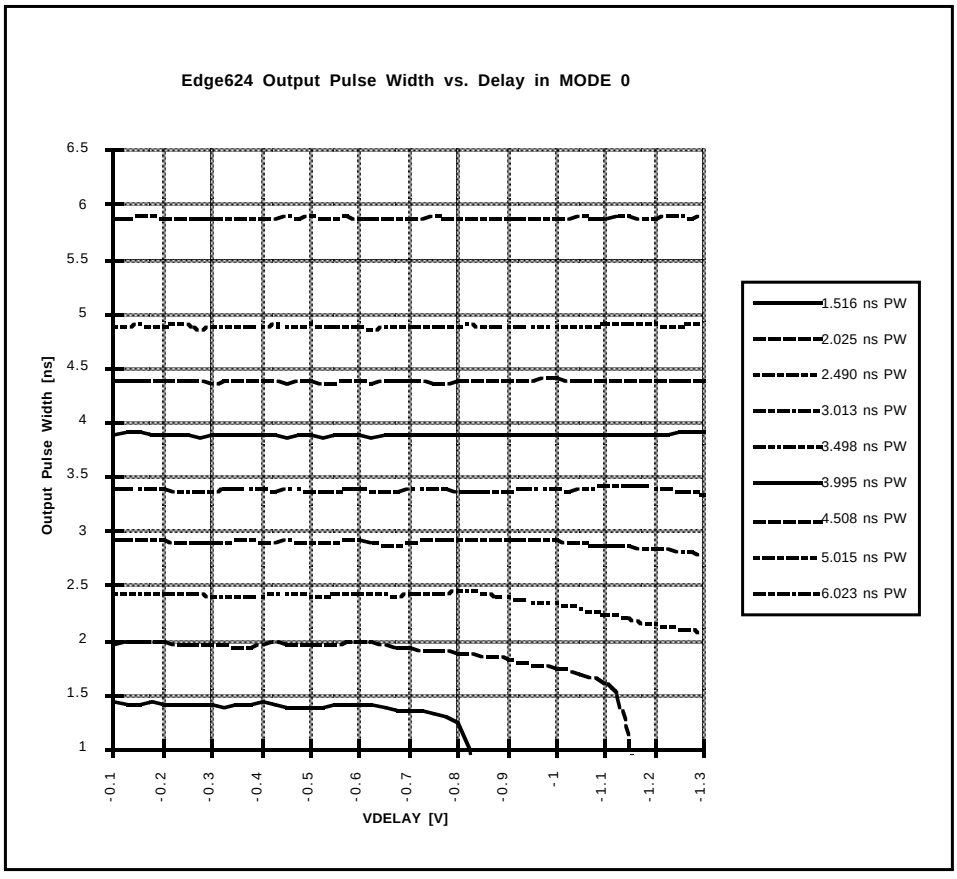


Figure 13. Minimum Pulse Width Capability in Mode 0

Application Infor mation *(continued)*

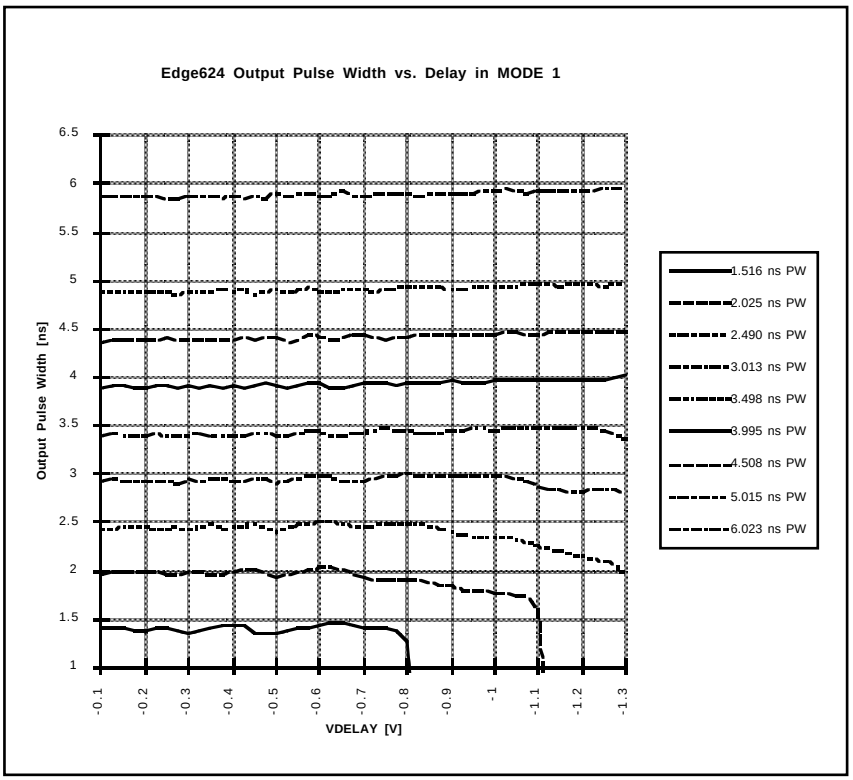


Figure 14. Minimum Pulse Width Capability in Mode 1

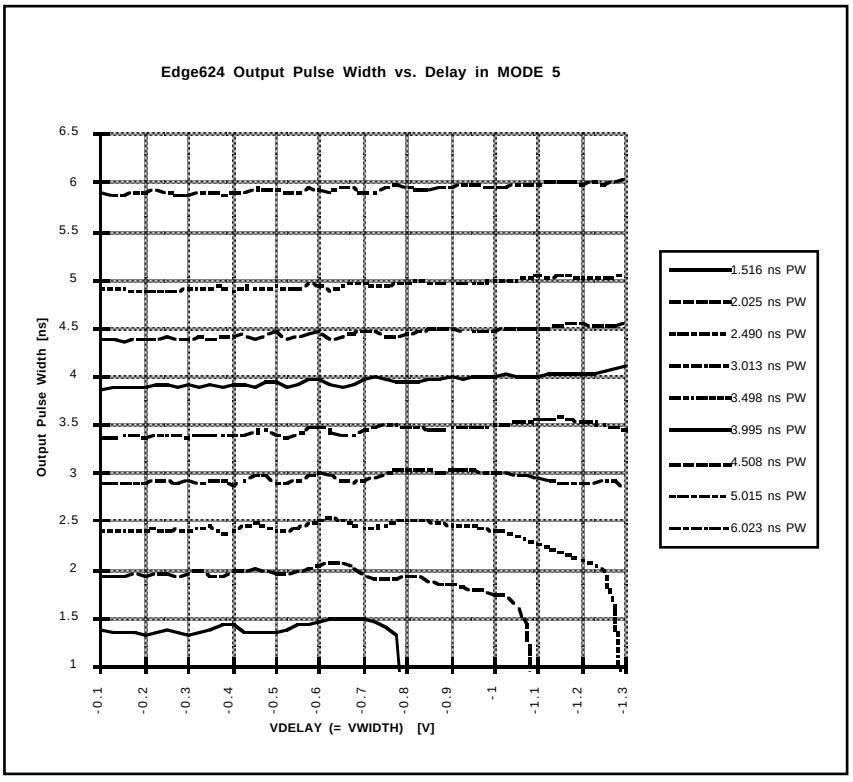


Figure 15. Minimum Pulse Width Capability in Mode 5

Application Information *(continued)*

Linearity

The Edge622 and Edge624 are designed to be monotonic and stable, although not necessarily linear. However, there is a characteristic nonlinearity curve associated with each operating mode of the part. Figures 16, 17, and 18 show this nonlinearity.

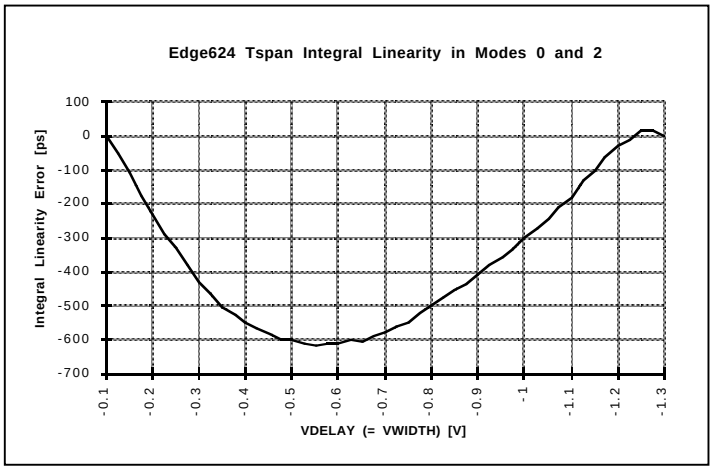


Figure 16. Integral Linearity Error - Modes 0 and 2

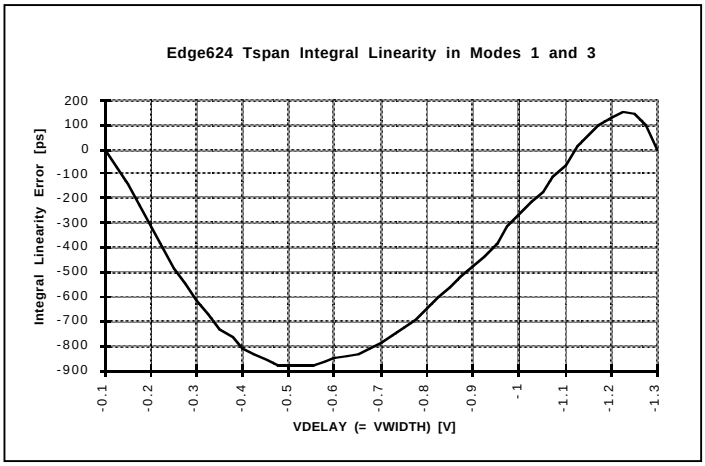


Figure 17. Integral Linearity Error - Modes 1 and 3

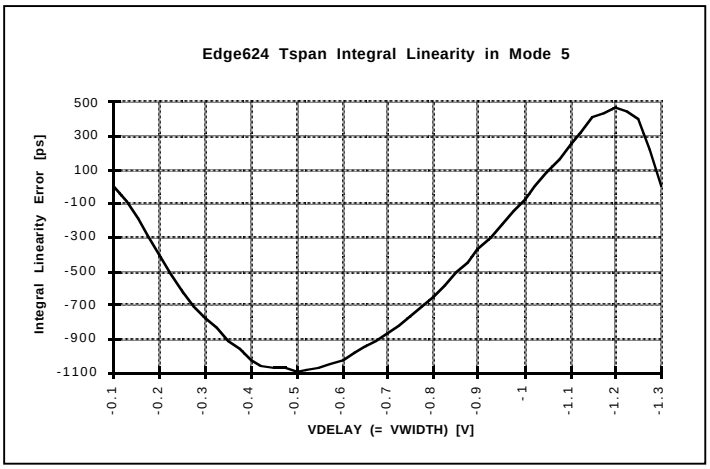


Figure 18. Integral Linearity Error - Mode 5

Application Information *(continued)*

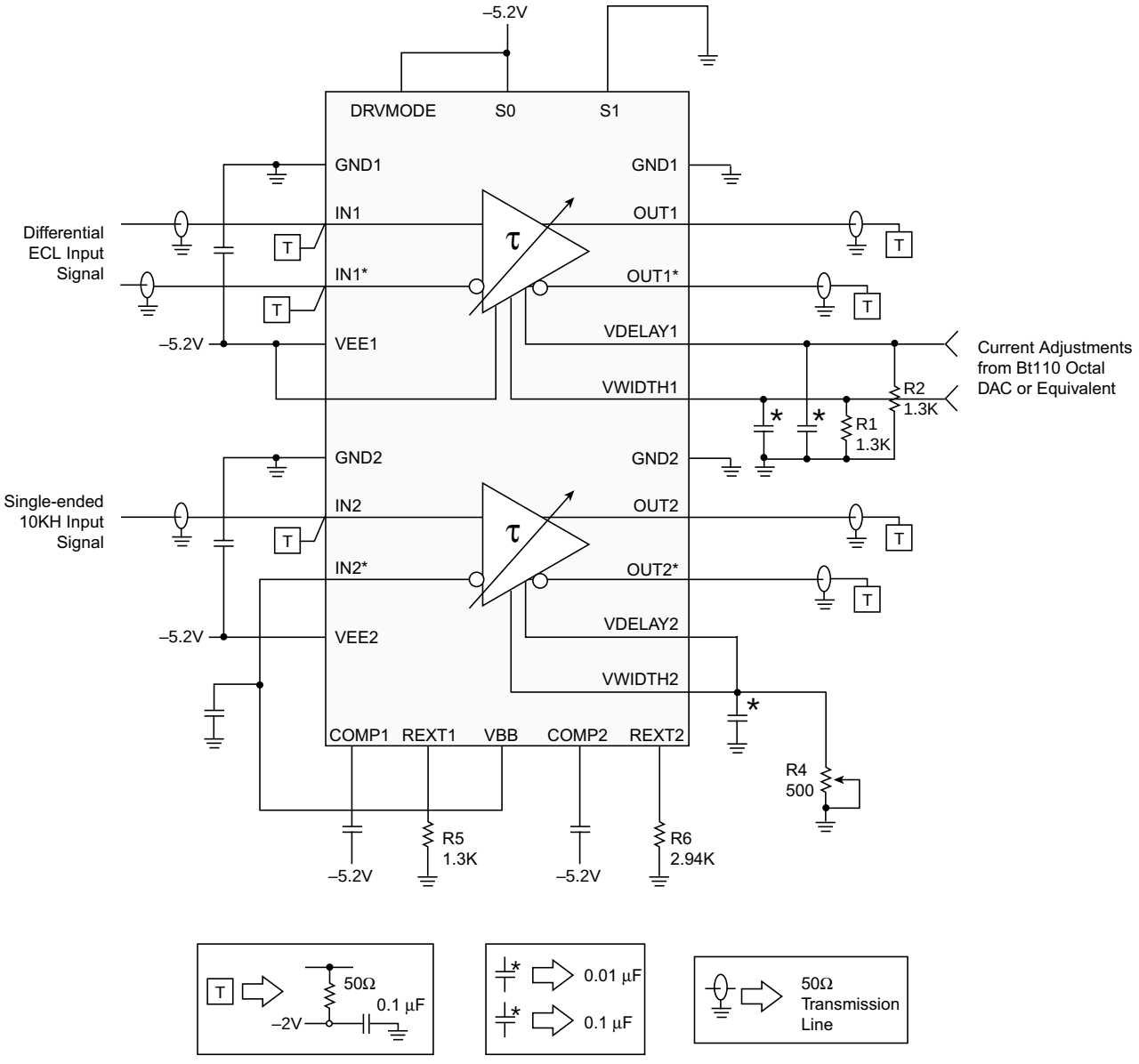


Figure 19. Edge 622 Typical Applications

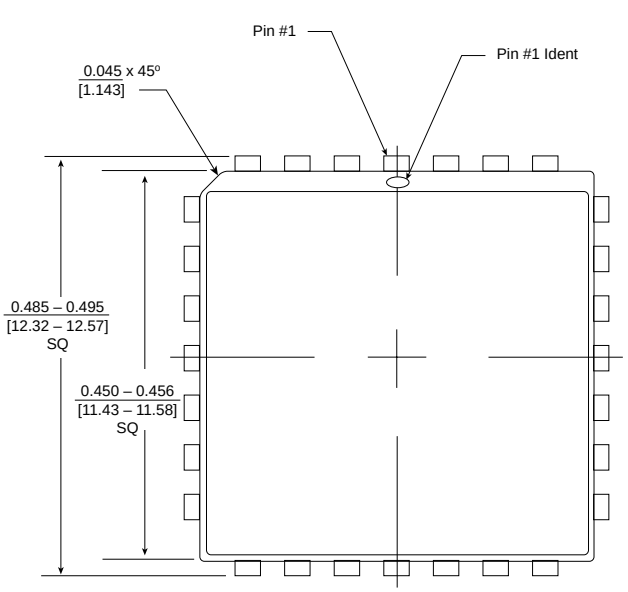
Application Information *(continued)*

Package Thermal Data

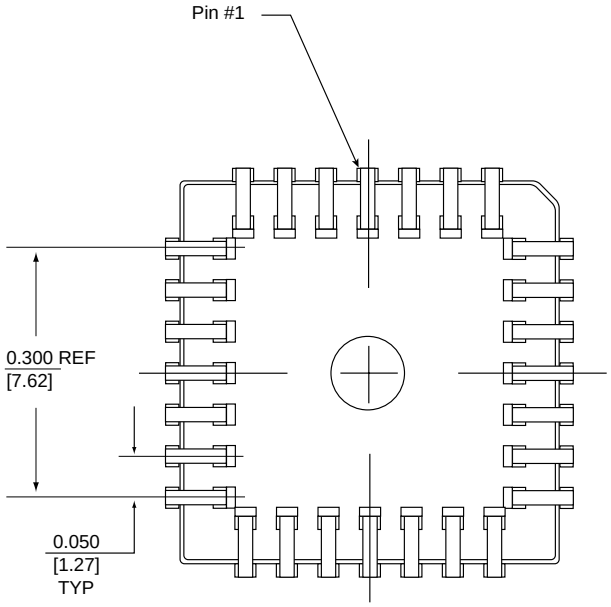
Parameter	Symbol	Min	Typ	Max	Units
Thermal Resistance					
Junction to Air					
Edge622KHJ					
Still Air	θJA		48.8		°C / W
50 LFPM of Airflow	θJA		35.5		°C / W
400 LFPM of Airflow	θJA		26.4		°C / W
Edge624KHJ	θJA				
Still Air	θJA		41		°C / W
50 LFPM of Airflow	θJA		33		°C / W
400 LFPM of Airflow			21		°C / W
Junction to Case					
Edge622KHJ	θJC		11.3		°C / W
Edge624KHJ	θJC		12.4		°C / W

Package Information

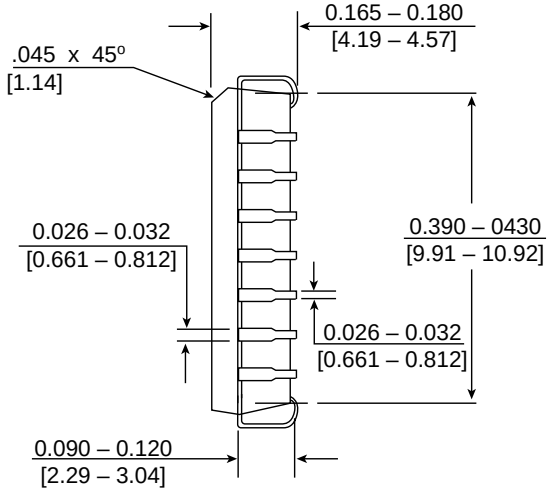
Edge622
28 Pin PLCC Package
θJA = 75 to 80˚C / W



Top View



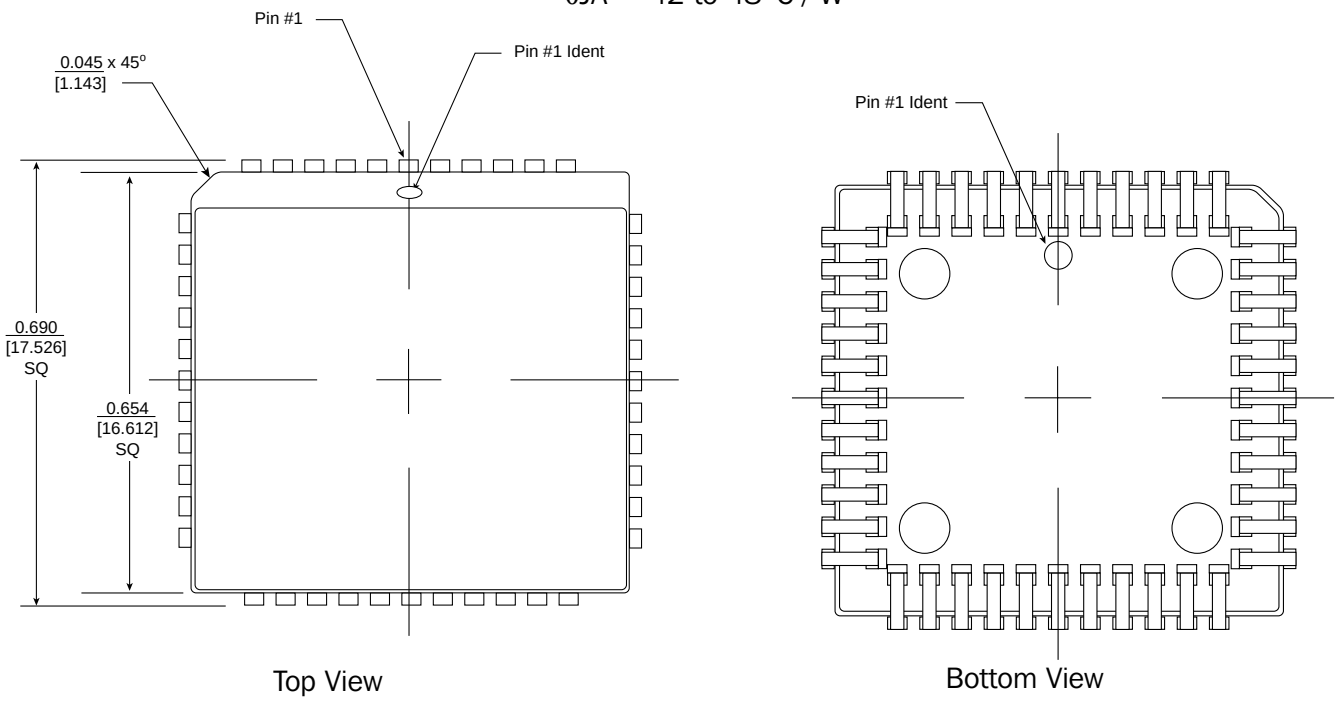
Bottom View

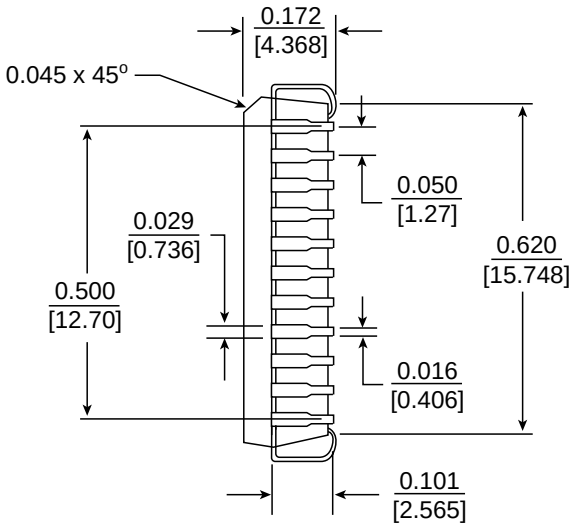


Notes: (unless otherwise specified)
1. Dimensions are in inches [millimeters].
2. Tolerances are: .XXX ± 0.005 [0.127].
3. PLCC packages are intended for surface mounting on solder lands on 0.050 [1.27] centers.

Package Information *(continued)*

Edge624
44 Pin PLCC Package
θJA = 42 to 48˚C / W





Notes: (unless otherwise specified)
1. Dimensions are in inches [millimeters].
2. Tolerances are: .XXX ± 0.005 [0.127].
3. PLCC packages are intended for surface mounting on solder lands on 0.050 [1.27] centers.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Device Ground	GND	0	0	0	V
Negative Power supply	VEE	-4.2	-5.2	-5.5	V
Ambient Operating Temperature	TA	0		+70	^{o}C

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VEE (relative to GND)		-6.0		0	V
Voltage on any Digital Pin		VEE		GND	V
Output Current		-50			mA
Ambient Operating Temperature	TA	-55		+70	^{o}C
Storage Temperature	TS	-65		+150	^{o}C
Junction Temperature	TJ			+150	^{o}C
Soldering Temperature (5 seconds, 1/4" from pin)	TA		0	+70	^{o}C

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

Parameter	Symbol	TA(°C)	Min	Typ	Max	Units
Digital Input High Voltage (Note 1)		0	-1170		-840	mV
IN, IN*	VIH	+25	-1130		-810	mV
		+70	-1070		-735	mV
Digital Input High Voltage (Note 1)		0	-1170		0	mV
DVRMODE, S0, S1	VIH	+25	-1130		0	mV
		+70	-1070		0	mV
Digital Input Low Voltage (Note 1)		0	-1950		-1480	mV
IN, IN*	VIL	+25	-1950		-1480	mV
		+70	-1950		-1450	mV
Digital Input Low Voltage (Note 1)		0	VEE		-1480	mV
DRVMODE, S0	VIL	+25	VEE		-1480	mV
		+70	VEE		-1450	mV
Digital Input Low Voltage (Note 1)		0	-2100		-1480	mV
S1	VIL	+25	-2100		-1480	mV
		+70	-2100		-1450	mV
S1 Third State (Extended Delay)		FULL	VEE		-3.2	V
		0	-1040		-760	mV
Digital Output High Voltage	VOH	+25	-1000		-730	mV
		+70	-940		-680	mV
		0	-1950		-1630	mV
Digital Output Low Voltage	VOL	+25	-1950		-1630	mV
		+70	-1950		-1600	mV
Threshold Output Voltage	VBB	FULL	-1.5	-1.35	-1.2	V
Input High Current (Vin = VIHmax)						
IN, DRVMODE, S0, S1	IIH	FULL		122	250	µA
IN*	IIH	FULL	-100			µA
Input Low Current (Vin = VILmin)						
IN, DRVMODE, S0, S1	IIL	FULL		90	150	µA
IN*	IIL	FULL	-100	-45		µA
624 Supply Current						
Mode 0	IEE	FULL		228	300	mA
Modes 1, 2		FULL		294	380	mA
Modes 3, 5		FULL		366	465	mA
622 Supply Current						
Mode 0	IEE	FULL		160	215	mA
Modes 1, 2		FULL		195	235	mA
Modes 3, 5		FULL		240	290	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with REXT1 = 1.3 KΩ, REXT2 = 2.94 KΩ, and VEE = -5.5V. All parameters specified at 0°C are guaranteed by characterization and are not production tested. The specified limits shown can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 400 linear feet per minute over the device mounted either in the test socket or on the printed circuit board.

AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Propagation Delays (Note 1)					
Minimum Delays					
MODE S1 S0 VDELAY VWIDTH					
0 0 0 -0.1V X	TPDmin	3.7	5.2	6.7	ns
1 0 1 -0.1V X	TPDmin	6.3	8.3	11.0	ns
2 1 0 -0.1V -0.1V	TPDmin	3.9	5.4	6.9	ns
3 1 1 -0.1V -0.1V	TPDmin	6.3	8.4	11.1	ns
5 VEE 1 -0.1V -0.1V	TPDmin	8.5	11.3	14.5	ns
Delay Adjustment Ranges					
MODE S1 S0 VDELAY VWIDTH					
0 0 0 -0.3V X	TPDmin	10.0	14.0	20.0	ns
1 0 1 -0.3V X	TPDmin	17.3	24.0	32.0	ns
2 1 0 -0.3V -0.3V	TPDmin	10.0	14.0	20.0	ns
3 1 1 -0.3V -0.3V	TPDmin	17.3	24.0	32.0	ns
5 VEE 1 -0.3V -0.3V	TPDmin	25.0	34.0	44.0	ns
VWIDTH Range of Adjustment (Mode 2 or 3 Only) VWIDTH = -0.1V to -1.3V		7.0	10.0	13.0	ns
Propagation Delay Tempco (Mode 2)			4		ps / ^{o}C
Output Rise/Fall Times (20% to 80%) (Note 2)	Tr, Tf	250	375	850	ps

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with TA = 25 °C with 400 LFPM of airflow, VEE = -5.5V, and all outputs terminated with 50 Ohms to –2.0 V. Timing reference points at the differential crossing points for input and output signals, REXT1 = 1.3 KOhm, and REXT2 = 2.94 KOhm. All input signals are fully differential.

Note 1: All measurements refer to both rising and falling edges for modes 0, 1, and 5, and rising edges only for modes 2 and 3. DRVMODE is logically low. Modes 2, 3, and 5 delay minimums and delay ranges are measured with VWIDTH = VDELAY.

Note 2: Based upon characterization data. Not production tested.

The specified limits shown can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 400 linear feet per minute over the device mounted either in the test socket or on the printed circuit board.

Ordering Information

Part Number	Package
E622AHJ	28-pin PLCC (with Internal Heat Spreader)
Edge622EVM	622 Evaluation Module
E624AHJ	44-pin PLCC (with Internal Heat Spreader)
Edge624EVM	624 Evaluation Module

Contact Infor mation

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