256K x 16 DRAM

5V, FAST PAGE MODE

FEATURES

- Industry-standard x16 pinouts, timing, functions and packages
- High-performance CMOS silicon-gate process
- Single +5V ±10% power supply*
- Low power, 3mW standby; 375mW active, typical
- All device pins are fully TTL-compatible
- 512-cycle refresh in 8ms (nine rows and nine columns)
- Refresh modes: $\overline{\text{RAS}}$ ONLY, $\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ (CBR) and HIDDEN
- FAST PAGE MODE access cycle
- BYTE WRITE access cycle
- BYTE READ access cycle

OPTIONS / MARKING

OPTIONS	MARKING
• Timing	
60ns access	-6*
70ns access	-7
80ns access	-8
• Packages	
Plastic SOJ (400 mil)	DJ
Plastic TSOP (400 mil)	TG

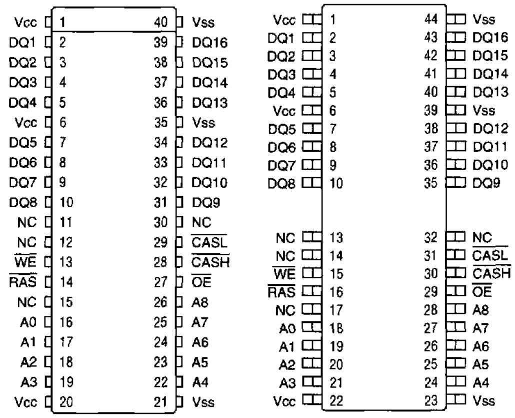
- Part Number Example: MT4C16257DJ-7

*60ns specifications are limited to a Vcc range of ±5%.

KEY TIMING PARAMETERS

SPEED	^{t}RC	^{t}RAC	^{t}PC	^{t}AA	^{t}CAC	^{t}RP
-6	110ns	60ns	35ns	30ns	15ns	40ns
-7	130ns	70ns	40ns	35ns	20ns	50ns
-8	150ns	80ns	45ns	40ns	20ns	60ns

PIN ASSIGNMENT (Top View)



40-Pin SOJ (DA-7)

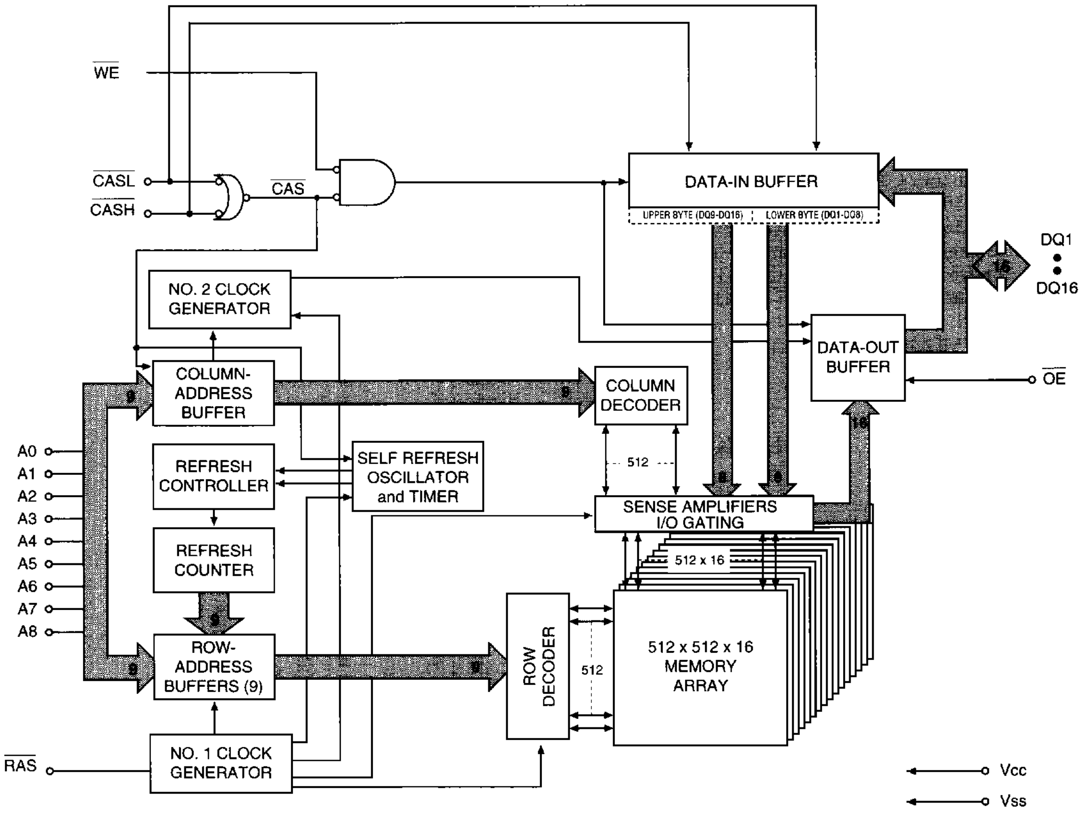
40/44-Pin TSOP (DB-4)

GENERAL DESCRIPTION

The MT4C16257 is a randomly accessed solid-state memory containing 4,194,304 bits organized in a x16 configuration. The MT4C16257 has both BYTE WRITE and WORD WRITE access cycles via two $\overline{\text{CAS}}$ pins.

The MT4C16257 $\overline{\text{CAS}}$ function and timing are determined by the first $\overline{\text{CAS}}$ ($\overline{\text{CASL}}$ or $\overline{\text{CASH}}$) to transition LOW and by the last to transition back HIGH. Use of only one of the two results in a BYTE WRITE cycle. $\overline{\text{CASL}}$ transitioning LOW selects a WRITE cycle for the lower byte (DQ1-DQ8) and $\overline{\text{CASH}}$ transitioning LOW selects a WRITE cycle for the upper byte (DQ9-DQ16). BYTE READ cycles are achieved through $\overline{\text{CASL}}$ or $\overline{\text{CASH}}$ in the same manner during READ cycles for the MT4C16257.

FUNCTIONAL BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

Each bit is uniquely addressed through the 18 address bits during READ or WRITE cycles. These are entered 9 bits (A0-A8) at a time. $\overline{\text{RAS}}$ is used to latch the first 9 bits and $\overline{\text{CAS}}$ the latter 9 bits.

The $\overline{\text{CAS}}$ control also determines whether the cycle will be a refresh cycle ($\overline{\text{RAS}}$ ONLY) or an active cycle (READ, WRITE or READ WRITE) once $\overline{\text{RAS}}$ goes LOW.

The $\overline{\text{CASL}}$ and $\overline{\text{CASH}}$ inputs internally generate a $\overline{\text{CAS}}$ signal functioning in an identical manner to the single $\overline{\text{CAS}}$ input on the other 256K x 16 DRAMs. The key difference is each $\overline{\text{CAS}}$ controls its corresponding DQ tristate logic (in conjunction with $\overline{\text{OE}}$ and $\overline{\text{WE}}$). $\overline{\text{CASL}}$ controls DQ1 through DQ8 and $\overline{\text{CASH}}$ controls DQ9 through DQ16.

The MT4C16257 $\overline{\text{CAS}}$ function is determined by the first $\overline{\text{CAS}}$ ($\overline{\text{CASL}}$ or $\overline{\text{CASH}}$) to transition LOW and the last one to transition back HIGH. The two $\overline{\text{CAS}}$ controls give the MT4C16257 both BYTE READ and BYTE WRITE cycle capabilities.

A logic HIGH on $\overline{\text{WE}}$ dictates READ mode while a logic LOW on $\overline{\text{WE}}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{\text{WE}}$ or $\overline{\text{CAS}}$, whichever occurs last. Taking $\overline{\text{WE}}$ LOW will initiate a WRITE cycle, selecting DQ1 through DQ16. If $\overline{\text{WE}}$ goes LOW prior to $\overline{\text{CAS}}$ going LOW, the output pin(s) remain open (High- Z) until the next $\overline{\text{CAS}}$ cycle. If $\overline{\text{WE}}$ goes LOW after $\overline{\text{CAS}}$ goes LOW and data reaches the output pins, data-out (Q) is activated and retains the selected cell data as long as $\overline{\text{CAS}}$ and $\overline{\text{OE}}$ remain LOW (regardless of $\overline{\text{WE}}$ or $\overline{\text{RAS}}$). This late $\overline{\text{WE}}$ pulse results in a READ WRITE cycle.

The 16 data inputs and 16 data outputs are routed through 16 pins using common I/O and pin direction is controlled by $\overline{\text{OE}}$.

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address-defined (A0-A8) page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by $\overline{\text{RAS}}$ followed by a column-address strobed-in by $\overline{\text{CAS}}$. $\overline{\text{CAS}}$ may be toggled by holding $\overline{\text{RAS}}$ LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning $\overline{\text{RAS}}$ HIGH terminates the FAST PAGE MODE operation.

Returning $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is also preconditioned for the next cycle during the $\overline{\text{RAS}}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{\text{RAS}}$ cycle (READ, WRITE) or $\overline{\text{RAS}}$ refresh cycle ($\overline{\text{RAS}}$ ONLY, CBR, or HIDDEN) so that all 512 combinations of $\overline{\text{RAS}}$ addresses (A0-A8) are executed at least every 8ms, regardless of sequence. The CBR REFRESH cycle will also invoke the refresh counter and controller for row-address control.

BYTE ACCESS CYCLE

The BYTE WRITE mode is determined by the use of $\overline{\text{CASL}}$ and $\overline{\text{CASH}}$. Enabling $\overline{\text{CASL}}$ will select a lower BYTE WRITE cycle (DQ1-DQ8) while enabling $\overline{\text{CASH}}$ will select an upper BYTE WRITE cycle (DQ9-DQ16). Enabling both $\overline{\text{CASL}}$ and $\overline{\text{CASH}}$ selects a WORD WRITE cycle.

The MT4C16257 can be viewed as two 256K x 8 DRAMS which have common input controls, with the exception of the $\overline{\text{CAS}}$ inputs. Figure 1 illustrates the MT4C16257 BYTE WRITE and WORD WRITE cycles.

The MT4C16257 also has BYTE READ and WORD READ cycles. Figure 2 illustrates the MT4C16257 BYTE READ and WORD READ cycles.

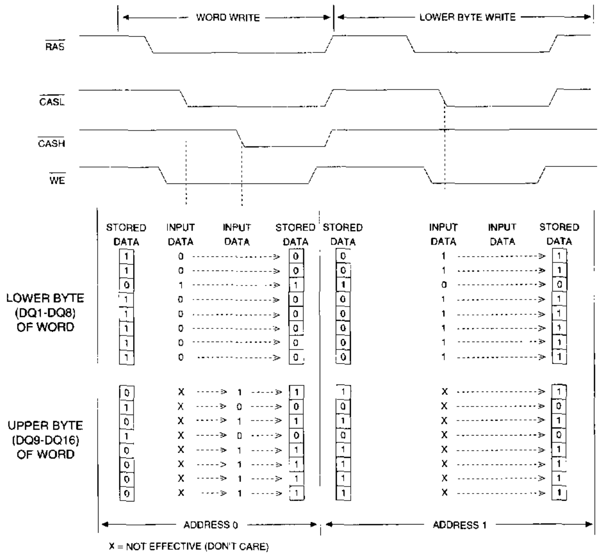


Figure 1
WORD AND BYTE WRITE EXAMPLE

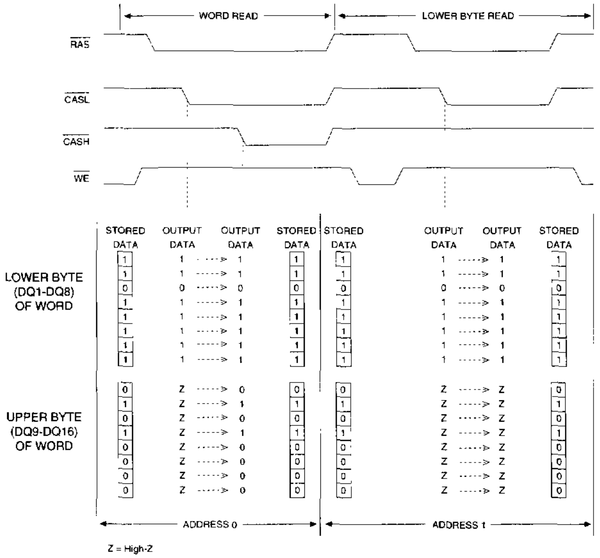


Figure 2
WORD AND BYTE READ EXAMPLE

TRUTH TABLE

FUNCTION		$\overline{\text{RAS}}$	$\overline{\text{CASL}}$	$\overline{\text{CASH}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	ADDRESSES		DQs	NOTES
							^tR	^tC		
Standby		H	H→X	H→X	X	X	X	X	High-Z	
READ: WORD		L	L	L	H	L	ROW	COL	Data-Out	
READ: LOWER BYTE		L	L	H	H	L	ROW	COL	Lower Byte, Data-Out Upper Byte, High-Z	
READ: UPPER BYTE		L	H	L	H	L	ROW	COL	Lower Byte, High-Z Upper Byte, Data-Out	
WRITE: WORD (EARLY WRITE)		L	L	L	L	X	ROW	COL	Data-In	
WRITE: LOWER BYTE (EARLY)		L	L	H	L	X	ROW	COL	Lower Byte, Data-In Upper Byte, High-Z	
WRITE: UPPER BYTE (EARLY)		L	H	L	L	X	ROW	COL	Lower Byte, High-Z Upper Byte, Data-In	
READ WRITE		L	L	L	H→L	L→H	ROW	COL	Data-Out, Data-In	1, 2
PAGE-MODE READ	1st Cycle	L	H→L	H→L	H	L	ROW	COL	Data-Out	2
	2nd Cycle	L	H→L	H→L	H	L	n/a	COL	Data-Out	2
PAGE-MODE WRITE	1st Cycle	L	H→L	H→L	L	X	ROW	COL	Data-In	1
	2nd Cycle	L	H→L	H→L	L	X	n/a	COL	Data-In	1
PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In	1, 2
	2nd Cycle	L	H→L	H→L	H→L	L→H	n/a	COL	Data-Out, Data-In	1, 2
HIDDEN REFRESH	READ	L→H→L	L	L	H	L	ROW	COL	Data-Out	2
	WRITE	L→H→L	L	L	L	X	ROW	COL	Data-In	1, 3
$\overline{\text{RAS}}$-ONLY REFRESH		L	H	H	X	X	ROW	n/a	High-Z	
CBR REFRESH		H→L	L	L	X	X	X	X	High-Z	4

NOTE:
1. These WRITE cycles may also be BYTE WRITE cycles (either $\overline{\text{CASL}}$ or $\overline{\text{CASH}}$ active).
2. These READ cycles may also be BYTE READ cycles (either $\overline{\text{CASL}}$ or $\overline{\text{CASH}}$ active).
3. EARLY WRITE only.
4. At least one of the two $\overline{\text{CAS}}$ signals must be active ($\overline{\text{CASL}}$ or $\overline{\text{CASH}}$).

Micron Technology, Inc., reserves the right to change products or specifications without notice.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} .... -1V to +7V
Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +150°C
Power Dissipation 1.2W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (V_{CC} = +5V ±10%**)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, all inputs	V_{IH}	2.4	V_{CC}+1	V	
Input Low (Logic 0) Voltage, all inputs	V_{IL}	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ V_{IN} ≤ V_{CC} (All other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V_{OUT} ≤ 5.5V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)	V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	**SYMBOL**	**-6****	**-7**	**-8**	**UNITS**	**NOTES**
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	2	2	2	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	1	1	1	mA	25
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC3}	195	175	160	mA	3, 4, 41
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC [MIN]; ^tCP, ^tASC = 10ns)	I_{CC4}	120	110	100	mA	3, 4, 41
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: ^tRC = ^tRC [MIN])	I_{CC5}	195	175	160	mA	3, 41
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC6}	180	160	140	mA	3, 5

**60ns specifications are limited to a V_{CC} range of ±5%.

CAPACITANCE

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A8	C_{I1}	5	pF	2
Input Capacitance: $\overline{\text{RAS}}$, $\overline{\text{CASL}}$, $\overline{\text{CASH}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$	C_{I2}	7	pF	2
Input/Output Capacitance: DQ (SOJ, TSOP)	C_{IO}	7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (V_{CC} = +5V ±10%*)

AC CHARACTERISTICS		-6*		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from column-address	^{t}AA		30		35		40	ns	
Column-address hold time (referenced to $\overline{\text{RAS}}$)	^{t}AR	50		55		60		ns	
Column-address setup time	^{t}ASC	0		0		0		ns	29
Row-address setup time	^{t}ASR	0		0		0		ns	
Column-address to $\overline{\text{WE}}$ delay time	^{t}AWD	55		60		65		ns	21
Access time from $\overline{\text{CAS}}$	^{t}CAC		15		20		20	ns	15, 31
Column-address hold time	^{t}CAH	10		15		15		ns	29
$\overline{\text{CAS}}$ pulse width	^{t}CAS	15	10,000	20	10,000	20	10,000	ns	37
$\overline{\text{CAS}}$ hold time (CBR REFRESH)	^{t}CHR	10		10		10		ns	5, 30
Last $\overline{\text{CAS}}$ going LOW to first $\overline{\text{CAS}}$ returning HIGH	^{t}CLCH	10		10		10		ns	32
$\overline{\text{CAS}}$ to output in Low-Z	^{t}CLZ	3		3		3		ns	31
$\overline{\text{CAS}}$ precharge time	^{t}CP	10		10		10		ns	16, 34
Access time from $\overline{\text{CAS}}$ precharge	^{t}CPA		35		40		45	ns	31
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	^{t}CRP	10		10		10		ns	30
$\overline{\text{CAS}}$ hold time	^{t}CSH	60		70		80		ns	30
$\overline{\text{CAS}}$ setup time (CBR REFRESH)	^{t}CSR	10		10		10		ns	5, 29
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ delay time	^{t}CWD	40		45		45		ns	21, 29
Write command to $\overline{\text{CAS}}$ lead time	^{t}CWL	15		20		20		ns	26, 30
Data-in hold time	^{t}DH	10		15		15		ns	22, 31
Data-in hold time (referenced to $\overline{\text{RAS}}$)	^{t}DHR	45		55		60		ns	
Data-in setup time	^{t}DS	0		0		0		ns	22, 31
Output disable time	^{t}OD	3	15	3	15	3	15	ns	28, 39
Output Enable time	^{t}OE		15		20		20	ns	31
$\overline{\text{OE}}$ hold time from $\overline{\text{WE}}$ during READ-MODIFY-WRITE cycle	^{t}OEH	15		20		20		ns	27
Output buffer turn-off delay	^{t}OFF	3	15	3	15	3	15	ns	20, 28, 31

*60ns specifications are limited to a V_{CC} range of ±5%.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = +5V ±10%*)

AC CHARACTERISTICS		-6*		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
$\overline{\text{OE}}$ setup prior to $\overline{\text{RAS}}$ during HIDDEN REFRESH cycle	^{t}ORD	0		0		0		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^{t}PC	35		40		45		ns	33
FAST-PAGE-MODE READ-WRITE cycle time	^{t}PRWC	85		95		100		ns	33
Access time from $\overline{\text{RAS}}$	^{t}RAC		60		70		80	ns	14
$\overline{\text{RAS}}$ to column-address delay time	^{t}RAD	15	30	15	35	15	40	ns	18
Row-address hold time	^{t}RAH	10		10		10		ns	
Column-address to $\overline{\text{RAS}}$ lead time	^{t}RAL	30		35		40		ns	
$\overline{\text{RAS}}$ pulse width	^{t}RAS	60	10,000	70	10,000	80	10,000	ns	
$\overline{\text{RAS}}$ pulse width (PAGE MODE)	^{t}RASP	60	100,000	70	100,000	80	100,000	ns	
Random READ or WRITE cycle time	^{t}RC	110		130		150		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	^{t}RCD	20	45	20	50	20	60	ns	17, 29
Read command hold time (referenced to $\overline{\text{CAS}}$)	^{t}RCH	0		0		0		ns	19, 26, 30
Read command setup time	^{t}RCS	0		0		0		ns	26, 29
Refresh period (512 cycles)	^{t}REF		8		8		8	ms	
$\overline{\text{RAS}}$ precharge time	^{t}RP	40		50		60		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time	^{t}RPC	10		10		10		ns	
Read command hold time (referenced to $\overline{\text{RAS}}$)	^{t}RRH	0		0		0		ns	19
$\overline{\text{RAS}}$ hold time	^{t}RSH	15		20		20		ns	38
READ WRITE cycle time	^{t}RWC	150		175		195		ns	
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ delay time	^{t}RWD	85		95		105		ns	21
Write command to $\overline{\text{RAS}}$ lead time	^{t}RWL	15		20		20		ns	26
Transition time (rise or fall)	^{t}T	3	50	3	50	3	50	ns	
Write command hold time	^{t}WCH	10		10		10		ns	26, 38
Write command hold time (referenced to $\overline{\text{RAS}}$)	^{t}WCR	45		55		60		ns	26
Write command setup time	^{t}WCS	0		0		0		ns	21, 26, 29
Write command pulse width	^{t}WP	10		10		10		ns	26

*60ns specifications are limited to a Vcc range of ±5%.

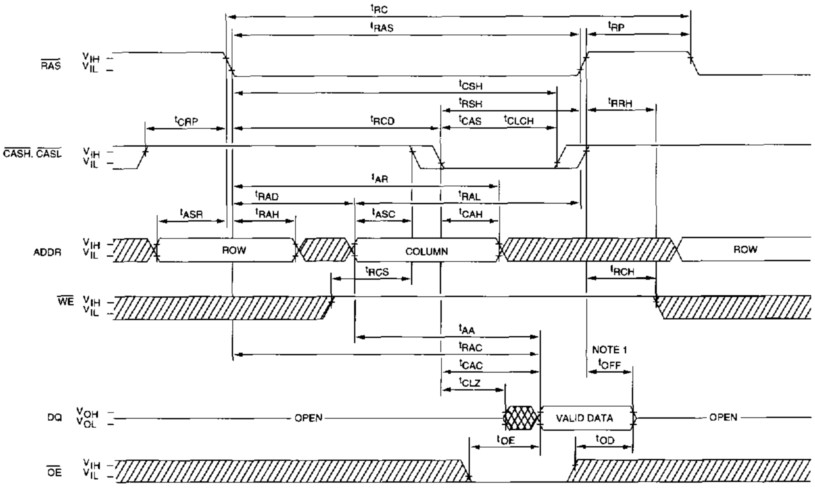
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±10%;f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{\text{RAS}}$ refresh cycles ($\overline{\text{RAS}}$ ONLY or CBR) before proper device operation is assured. The eight $\overline{\text{RAS}}$ cycle wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{\text{CAS}}$ = V_{IH}, data output is High-Z.
12. If $\overline{\text{CAS}}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates and 100pF, V_{OL} = 0.80 and V_{OH} = 2.0V.
14. Assumes that ^{t}RCD < ^{t}RCD (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that ^{t}RCD ≥ ^{t}RCD (MAX).
16. If $\overline{\text{CAS}}$ is LOW at the falling edge of $\overline{\text{RAS}}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, $\overline{\text{CAS}}$ must be pulsed HIGH for ^{t}CP.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD limit ensures that ^{t}RCD (MAX) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition; it is not a reference to V_{OH} or V_{OL}. The 3ns minimum is a parameter guaranteed by design.
21. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are restrictive operating parameters in LATE WRITE and READ-MODIFY-WRITE cycles only. If ^{t}WCS ≥ ^{t}WCS (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ^{t}RWD ≥ ^{t}RWD (MIN), ^{t}AWD ≥ ^{t}AWD (MIN) and ^{t}CWD ≥ ^{t}CWD (MIN), the cycle is a READ WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of Q (at access time and until $\overline{\text{CAS}}$ or $\overline{\text{OE}}$ goes back to V_{IH}) is indeterminate. $\overline{\text{OE}}$ held HIGH and $\overline{\text{WE}}$ taken LOW after $\overline{\text{CAS}}$ goes LOW results in a LATE WRITE ($\overline{\text{OE}}$-controlled) cycle.
22. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in EARLY WRITE cycles and $\overline{\text{WE}}$ leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
23. During a READ cycle, if $\overline{\text{OE}}$ is LOW then taken HIGH before $\overline{\text{CAS}}$ goes HIGH, Q goes open. If $\overline{\text{OE}}$ is tied permanently LOW, a LATE WRITE or READ-MODIFY-WRITE operation is not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{\text{WE}}$ = LOW and $\overline{\text{OE}}$ = HIGH.
25. All other inputs at V_{CC} -0.2V.
26. Write command is defined as $\overline{\text{WE}}$ going LOW.
27. LATE WRITE and READ-MODIFY-WRITE cycles must have both ^{t}OD and ^{t}OEH met ($\overline{\text{OE}}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously written data if $\overline{\text{CAS}}$ remains LOW and $\overline{\text{OE}}$ is taken back LOW after ^{t}OEH is met. If $\overline{\text{CAS}}$ goes HIGH prior to $\overline{\text{OE}}$ going back LOW, the DQs will remain open.
28. The DQs open during READ cycles once ^{t}OD or ^{t}OFF occur. If $\overline{\text{CAS}}$ goes HIGH before $\overline{\text{OE}}$, the DQs will open regardless of the state of the $\overline{\text{OE}}$. If $\overline{\text{CAS}}$ stays LOW while $\overline{\text{OE}}$ is brought HIGH, the DQs will open. If $\overline{\text{OE}}$ is brought back LOW ($\overline{\text{CAS}}$ still LOW), the DQs will provide the previously read data.

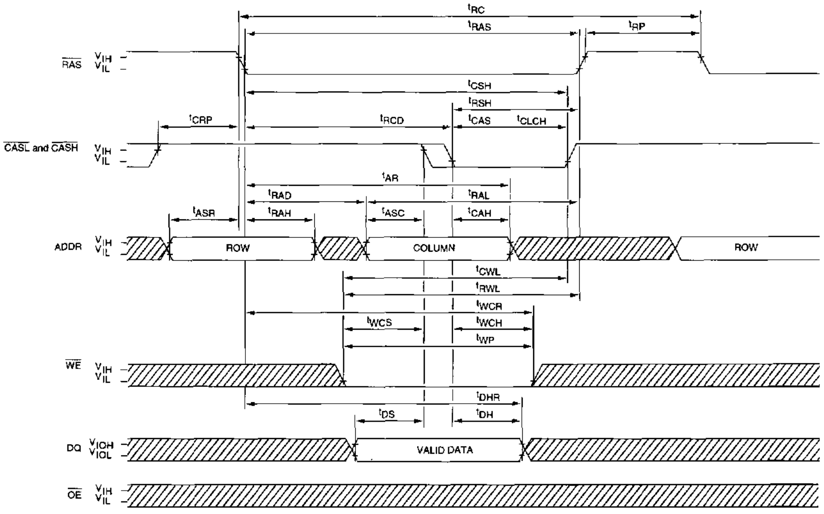
NOTES (continued)

29. The first $\overline{\text{CAS}}$x edge to transition LOW.
30. The last $\overline{\text{CAS}}$x edge to transition HIGH.
31. Output parameter (DQx) is referenced to corresponding $\overline{\text{CAS}}$ input, DQ1-DQ8 by $\overline{\text{CASL}}$ and DQ9-DQ16 by $\overline{\text{CASH}}$.
32. Last falling $\overline{\text{CAS}}$x edge to first rising $\overline{\text{CAS}}$x edge.
33. Last rising $\overline{\text{CAS}}$x edge to next cycle's last rising $\overline{\text{CAS}}$x edge.
34. Last rising $\overline{\text{CAS}}$x edge to first falling $\overline{\text{CAS}}$x edge.
35. First DQs controlled by the first $\overline{\text{CAS}}$x to go LOW.
36. Last DQs controlled by the last $\overline{\text{CAS}}$x to go HIGH.
37. Each $\overline{\text{CAS}}$x must meet minimum pulse width.
38. Last $\overline{\text{CAS}}$x to go LOW.
39. All DQs controlled, regardless $\overline{\text{CASL}}$ and $\overline{\text{CASH}}$.
40. Column-address changed once each cycle.

READ CYCLE



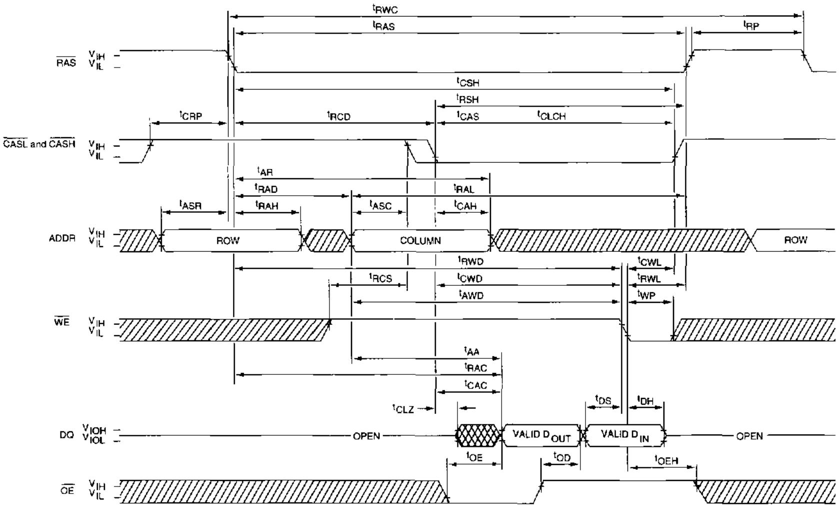
EARLY WRITE CYCLE



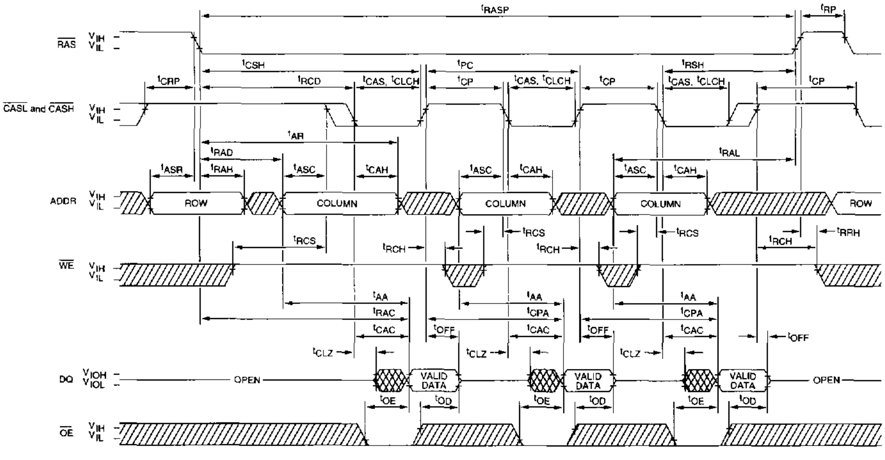
▨ DON'T CARE

▩ UNDEFINED

READ WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)



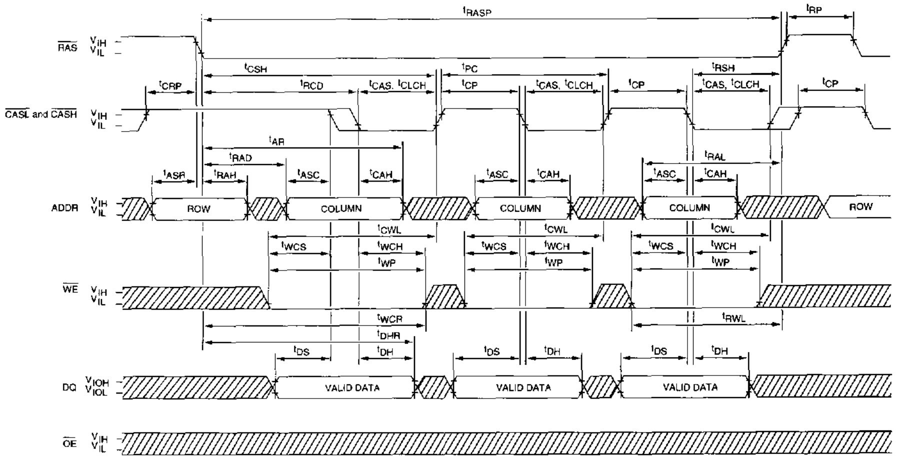
FAST-PAGE-MODE READ CYCLE



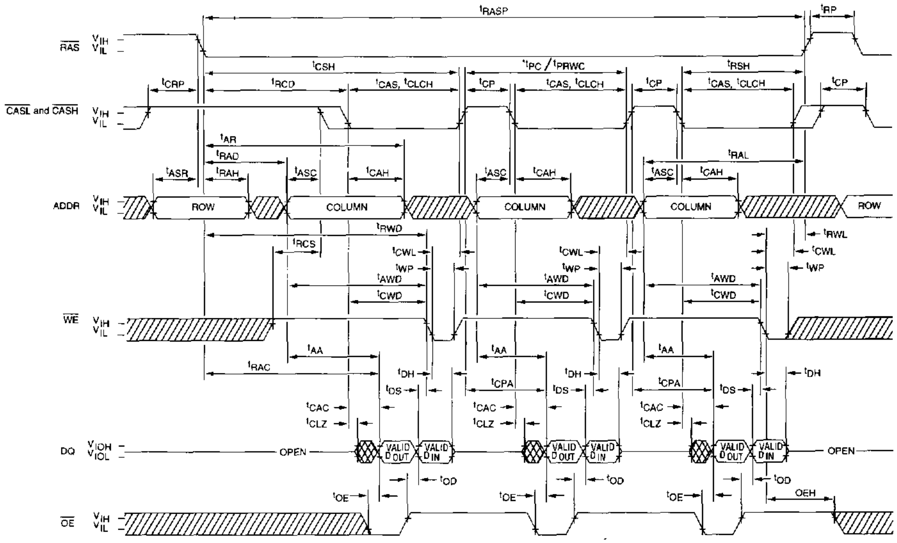
▨ DON'T CARE

▩ UNDEFINED

FAST-PAGE-MODE EARLY-WRITE CYCLE



FAST-PAGE-MODE READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)



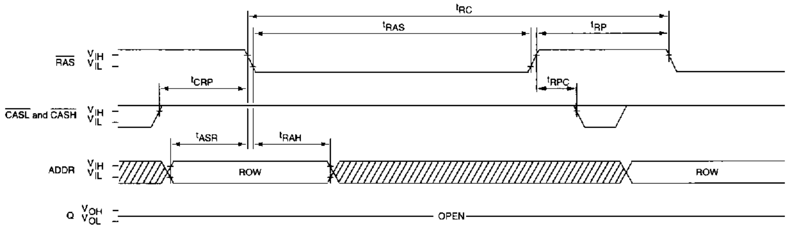
▨ DON'T CARE

▩ UNDEFINED

***NOTE:** tPC is for LATE WRITE only.

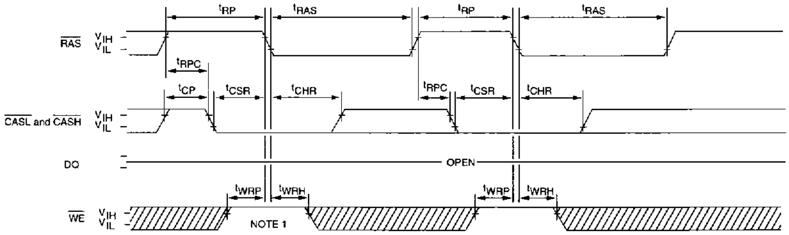
$\overline{\text{RAS}}$-ONLY REFRESH CYCLE

(Addresses; $\overline{\text{OE}}$, $\overline{\text{WE}}$ = DON'T CARE)



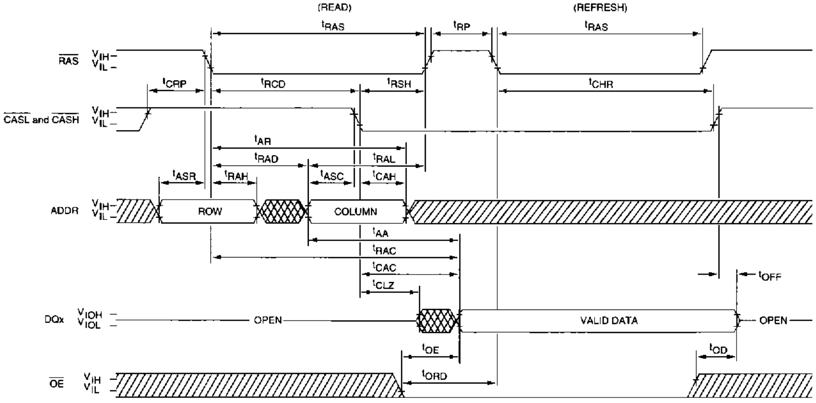
CBR REFRESH CYCLE

(Addresses and $\overline{\text{OE}}$ = DON'T CARE)



HIDDEN REFRESH CYCLE [24]

($\overline{\text{WE}}$ = HIGH; $\overline{\text{OE}}$ = LOW)



▨ DON'T CARE

▩ UNDEFINED

NOTE: 1. tWRP and tWRH are for system design reference only. The $\overline{\text{WE}}$ signal is actually a "don't care" at $\overline{\text{RAS}}$ time during a CBR REFRESH. However, $\overline{\text{WE}}$ should be held HIGH at $\overline{\text{RAS}}$ time during a CBR REFRESH to ensure compatibility with other DRAMs which require $\overline{\text{WE}}$ HIGH at $\overline{\text{RAS}}$ time during a CBR REFRESH.