

**Document Title**

**128Kx36 & 256Kx18-Bit Synchronous Pipelined Burst SRAM**

**Revision History**

| <u><b>Rev. No</b></u> | <u><b>History</b></u>                                                                                                                                                                                                                                   | <u><b>Draft Date</b></u> | <u><b>Remark</b></u> |
|-----------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------|----------------------|
| 0.0                   | Initial draft                                                                                                                                                                                                                                           | Nov . 05. 1999           | Preliminary          |
| 0.1                   | 1. Changed DC condition at Icc, ISB, ISB1 & ISB2.<br>Icc ; from 290mA to 340mA at -15,<br>from 270mA to 320mA at -14,<br><br>ISB ; from 80mA to 90mA at -15,<br>from 80mA to 90mA at -14,<br><br>ISB1 ; from 50mA to 80mA,<br>ISB2 ; from 30mA to 40mA, | April. 03. 2000          | Preliminary          |
| 0.2                   | 1. Changed input & output capacitance.<br>CIN ; from 6pF to 5pF,<br>COUT ; from 8pF to 7pF,                                                                                                                                                             | May. 15. 2000            | Preliminary          |

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The attached data sheets are prepared and approved by SAMSUNG Electronics. SAMSUNG Electronics CO., LTD. reserve the right to change the specifications. SAMSUNG Electronics will evaluate and reply to your requests and questions on the parameters of this device. If you have any questions, please contact the SAMSUNG branch office near your office, call or contact Headquarters.

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## 128Kx36 & 256Kx18-Bit Synchronous Pipelined Burst SRAM

### FEATURES

- Synchronous Operation.
- 2 Stage Pipelined operation with 4 Burst.
- On-Chip Address Counter.
- Self-Timed Write Cycle.
- On-Chip Address and Control Registers.
- $V_{DD} = 2.5V \pm 0.125V / -0.125V$  Power Supply.
- $V_{DDQ}$  Supply Voltage  $2.5V \pm 0.125V / -0.125V$ .
- Byte Writable Function.
- Global Write Enable Controls a full bus-width write.
- Power Down State via ZZ Signal.
- LBO Pin allows a choice of either a interleaved burst or a linear burst.
- Three Chip Enables for simple depth expansion with No Data Contention ; 2cycle Enable, 1cycle Disable.
- Asynchronous Output Enable Control.
- ADSP, ADSC, ADV Burst Control Pins.
- TTL-Level Three-State Output.
- 100-TQFP-1420A .

### FAST ACCESS TIMES

| PARAMETER                 | Symbol | -15 | -14 | Unit |
|---------------------------|--------|-----|-----|------|
| Cycle Time                | tCYC   | 6.7 | 7.2 | ns   |
| Clock Access Time         | tCD    | 3.8 | 4.0 | ns   |
| Output Enable Access Time | tOE    | 3.8 | 4.0 | ns   |

### GENERAL DESCRIPTION

The K7A403644A and K7A401844A are 4,718,592-bit Synchronous Static Random Access Memory designed for high performance second level cache of Pentium and Power PC based System.

It is organized as 128K(256K) words of 36(18) bits and integrates address and control registers, a 2-bit burst address counter and added some new functions for high performance cache RAM applications;  $\overline{GW}$ ,  $\overline{BW}$ ,  $\overline{LBO}$ ,  $\overline{ZZ}$ . Write cycles are internally self-timed and synchronous.

Full bus-width write is done by  $\overline{GW}$ , and each byte write is performed by the combination of  $\overline{WEx}$  and  $\overline{BW}$  when  $\overline{GW}$  is high. And with  $\overline{CS1}$  high,  $\overline{ADSP}$  is blocked to control signals.

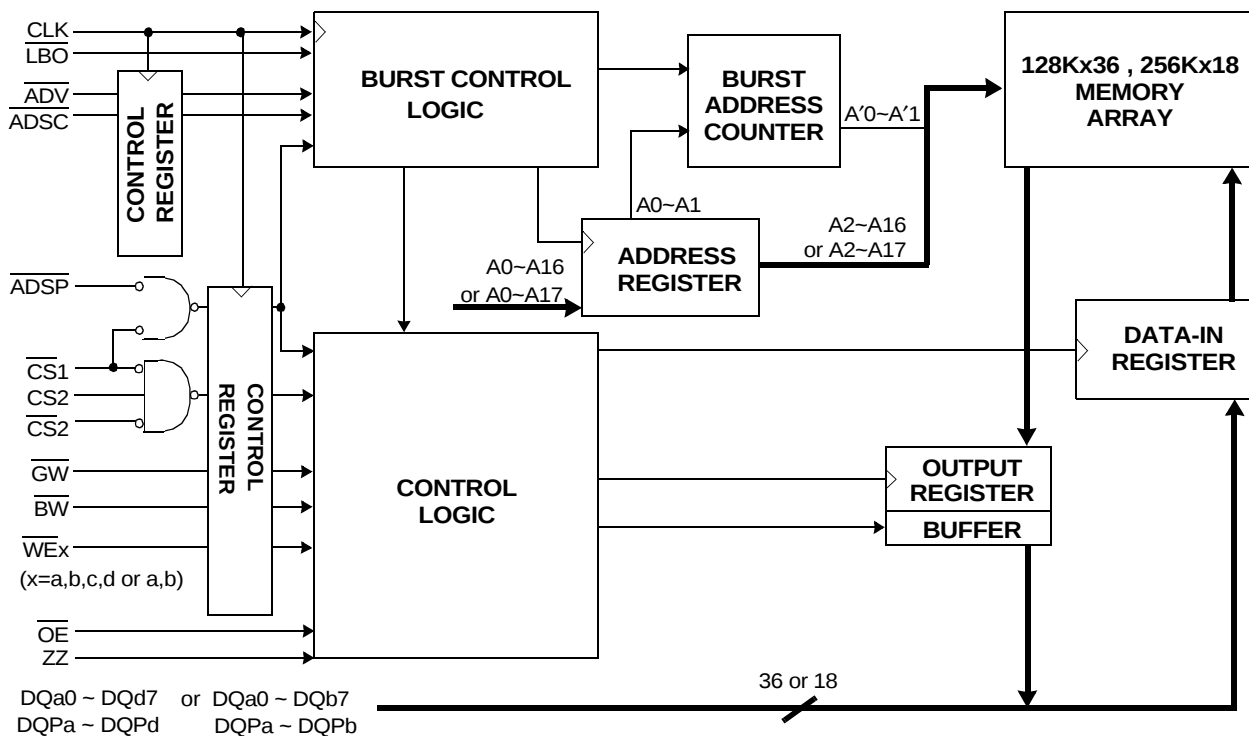
Burst cycle can be initiated with either the address status processor( $\overline{ADSP}$ ) or address status cache controller( $\overline{ADSC}$ ) inputs. Subsequent burst addresses are generated internally in the system's burst sequence and are controlled by the burst address advance( $\overline{ADV}$ ) input.

$\overline{LBO}$  pin is DC operated and determines burst sequence(linear or interleaved).

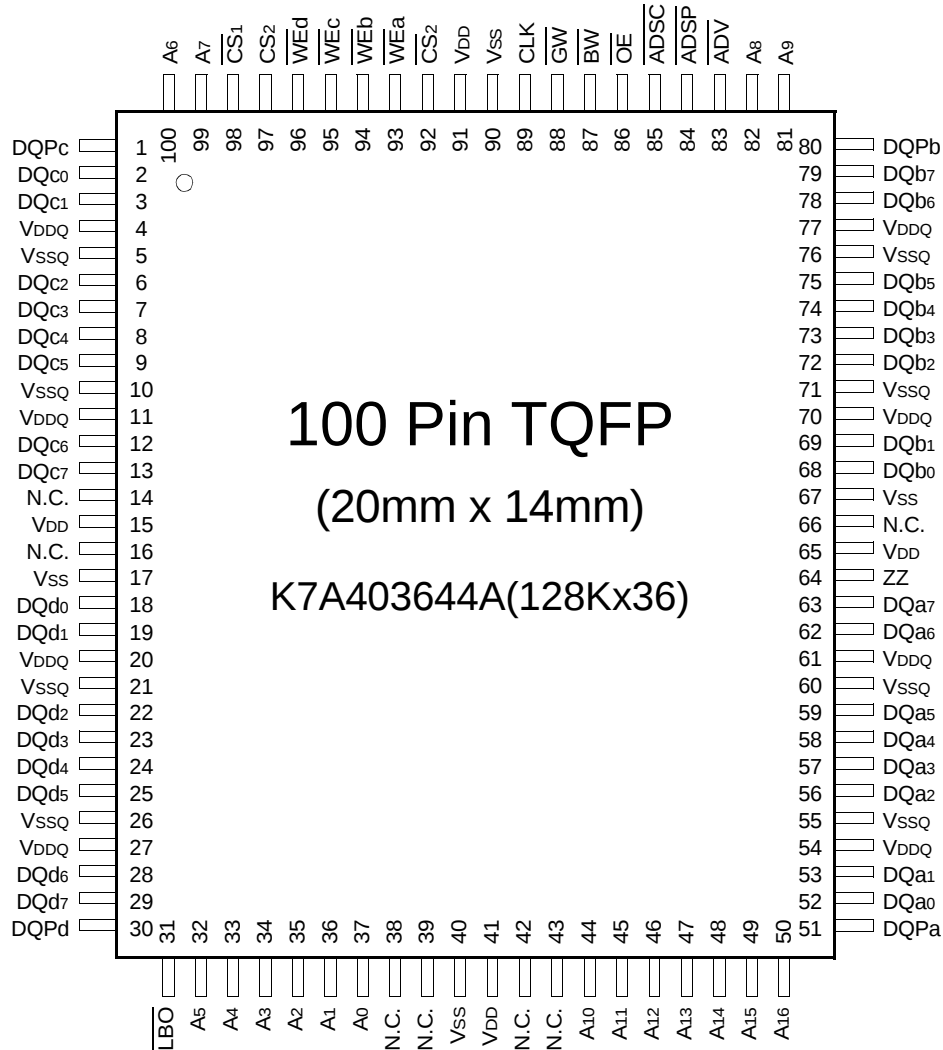
$\overline{ZZ}$  pin controls Power Down State and reduces Stand-by current regardless of CLK.

The K7A403644A and K7A401844A are fabricated using SAMSUNG's high performance CMOS technology and is available in a 100pin TQFP package. Multiple power and ground pins are utilized to minimize ground bounce.

### LOGIC BLOCK DIAGRAM



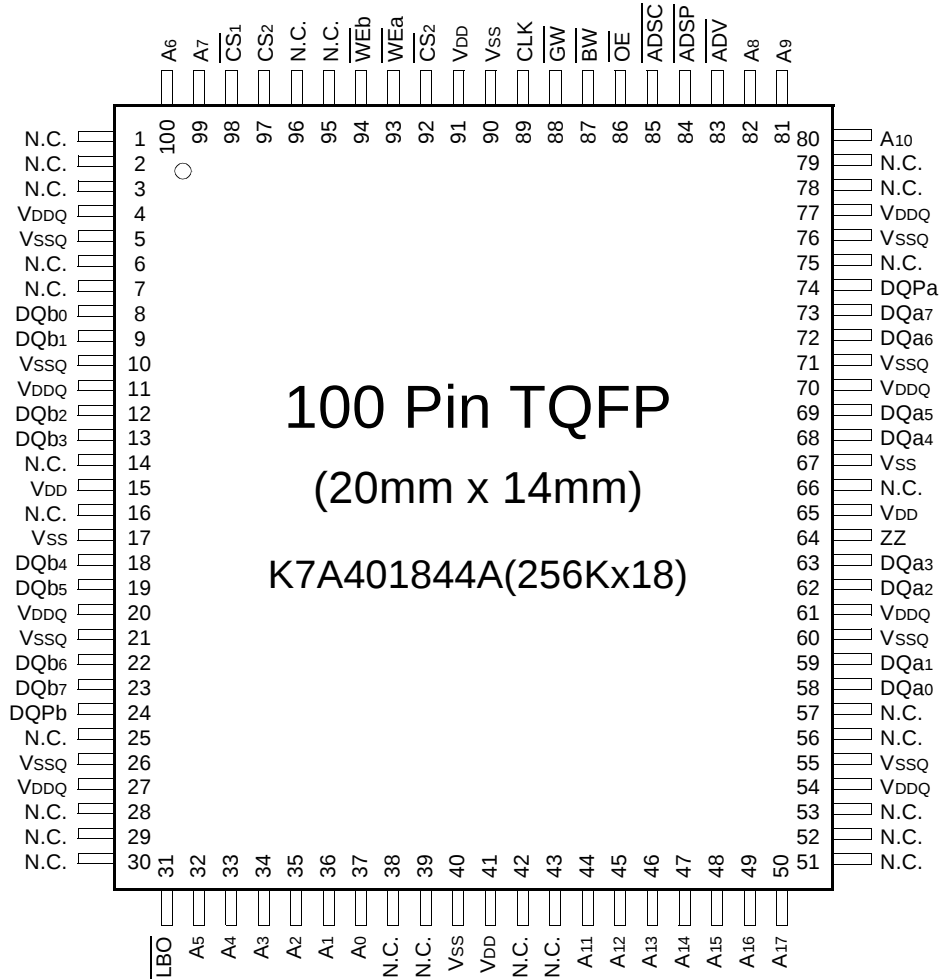
**PIN CONFIGURATION(TOP VIEW)**



**PIN NAME**

| SYMBOL      | PIN NAME                  | TQFP PIN NO.                                              | SYMBOL  | PIN NAME                   | TQFP PIN NO.            |
|-------------|---------------------------|-----------------------------------------------------------|---------|----------------------------|-------------------------|
| A0 - A16    | Address Inputs            | 32,33,34,35,36,37<br>44,45,46,47,48,49<br>50,81,82,99,100 | VDD     | Power Supply(+2.5V)        | 15,41,65,91             |
|             |                           |                                                           | VSS     | Ground                     | 17,40,67,90             |
| ADV         | Burst Address Advance     | 83                                                        | N.C.    | No Connect                 | 14,16,38,39,42,43,66    |
| ADSP        | Address Status Processor  | 84                                                        |         |                            |                         |
| ADSC        | Address Status Controller | 85                                                        | DQa0~a7 | Data Inputs/Outputs        | 52,53,56,57,58,59,62,63 |
| CLK         | Clock                     | 89                                                        | DQb0~b7 |                            | 68,69,72,73,74,75,78,79 |
| CS1         | Chip Select               | 98                                                        | DQC0~c7 |                            | 2,3,6,7,8,9,12,13       |
| CS2         | Chip Select               | 97                                                        | DQd0~d7 |                            | 18,19,22,23,24,25,28,29 |
| CS2         | Chip Select               | 92                                                        | DQPa~Pd |                            | 51,80,1,30              |
| WEx         | Byte Write Inputs         | 93,94,95,96                                               |         |                            |                         |
| (x=a,b,c,d) |                           |                                                           | VDDQ    | Output Power Supply (2.5V) | 4,11,20,27,54,61,70,77  |
| OE          | Output Enable             | 86                                                        | VSSQ    | Output Ground              | 5,10,21,26,55,60,71,76  |
| GW          | Global Write Enable       | 88                                                        |         |                            |                         |
| BW          | Byte Write Enable         | 87                                                        |         |                            |                         |
| ZZ          | Power Down Input          | 64                                                        |         |                            |                         |
| LBO         | Burst Mode Control        | 31                                                        |         |                            |                         |

**PIN CONFIGURATION(TOP VIEW)**



**PIN NAME**

| SYMBOL   | PIN NAME                  | TQFP PIN NO.                                           | SYMBOL   | PIN NAME                   | TQFP PIN NO.                                                             |
|----------|---------------------------|--------------------------------------------------------|----------|----------------------------|--------------------------------------------------------------------------|
| A0 - A17 | Address Inputs            | 32,33,34,35,36,37,44,45,46,47,48,49,50,80,81,82,99,100 | VDD      | Power Supply(+2.5V)        | 15,41,65,91                                                              |
|          |                           |                                                        | VSS      | Ground                     | 17,40,67,90                                                              |
|          |                           |                                                        | N.C.     | No Connect                 | 1,2,3,6,7,14,16,25,28,29,30,38,39,42,43,51,52,53,56,57,66,75,78,79,95,96 |
| ADV      | Burst Address Advance     | 83                                                     |          |                            |                                                                          |
| ADSP     | Address Status Processor  | 84                                                     | DQa0~a7  | Data Inputs/Outputs        | 58,59,62,63,68,69,72,73                                                  |
| ADSC     | Address Status Controller | 85                                                     | DQb0~b7  |                            | 8,9,12,13,18,19,22,23                                                    |
| CLK      | Clock                     | 89                                                     | DQPa, Pb |                            | 74,24                                                                    |
| CS1      | Chip Select               | 98                                                     | VDDQ     | Output Power Supply (2.5V) | 4,11,20,27,54,61,70,77                                                   |
| CS2      | Chip Select               | 97                                                     | VSSQ     | Output Ground              | 5,10,21,26,55,60,71,76                                                   |
| CS2      | Chip Select               | 92                                                     |          |                            |                                                                          |
| WEx      | Byte Write Inputs         | 93,94                                                  |          |                            |                                                                          |
| (x=a,b)  |                           |                                                        |          |                            |                                                                          |
| OE       | Output Enable             | 86                                                     |          |                            |                                                                          |
| GW       | Global Write Enable       | 88                                                     |          |                            |                                                                          |
| BW       | Byte Write Enable         | 87                                                     |          |                            |                                                                          |
| ZZ       | Power Down Input          | 64                                                     |          |                            |                                                                          |
| LBO      | Burst Mode Control        | 31                                                     |          |                            |                                                                          |

## FUNCTION DESCRIPTION

The K7A403644A and K7A401844A are synchronous SRAM designed to support the burst address accessing sequence of the P6 and Power PC based microprocessor. All inputs (with the exception of  $\overline{OE}$ , LBO and ZZ) are sampled on rising clock edges. The start and duration of the burst access is controlled by  $\overline{ADSC}$ ,  $\overline{ADSP}$  and  $\overline{ADV}$  and chip select pins.

The accesses are enabled with the chip select signals and output enabled signals. Wait states are inserted into the access with  $\overline{ADV}$ .

When ZZ is pulled high, the SRAM will enter a Power Down State. At this time, internal state of the SRAM is preserved. When ZZ returns to low, the SRAM normally operates after 2cycles of wake up time. ZZ pin is pulled down internally.

Read cycles are initiated with  $\overline{ADSP}$  (regardless of  $\overline{WEx}$  and  $\overline{ADSC}$ ) using the new external address clocked into the on-chip address register whenever  $\overline{ADSP}$  is sampled low, the chip selects are sampled active, and the output buffer is enabled with  $\overline{OE}$ . In read operation the data of cell array accessed by the current address, registered in the Data-out registers by the positive edge of CLK, are carried to the Data-out buffer by the next positive edge of CLK. The data, registered in the Data-out buffer, are projected to the output pins.  $\overline{ADV}$  is ignored on the clock edge that samples  $\overline{ADSP}$  asserted, but is sampled on the subsequent clock edges. The address increases internally for the next access of the burst when  $\overline{WEx}$  are sampled High and  $\overline{ADV}$  is sampled low. And  $\overline{ADSP}$  is blocked to control signals by disabling  $\overline{CS1}$ .

All byte write is done by  $\overline{GW}$  (regardless of  $\overline{BW}$  and  $\overline{WEx}$ ), and each byte write is performed by the combination of  $\overline{BW}$  and  $\overline{WEx}$  when  $\overline{GW}$  is high.

Write cycles are performed by disabling the output buffers with  $\overline{OE}$  and asserting  $\overline{WEx}$ .  $\overline{WEx}$  are ignored on the clock edge that samples  $\overline{ADSP}$  low, but are sampled on the subsequent clock edges. The output buffers are disabled when  $\overline{WEx}$  are sampled Low (regardless of  $\overline{OE}$ ). Data is clocked into the data input register when  $\overline{WEx}$  sampled Low. The address increases internally to the next address of burst, if both  $\overline{WEx}$  and  $\overline{ADV}$  are sampled Low. Individual byte write cycles are performed by any one or more byte write enable signals ( $\overline{WEa}$ ,  $\overline{WEb}$ ,  $\overline{WEc}$  or  $\overline{WEd}$ ) sampled low. The  $\overline{WEa}$  control DQa0 ~ DQa7 and DQPa,  $\overline{WEb}$  controls DQb0 ~ DQb7 and DQPb,  $\overline{WEc}$  controls DQc0 ~ DQc7 and DQPc, and  $\overline{WEd}$  control DQd0 ~ DQd7 and DQPd. Read or write cycle may also be initiated with  $\overline{ADSC}$ , instead of  $\overline{ADSP}$ . The differences between cycles initiated with  $\overline{ADSC}$  and  $\overline{ADSP}$  as are follows;

$\overline{ADSP}$  must be sampled high when  $\overline{ADSC}$  is sampled low to initiate a cycle with  $\overline{ADSC}$ .

$\overline{WEx}$  are sampled on the same clock edge that sampled  $\overline{ADSC}$  low (and  $\overline{ADSP}$  high).

Addresses are generated for the burst access as shown below. The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is determined by the state of the LBO pin. When this pin is Low, linear burst sequence is selected. When this pin is High, Interleaved burst sequence is selected.

## BURST SEQUENCE TABLE

(Interleaved Burst)

| LBO PIN                                                         | HIGH | Case 1         |                | Case 2         |                | Case 3         |                | Case 4         |                |
|-----------------------------------------------------------------|------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
|                                                                 |      | A <sub>1</sub> | A <sub>0</sub> | A <sub>1</sub> | A <sub>0</sub> | A <sub>1</sub> | A <sub>0</sub> | A <sub>1</sub> | A <sub>0</sub> |
| <div>First Address</div> <div>↓</div> <div>Fourth Address</div> |      | 0              | 0              | 0              | 1              | 1              | 0              | 1              | 1              |
|                                                                 |      | 0              | 1              | 0              | 0              | 1              | 1              | 1              | 0              |
|                                                                 |      | 1              | 0              | 1              | 1              | 0              | 0              | 0              | 1              |
|                                                                 |      | 1              | 1              | 1              | 0              | 0              | 1              | 0              | 0              |

Note : 1.  $\overline{LBO}$  pin must be tied to High or Low, and Floating State must not be allowed.

(Linear Burst)

| $\overline{\text{LBO}}$ PIN                                     | LOW | Case 1         |                | Case 2         |                | Case 3         |                | Case 4         |                |
|-----------------------------------------------------------------|-----|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
|                                                                 |     | A <sub>1</sub> | A <sub>0</sub> | A <sub>1</sub> | A <sub>0</sub> | A <sub>1</sub> | A <sub>0</sub> | A <sub>1</sub> | A <sub>0</sub> |
| <div>First Address</div> <div>↓</div> <div>Fourth Address</div> |     | 0              | 0              | 0              | 1              | 1              | 0              | 1              | 1              |
|                                                                 |     | 0              | 1              | 1              | 0              | 1              | 1              | 0              | 0              |
|                                                                 |     | 1              | 0              | 1              | 1              | 0              | 0              | 0              | 1              |
|                                                                 |     | 1              | 1              | 0              | 0              | 0              | 1              | 1              | 0              |

Note : 1.  $\overline{LBO}$  pin must be tied to High or Low, and Floating State must not be allowed.

## ASYNCHRONOUS TRUTH TABLE

(See Notes 1 and 2):

| OPERATION  | ZZ | $\overline{OE}$ | I/O STATUS  |
|------------|----|-----------------|-------------|
| Sleep Mode | H  | X               | High-Z      |
| Read       | L  | L               | DQ          |
|            | L  | H               | High-Z      |
| Write      | L  | X               | Din, High-Z |
| Deselected | L  | X               | High-Z      |

## Notes

1. X means "Don't Care".
2. ZZ pin is pulled down internally
3. For write cycles that following read cycles, the output buffers must be disabled with  $\overline{OE}$ , otherwise data bus contention will occur.
4. Sleep Mode means power down state of which stand-by current does not depend on cycle time.
5. Deselected means power down state of which stand-by current depends on cycle time.

## TRUTH TABLES

### SYNCHRONOUS TRUTH TABLE

| $\overline{CS}_1$ | $\overline{CS}_2$ | $\overline{CS}_2$ | $\overline{ADSP}$ | $\overline{ADSC}$ | $\overline{ADV}$ | $\overline{WRITE}$ | CLK | ADDRESS ACCESSED | OPERATION                  |
|-------------------|-------------------|-------------------|-------------------|-------------------|------------------|--------------------|-----|------------------|----------------------------|
| H                 | X                 | X                 | X                 | L                 | X                | X                  | ↑   | N/A              | Not Selected               |
| L                 | L                 | X                 | L                 | X                 | X                | X                  | ↑   | N/A              | Not Selected               |
| L                 | X                 | H                 | L                 | X                 | X                | X                  | ↑   | N/A              | Not Selected               |
| L                 | L                 | X                 | X                 | L                 | X                | X                  | ↑   | N/A              | Not Selected               |
| L                 | X                 | H                 | X                 | L                 | X                | X                  | ↑   | N/A              | Not Selected               |
| L                 | H                 | L                 | L                 | X                 | X                | X                  | ↑   | External Address | Begin Burst Read Cycle     |
| L                 | H                 | L                 | H                 | L                 | X                | L                  | ↑   | External Address | Begin Burst Write Cycle    |
| L                 | H                 | L                 | H                 | L                 | X                | H                  | ↑   | External Address | Begin Burst Read Cycle     |
| X                 | X                 | X                 | H                 | H                 | L                | H                  | ↑   | Next Address     | Continue Burst Read Cycle  |
| H                 | X                 | X                 | X                 | H                 | L                | H                  | ↑   | Next Address     | Continue Burst Read Cycle  |
| X                 | X                 | X                 | H                 | H                 | L                | L                  | ↑   | Next Address     | Continue Burst Write Cycle |
| H                 | X                 | X                 | X                 | H                 | L                | L                  | ↑   | Next Address     | Continue Burst Write Cycle |
| X                 | X                 | X                 | H                 | H                 | H                | H                  | ↑   | Current Address  | Suspend Burst Read Cycle   |
| H                 | X                 | X                 | X                 | H                 | H                | H                  | ↑   | Current Address  | Suspend Burst Read Cycle   |
| X                 | X                 | X                 | H                 | H                 | H                | L                  | ↑   | Current Address  | Suspend Burst Write Cycle  |
| H                 | X                 | X                 | X                 | H                 | H                | L                  | ↑   | Current Address  | Suspend Burst Write Cycle  |

- Notes :** 1. X means "Don't Care". 2. The rising edge of clock is symbolized by ↑.  
3.  $\overline{WRITE}$  = L means Write operation in WRITE TRUTH TABLE.  
 $\overline{WRITE}$  = H means Read operation in WRITE TRUTH TABLE.  
4. Operation finally depends on status of asynchronous input pins(ZZ and  $\overline{OE}$ ).

### WRITE TRUTH TABLE( x36)

| $\overline{GW}$ | $\overline{BW}$ | $\overline{WEa}$ | $\overline{WEb}$ | $\overline{WEc}$ | $\overline{WEd}$ | OPERATION          |
|-----------------|-----------------|------------------|------------------|------------------|------------------|--------------------|
| H               | H               | X                | X                | X                | X                | READ               |
| H               | L               | H                | H                | H                | H                | READ               |
| H               | L               | L                | H                | H                | H                | WRITE BYTE a       |
| H               | L               | H                | L                | H                | H                | WRITE BYTE b       |
| H               | L               | H                | H                | L                | L                | WRITE BYTE c and d |
| H               | L               | L                | L                | L                | L                | WRITE ALL BYTES    |
| L               | X               | X                | X                | X                | X                | WRITE ALL BYTES    |

- Notes :** 1. X means "Don't Care".  
2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

### WRITE TRUTH TABLE(x18)

| $\overline{GW}$ | $\overline{BW}$ | $\overline{WEa}$ | $\overline{WEb}$ | OPERATION       |
|-----------------|-----------------|------------------|------------------|-----------------|
| H               | H               | X                | X                | READ            |
| H               | L               | H                | H                | READ            |
| H               | L               | L                | H                | WRITE BYTE a    |
| H               | L               | H                | L                | WRITE BYTE b    |
| H               | L               | L                | L                | WRITE ALL BYTES |
| L               | X               | X                | X                | WRITE ALL BYTES |

- Notes :** 1. X means "Don't Care".  
2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

**PASS-THROUGH TRUTH TABLE**

| PREVIOUS CYCLE                                    |       | PRESENT CYCLE                                                |                 |       |    | NEXT CYCLE                          |
|---------------------------------------------------|-------|--------------------------------------------------------------|-----------------|-------|----|-------------------------------------|
| OPERATION                                         | WRITE | OPERATION                                                    | CS <sub>1</sub> | WRITE | OE |                                     |
| Write Cycle, All bytes<br>Address=An-1, Data=Dn-1 | All L | Initiate Read Cycle<br>Address=An<br>Data=Qn-1 for all bytes | L               | H     | L  | Read Cycle<br>Data=Qn               |
| Write Cycle, All bytes<br>Address=An-1, Data=Dn-1 | All L | No new cycle<br>Data=Qn-1 for all bytes                      | H               | H     | L  | No carryover from<br>previous cycle |
| Write Cycle, All bytes<br>Address=An-1, Data=Dn-1 | All L | No new cycle<br>Data=High-Z                                  | H               | H     | H  | No carryover from<br>previous cycle |
| Write Cycle, One byte<br>Address=An-1, Data=Dn-1  | One L | Initiate Read Cycle<br>Address=An<br>Data=Qn-1 for one byte  | L               | H     | L  | Read Cycle<br>Data=Qn               |
| Write Cycle, One byte<br>Address=An-1, Data=Dn-1  | One L | No new cycle<br>Data=Qn-1 for one byte                       | H               | H     | L  | No carryover from<br>previous cycle |

**Notes :** 1. This operation makes written data immediately available at output during a read cycle preceded by a write cycle.s

**ABSOLUTE MAXIMUM RATINGS\***

| PARAMETER                                                      | SYMBOL            | RATING                        | UNIT |
|----------------------------------------------------------------|-------------------|-------------------------------|------|
| Voltage on V <sub>DD</sub> Supply Relative to V <sub>SS</sub>  | V <sub>DD</sub>   | -0.3 to 3.6                   | V    |
| Voltage on V <sub>DDQ</sub> Supply Relative to V <sub>SS</sub> | V <sub>DDQ</sub>  | -0.3 to 3.6                   | V    |
| Voltage on Input Pin Relative to V <sub>SS</sub>               | V <sub>IN</sub>   | -0.3 to V <sub>DD</sub> +0.5  | V    |
| Voltage on I/O Pin Relative to V <sub>SS</sub>                 | V <sub>IO</sub>   | -0.3 to V <sub>DDQ</sub> +0.5 | V    |
| Power Dissipation                                              | P <sub>D</sub>    | 2.2                           | W    |
| Storage Temperature                                            | T <sub>STG</sub>  | -65 to 150                    | °C   |
| Operating Temperature                                          | T <sub>OPR</sub>  | 0 to 70                       | °C   |
| Storage Temperature Range Under Bias                           | T <sub>BIAS</sub> | -10 to 85                     | °C   |

**\*Note :** Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**OPERATING CONDITIONS (0°C ≤ T<sub>A</sub> ≤ 70°C)**

| PARAMETER      | SYMBOL           | MIN   | Typ. | MAX   | UNIT |
|----------------|------------------|-------|------|-------|------|
| Supply Voltage | V <sub>DD</sub>  | 2.375 | 2.5  | 2.625 | V    |
|                | V <sub>DDQ</sub> | 2.375 | 2.5  | 2.625 | V    |
| Ground         | V <sub>SS</sub>  | 0     | 0    | 0     | V    |

**CAPACITANCE\*(T<sub>A</sub>=25°C, f=1MHz)**

| PARAMETER          | SYMBOL           | TEST CONDITION       | MIN | MAX | UNIT |
|--------------------|------------------|----------------------|-----|-----|------|
| Input Capacitance  | C <sub>IN</sub>  | V <sub>IN</sub> =0V  | -   | 5   | pF   |
| Output Capacitance | C <sub>OUT</sub> | V <sub>OUT</sub> =0V | -   | 7   | pF   |

**\*Note :** Sampled not 100% tested.

**DC ELECTRICAL CHARACTERISTICS**( $T_A=0$  to  $70^{\circ}\text{C}$ ,  $V_{DD}=2.5\text{V}+0.125\text{V}/-0.125\text{V}$ )

| PARAMETER                        | SYMBOL | TEST CONDITIONS                                                                  |     | MIN   | MAX       | UNIT |
|----------------------------------|--------|----------------------------------------------------------------------------------|-----|-------|-----------|------|
| Input Leakage Current(except ZZ) | IIL    | VDD = Max ; VIN=VSS to VDD                                                       |     | -2    | +2        | μA   |
| Output Leakage Current           | IoL    | Output Disabled, VOUT=VSS to VDDQ                                                |     | -2    | +2        | μA   |
| Operating Current                | Icc    | Device Selected, Iout=0mA, ZZ≤VIL, All Inputs=VIL or VIH , Cycle Time ≥cyc Min   | -15 | -     | 340       | mA   |
|                                  |        |                                                                                  | -14 | -     | 320       |      |
| Standby Current                  | ISB    | Device deselected, Iout=0mA,ZZ≤VIL, f=Max, All Inputs≤0.2V or ≥ VDD-0.2V         | -15 | -     | 90        | mA   |
|                                  |        |                                                                                  | -14 | -     | 90        |      |
|                                  | ISB1   | Device deselected, Iout=0mA, ZZ≤0.2V, f = 0, All Inputs=fixed (VDD-0.2V or 0.2V) |     | -     | 80        | mA   |
|                                  | ISB2   | Device deselected, Iout=0mA, ZZ≥VDD-0.2V, f=Max, All Inputs≤VIL or ≥VIH          |     | -     | 40        | mA   |
| Output Low Voltage               | VoL    | IoL = 1.0mA                                                                      |     | -     | 0.4       | V    |
| Output High Voltage              | VoH    | IoH = -1.0mA                                                                     |     | 2.0   | -         | V    |
| Input Low Voltage                | ViL    |                                                                                  |     | -0.3* | 0.7       | V    |
| Input High Voltage               | ViH    |                                                                                  |     | 1.7   | VDD+0.5** | V    |

\* V<sub>IL</sub>(Min)=-2.0(Pulse Width ≤ tcyc/2)

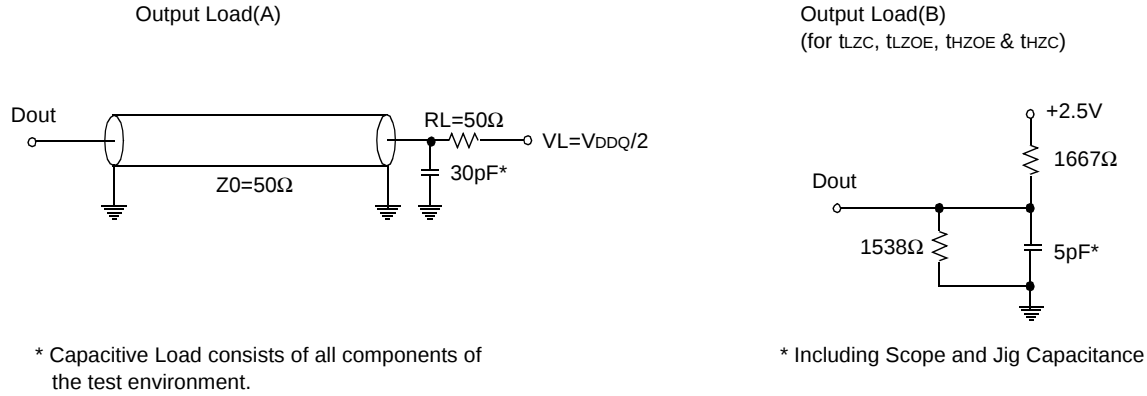
\*\* V<sub>IH</sub>(Max)=3.6(Pulse Width ≤ tcyc/2)

\*\* In Case of I/O Pins, the Max. V<sub>IH</sub>=V<sub>DDQ</sub>+0.5V

**TEST CONDITIONS**

(  $V_{DD}=2.5\text{V}+0.125\text{V}/-0.125\text{V}$ ,  $V_{DDQ}=2.5\text{V}+0.125/-0.125\text{V}$  ,  $T_A=0$  to  $70^{\circ}\text{C}$ )

| PARAMETER                                           | VALUE               |
|-----------------------------------------------------|---------------------|
| Input Pulse Level                                   | 0 to 2.5V           |
| Input Rise and Fall Time(Measured at 0.3V and 2.1V) | 1ns                 |
| Input and Output Timing Reference Levels            | V <sub>DDQ</sub> /2 |
| Output Load                                         | See Fig. 1          |



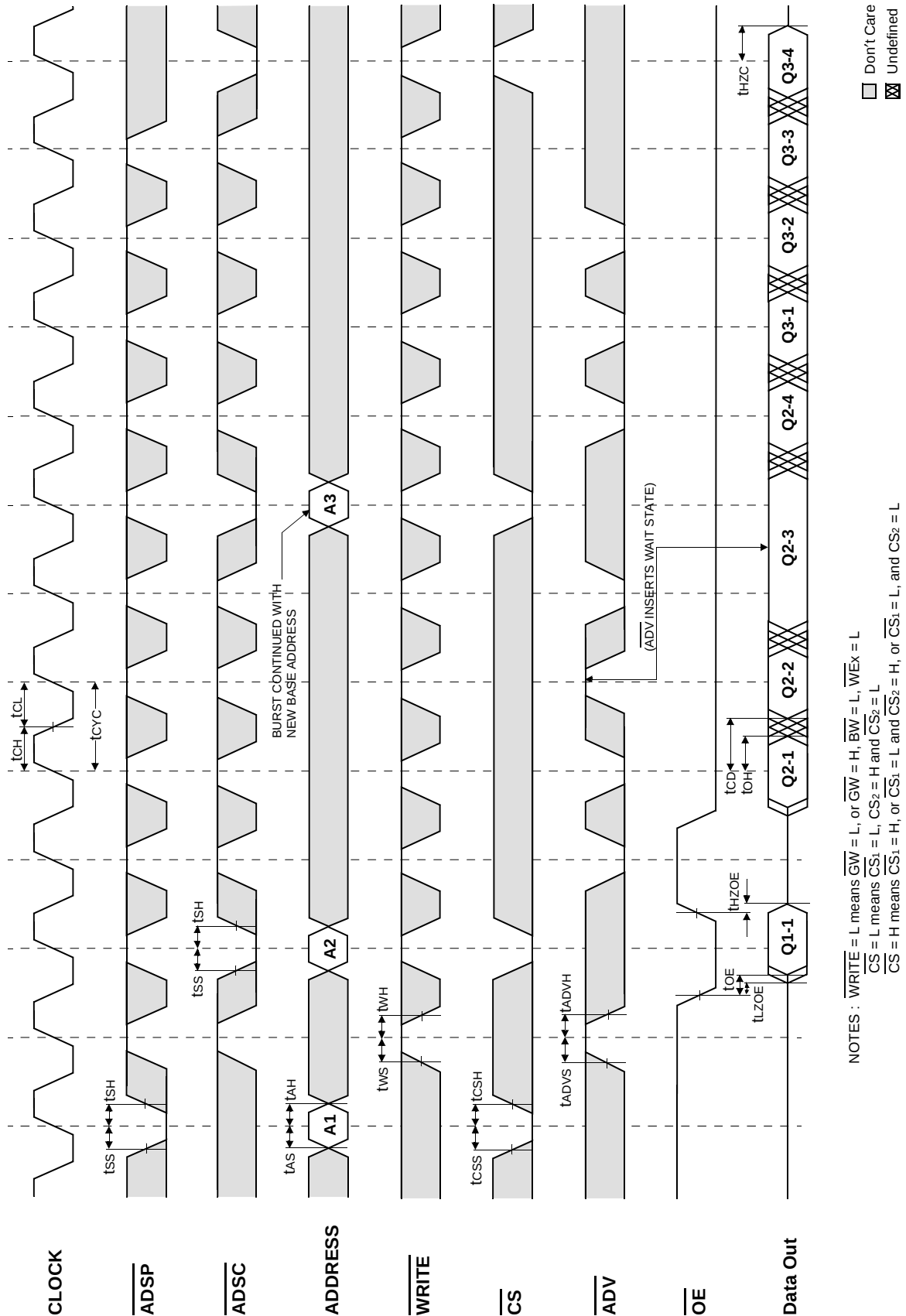
**Fig. 1**

**AC TIMING CHARACTERISTICS**( $T_A=0$  to  $70^{\circ}\text{C}$ ,  $V_{DD}=2.5\text{V}+0.125\text{V}/-0.125\text{V}$ )

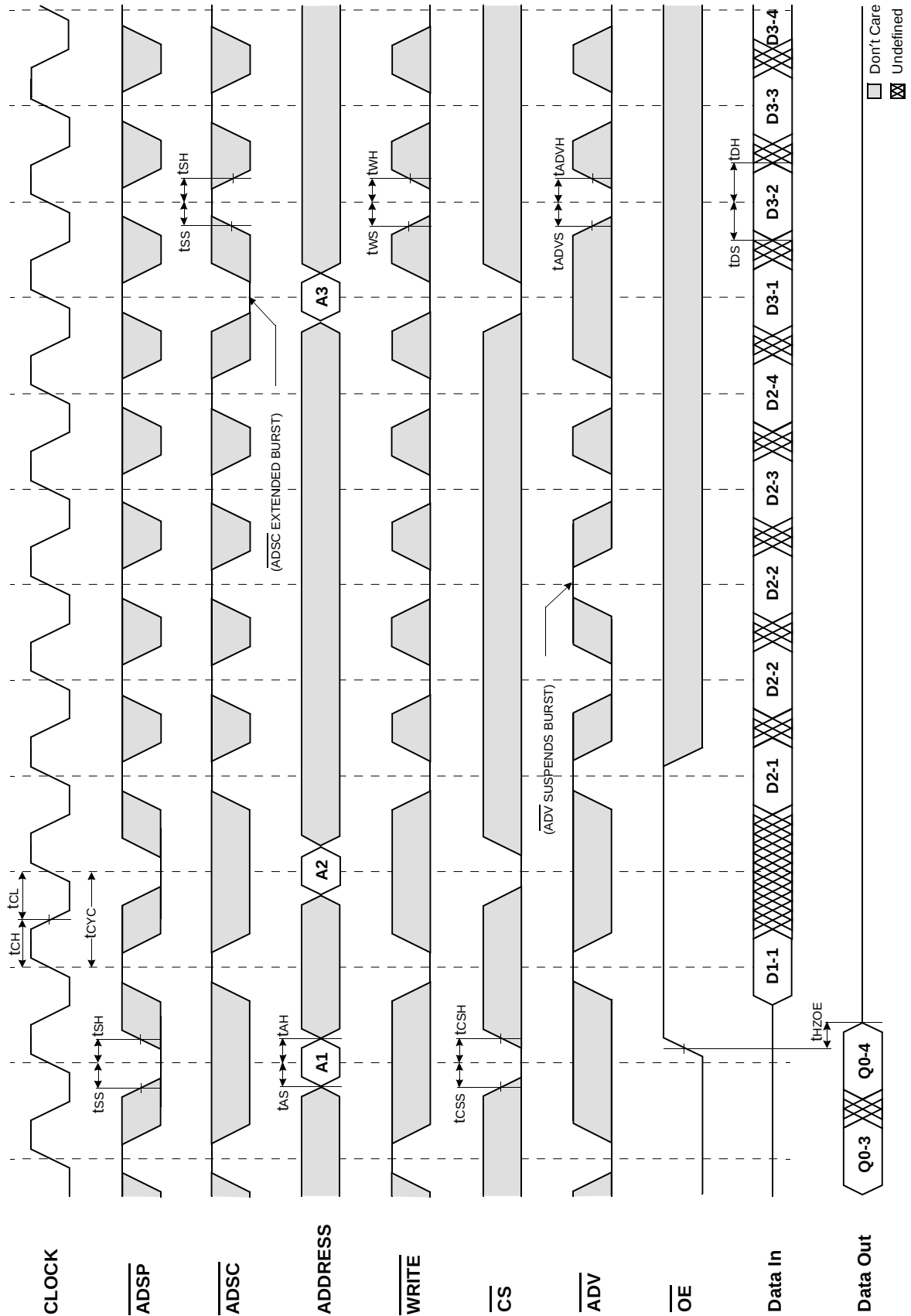
| PARAMETER                                                                                                | Symbol | -15 |     | -14 |     | UNIT  |
|----------------------------------------------------------------------------------------------------------|--------|-----|-----|-----|-----|-------|
|                                                                                                          |        | Min | Max | Min | Max |       |
| Cycle Time                                                                                               | tCYC   | 6.7 | -   | 7.2 | -   | ns    |
| Clock Access Time                                                                                        | tCD    | -   | 3.8 | -   | 4.0 | ns    |
| Output Enable to Data Valid                                                                              | tOE    | -   | 3.8 | -   | 4.0 | ns    |
| Clock High to Output Low-Z                                                                               | tLZC   | 0   | -   | 0   | -   | ns    |
| Output Hold from Clock High                                                                              | tOH    | 1.5 | -   | 1.5 | -   | ns    |
| Output Enable Low to Output Low-Z                                                                        | tLZOE  | 0   | -   | 0   | -   | ns    |
| Output Enable High to Output High-Z                                                                      | tHZOE  | -   | 3.8 | -   | 3.8 | ns    |
| Clock High to Output High-Z                                                                              | tHZC   | 1.5 | 3.8 | 1.5 | 3.8 | ns    |
| Clock High Pulse Width                                                                                   | tCH    | 2.4 | -   | 2.8 | -   | ns    |
| Clock Low Pulse Width                                                                                    | tCL    | 2.4 | -   | 2.8 | -   | ns    |
| Address Setup to Clock High                                                                              | tAS    | 1.5 | -   | 1.5 | -   | ns    |
| Address Status Setup to Clock High                                                                       | tSS    | 1.5 | -   | 1.5 | -   | ns    |
| Data Setup to Clock High                                                                                 | tDS    | 1.5 | -   | 1.5 | -   | ns    |
| Write Setup to Clock High ( $\overline{\text{GW}}$ , $\overline{\text{BW}}$ , $\overline{\text{WEX}}$ )  | tWS    | 1.5 | -   | 1.5 | -   | ns    |
| Address Advance Setup to Clock High                                                                      | tADVS  | 1.5 | -   | 1.5 | -   | ns    |
| Chip Select Setup to Clock High                                                                          | tCSS   | 1.5 | -   | 1.5 | -   | ns    |
| Address Hold from Clock High                                                                             | tAH    | 0.5 | -   | 0.5 | -   | ns    |
| Address Status Hold from Clock High                                                                      | tSH    | 0.5 | -   | 0.5 | -   | ns    |
| Data Hold from Clock High                                                                                | tDH    | 0.5 | -   | 0.5 | -   | ns    |
| Write Hold from Clock High ( $\overline{\text{GW}}$ , $\overline{\text{BW}}$ , $\overline{\text{WEX}}$ ) | tWH    | 0.5 | -   | 0.5 | -   | ns    |
| Address Advance Hold from Clock High                                                                     | tADVH  | 0.5 | -   | 0.5 | -   | ns    |
| Chip Select Hold from Clock High                                                                         | tCSH   | 0.5 | -   | 0.5 | -   | ns    |
| ZZ High to Power Down                                                                                    | tPDS   | 2   | -   | 2   | -   | cycle |
| ZZ Low to Power Up                                                                                       | tPUS   | 2   | -   | 2   | -   | cycle |

- Notes :**
1. All address inputs must meet the specified setup and hold times for all rising clock edges whenever  $\overline{\text{ADSC}}$  and/or  $\overline{\text{ADSP}}$  is sampled low and  $\overline{\text{CS}}$  is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.
  2. Both chip selects must be active whenever  $\overline{\text{ADSC}}$  or  $\overline{\text{ADSP}}$  is sampled low in order for the this device to remain enabled.
  3.  $\overline{\text{ADSC}}$  or  $\overline{\text{ADSP}}$  must not be asserted for at least 2 Clock after leaving ZZ state.

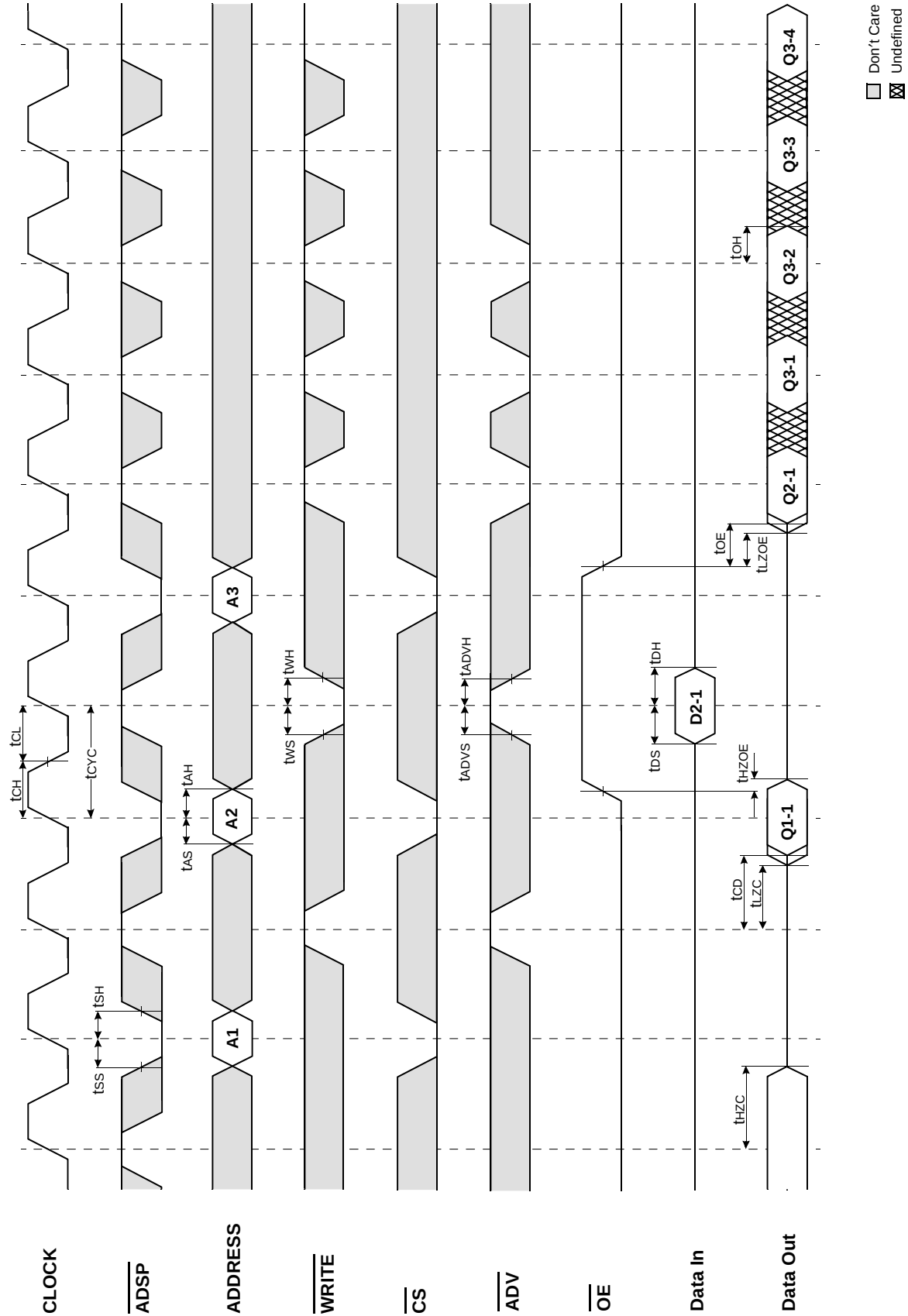
TIMING WAVEFORM OF READ CYCLE



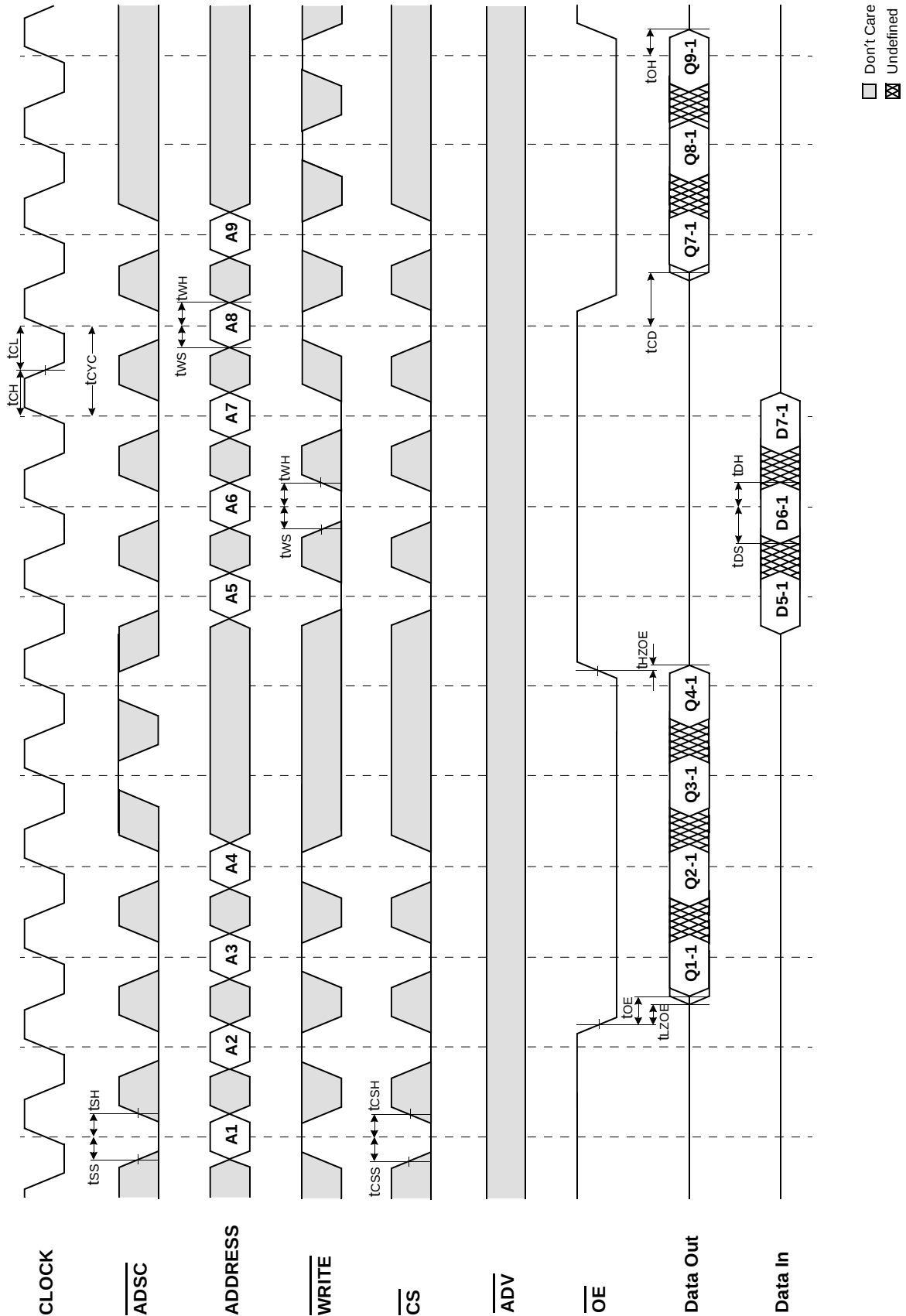
TIMING WAVEFORM OF WRTE CYCLE



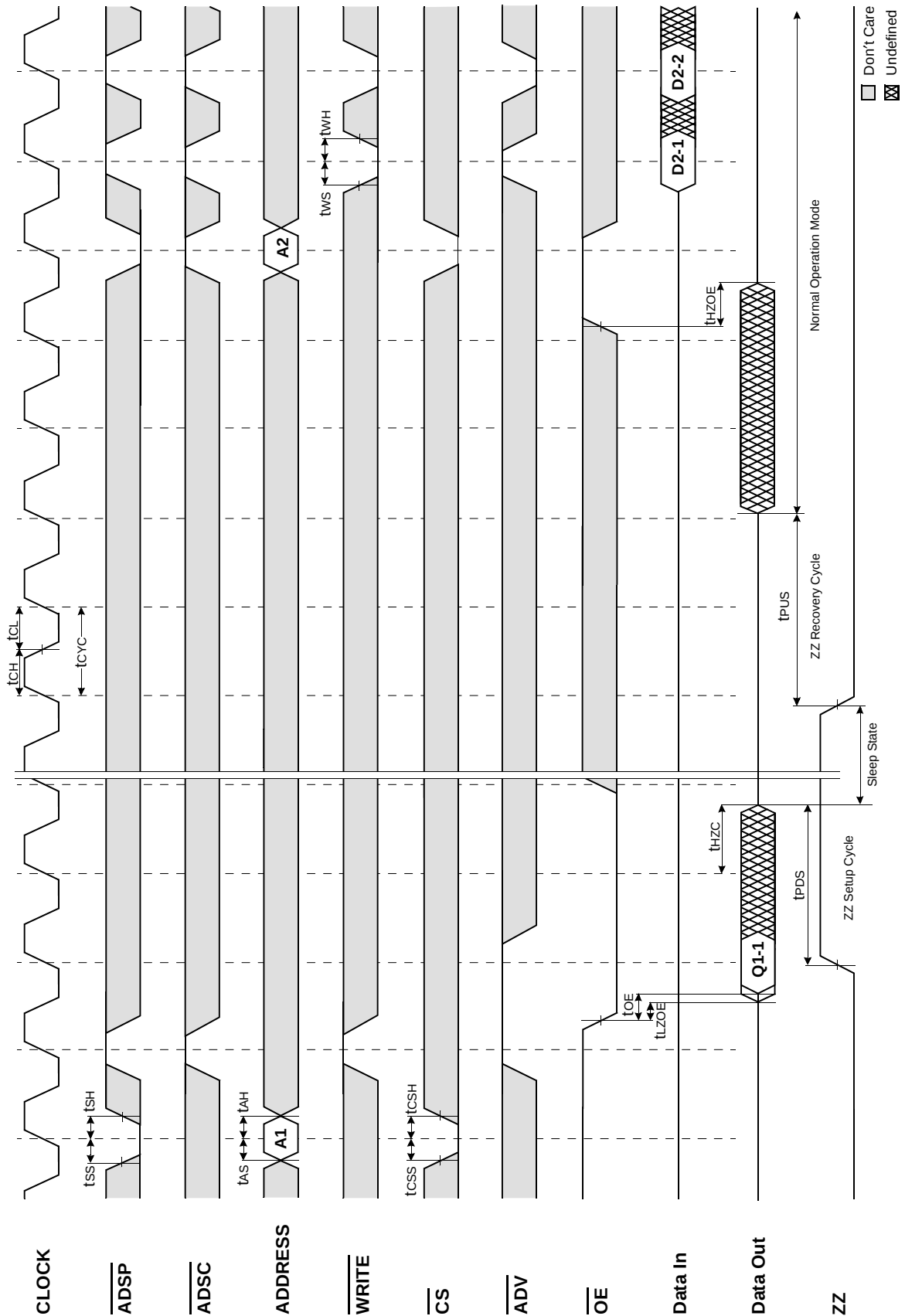
TIMING WAVEFORM OF COMBINATION READ/WRITE CYCLE(ADSP CONTROLLED , ADSC=HIGH)



TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE(ADSC CONTROLLED, ADSP=HIGH)



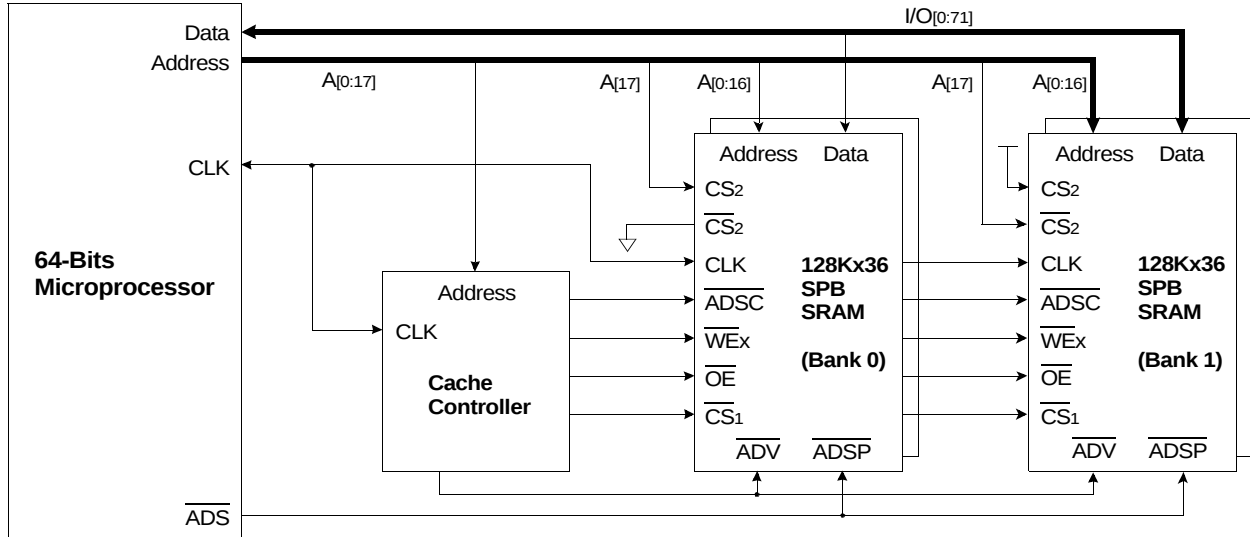
TIMING WAVEFORM OF POWER DOWN CYCLE



## APPLICATION INFORMATION

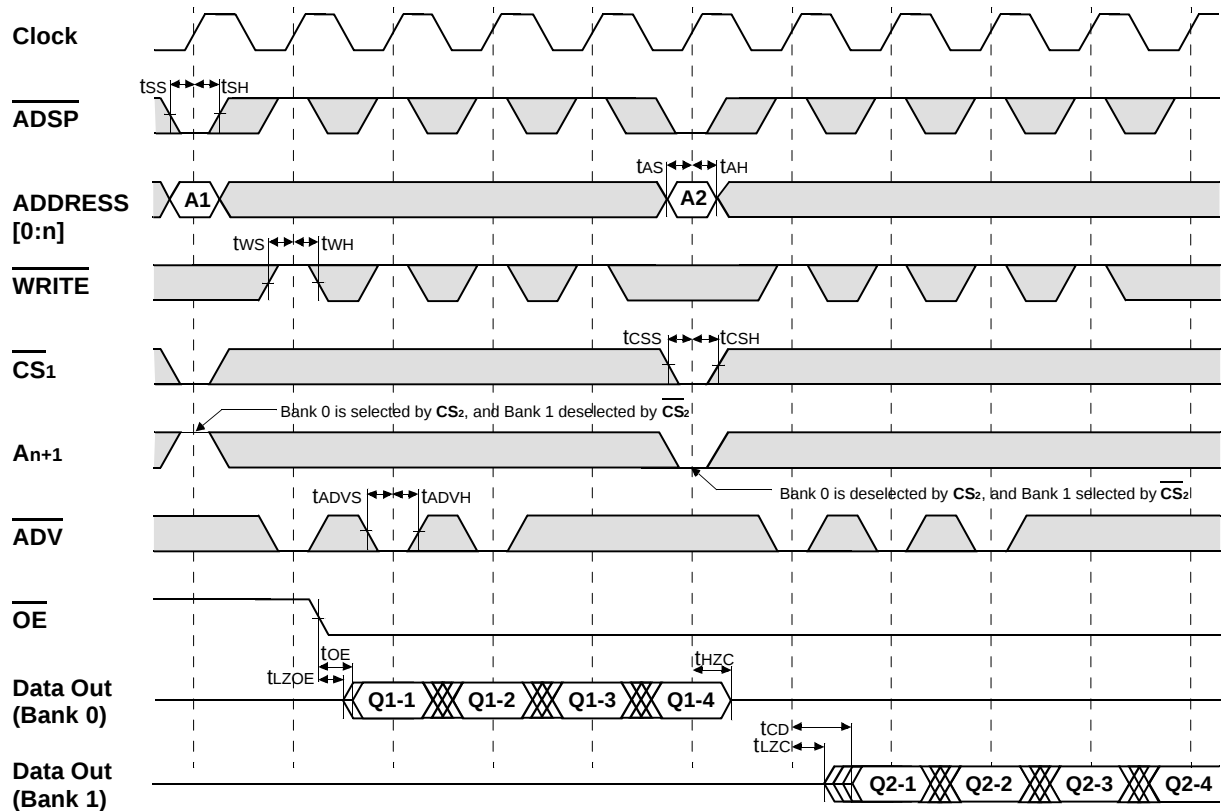
### DEPTH EXPANSION

The Samsung 128Kx36 Synchronous Pipelined Burst SRAM has two additional chip selects for simple depth expansion. This permits easy secondary cache upgrades from 128K depth to 256K depth without extra logic.



### INTERLEAVE READ TIMING (Refer to non-interleave write timing for interleave write timing)

(ADSP CONTROLLED, ADSC=HIGH)



\*Notes : n = 14 32K depth  
15 64K depth  
16 128K depth  
17 256K depth

□ Don't Care ▣ Undefined

**PACKAGE DIMENSIONS**

100-TQFP-1420A

Units ; millimeters/Inches

