Data Sheet
January 1992

AT&T Microelectronics

ATT7C183
ATT7C184

High-Speed CMOS SRAM 128 Kbit (2 x 4K x 16 or 8K x 16) Cache-Data

Features

- High-speed — 25 ns maximum access time
- Direct map or two-way set associative
- Automatic powerdown during long cycles
- Advanced CMOS technology
- Data retention at 2 V for battery backup operation
- Plug-compatible with Cypress CY7C183/184
- Low-power operation
  — Active: 700 mW typical at 45 ns
  — Standby: 75 mW typical
- Package styles available:
  — 48-pin, plastic DIP
  — 52-pin, PLCC

Description

The ATT7C183 and ATT7C184 devices are high-performance, low-power, CMOS static RAMs organized into either two two-way set associative blocks of 4K x 16 RAM or one directly mapped 8K x 16-bit RAM.

The ATT7C183 and ATT7C184 are designed specifically for use with the *Intel** 82385 Cache Controller. Addresses are latched on the falling edge of the address-latch-enable (ALE) signal. When ALE is high, the latch is transparent. The ATT7C183 has all address bits latched by the ALE signal except A12. A12, which bypasses the latch, has a faster access time. In the ATT7C184, all address bits are latched by the ALE signal. Operation is from a single 5 V power supply, and all interface signals are TTL compatible. Power consumption is 700 mW (typical) at 45 ns.

Two standby modes are available. Automatic powerdown during long cycles reduces power consumption during read accesses that are longer than the minimum access time, or when the memory is deselected and addresses do not change (are stable). In addition, data can be retained in inactive storage with a supply voltage as low as 2 V. The memory typically consumes only 9 mW at 3 V, thereby allowing effective battery backup operation.

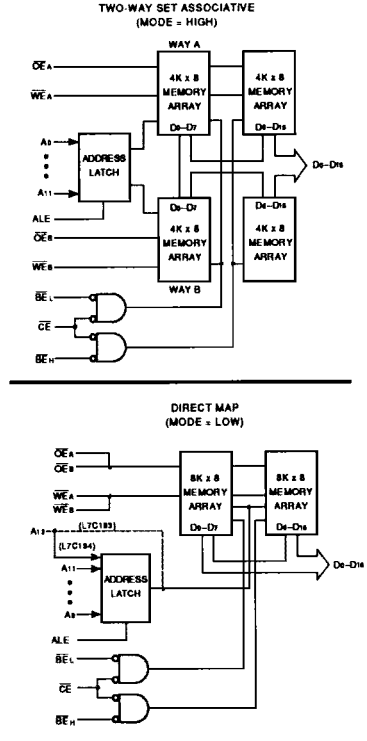


Figure 1. Block Diagram

**Intel* is a trademark of Intel Corporation.*

Pin Information

Table 1. DIP Pin Descriptions

Pin	Name/Function
A0—A12	Address
I/O0—I/O15	Data Input/Output
$\overline{CE}$	Chip Enable
$\overline{WE_A}$ and $\overline{WE_B}$	Write Enable
$\overline{OE_A}$ and $\overline{OE_B}$	Output Enable
$\overline{BE_L}$ and $\overline{BE_H}$	Bank Enable
ALE	Address Latch Enable
MODE	Configuration Mode
GND	Ground
Vcc	Power

Table 2. PLCC Pin Descriptions

Pin	Name/Function
A0—A12	Address
I/O0—I/O15	Data Input/Output
$\overline{CE}$	Chip Enable
$\overline{WE_A}$ and $\overline{WE_B}$	Write Enable
$\overline{OE_A}$ and $\overline{OE_B}$	Output Enable
$\overline{BE_L}$ and $\overline{BE_H}$	Bank Enable
ALE	Address Latch Enable
MODE	Configuration Mode
GND	Ground
Vcc	Power
NC	No Connect

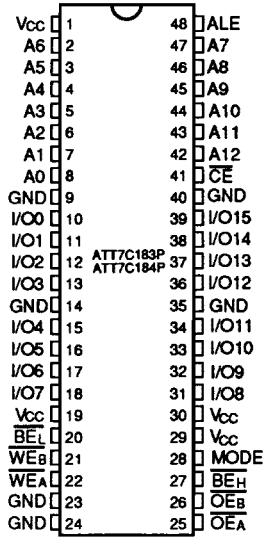


Figure 2. Pin Diagram

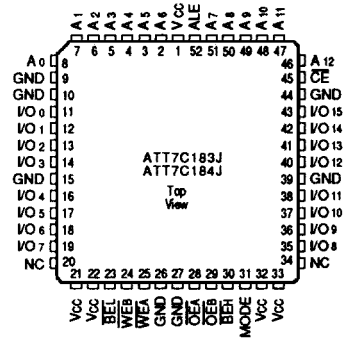


Figure 3. Pin Diagram

Functional Description

The MODE pin controls whether the ATT7C183 and ATT7C184 devices are configured as direct-mapped 8K x 16 or two-way set associative 2 x 4K x 16 RAMs. When MODE is high, the circuits are placed in the two-way mode. In the two-way mode, the upper address bit, A12, is in a don't care state and should be externally wired to ground. When MODE is low, the circuits are placed in the direct-mapped mode.

Writing is accomplished in the two-way mode by taking $\overline{CE}$ low and by inserting the respective $\overline{BEx}$ and $\overline{WEx}$ signals low. $\overline{BEL}$ enables bits D0—D7, while $\overline{BEH}$ enables bits D8—D15. $\overline{WEA}$ enables cache bank A, and $\overline{WEB}$ enables cache bank B to receive whatever data resides on the data bus. $\overline{OEA}$ and $\overline{OEB}$ similarly enable cache banks A and B, respectively, to drive the data bus.

Writing is accomplished in the direct mode by tying $\overline{WEA}$ and $\overline{WEB}$ together externally and using A12 to determine which 4K x 16 memory bank is selected.

Reading is accomplished in the two-way mode by taking $\overline{CE}$ low and inserting the respective $\overline{OEx}$ and $\overline{BEx}$ signals low and the respective $\overline{WEx}$ signal high. The contents of the memory location specified on the address pins then appear on the 16 outputs. Activation of $\overline{OEA}$ and $\overline{OEB}$ simultaneously causes both banks to be deselected.

Reading is accomplished in the direct mode by tying $\overline{OEA}$ and $\overline{OEB}$ together externally. A12 determines which 4K x 16 memory bank is enabled.

Latch-up and static discharge protection are provided on-chip. The ATT7C183 and ATT7C184 devices can withstand an injection current of up to 200 mA on any pin without damage.

Truth Table

Table 3. Truth Table — Two-Way Mode (MODE = High)

$\overline{CE}$	$\overline{BEL}$	$\overline{BEH}$	$\overline{OEA}$	$\overline{OEB}$	$\overline{WEA}$	$\overline{WEB}$	Operation
H	X	X	X	X	X	X	Outputs High-Z, Write Disabled
L	H	H	X	X	X	X	Outputs High-Z, Write Disabled
X	X	X	H	H	X	X	Outputs High-Z
X	X	X	L	L	X	X	Outputs High-Z
L	L	H	L	H	H	H	Read I/O0—I/O7, Way A
L	L	H	H	L	H	H	Read I/O0—I/O7, Way B
L	H	L	L	H	H	H	Read I/O8—I/O15, Way A
L	H	L	H	L	H	H	Read I/O8—I/O15, Way B
L	L	L	L	H	H	H	Read I/O0—I/O15, Way A
L	L	L	H	L	H	H	Read I/O0—I/O15, Way B
L	L	H	X	X	L	H	Write I/O0—I/O7, Way A
L	L	H	X	X	H	L	Write I/O0—I/O7, Way B
L	H	L	X	X	L	H	Write I/O8—I/O15, Way A
L	H	L	X	X	H	L	Write I/O8—I/O15, Way B
L	L	L	X	X	L	H	Write I/O0—I/O15, Way A
L	L	L	X	X	H	L	Write I/O0—I/O15, Way B
L	L	H	X	X	L	L	Write I/O0—I/O7, Way A and B
L	H	L	X	X	L	L	Write I/O8—I/O15, Way A and B
L	L	L	X	X	L	L	Write I/O0—I/O15, Way A and B

Functional Description (continued)

Truth Table (continued)

Table 4. Truth Table — Direct Mode (MODE = Low)

$\overline{CE}$	$\overline{BE_L}$	$\overline{BE_H}$	$\overline{OE_A}$	$\overline{OE_B}$	$\overline{WE_A}$	$\overline{WE_B}$	Operation
H	X	X	X	X	X	X	Outputs High-Z, Write Disabled
L	H	H	X	X	X	X	Outputs High-Z, Write Disabled
X	X	X	H	H	X	X	Outputs High-Z
L	L	H	L	L	H	H	Read I/O0—I/O7
L	H	L	L	L	H	H	Read I/O8—I/O15
L	L	L	L	L	H	H	Read I/O0—I/O15
L	L	H	X	X	L	L	Write I/O0—I/O7
L	H	L	X	X	L	L	Write I/O8—I/O15
L	L	L	X	X	L	L	Write I/O0—I/O15

Absolute Maximum Ratings

Stresses in excess of the Absolute Maximum Ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those indicated in the operational sections of this data sheet. Exposure to Absolute Maximum Ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min	Max	Unit
Storage Temperature	T_{stg}	−65	150	°C
Operating Ambient Temperature	T_A	−55	125	°C
Supply Voltage with Respect to Ground	V_{CC}	−0.5	7.0	V
Input Signal with Respect to Ground	—	−3.0	7.0	V
Signal Applied to High-impedance Output	—	−3.0	7.0	V
Output Current into Low Outputs	—	—	25	mA
Latch-up Current	—	>200	—	mA

Handling Precautions

The ATT7C183 and ATT7C184 devices include internal circuitry designed to protect the chips from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use to avoid exposure to excessive electrical stress.

Recommended Operating Conditions

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation	0 °C to 70 °C	4.5 V ≤ Vcc ≤ 5.5 V
Data Retention	0 °C to 70 °C	2.0 V ≤ Vcc ≤ 5.5 V

Electrical Characteristics

Over all Recommended Operating Conditions

Table 5. General Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage:						
High	V_{OH}	I_{OH} = –4.0 mA, V_{CC} = 4.5 V	2.4	—	—	V
Low	V_{OL}	I_{OL} = 8.0 mA	—	—	0.4	V
Input Voltage:						
High	V_{IH}	—	2.2	—	V_{CC} + 0.3	V
Low[1]	V_{IL}	—	–3.0	—	0.8	V
Input Current	I_{IX}	Ground ≤ V_I ≤ V_{CC}	–10	—	10	µA
Output Leakage Current	I_{OZ}	Ground ≤ V_O ≤ V_{CC}, $\overline{CE}$ = V_{CC}	–10	—	10	µA
Output Short Current	I_{OS}	V_O = Ground, V_{CC} = Max[2]	—	—	–350	mA
Vcc Current:						
Standby[3]	I_{CC2}	—	—	50	250	µA
DR Mode	I_{CC3}	V_{CC} = 3.0 V[4]	—	3.0	50	µA
Capacitance:						
Input	C_I	T_A = 25 °C, V_{CC} = 5.0 V	—	—	5	pF
Output	C_O	Test frequency = 1 MHz[5]	—	—	7	pF

1. This device provides hard clamping of transient undershoot. Input levels below ground are clamped beginning at –0.6 V. A current in excess of 100 mA is required to reach –2 V. The device can withstand indefinite operation with inputs as low as –3 V, subject only to power dissipation and bond-wire fusing constraints.
2. Duration of the output short-circuit should not exceed 30 s.
3. Tested with outputs open and all address and data inputs stable. The device is continuously disabled, i.e., $\overline{CE}$ and $\overline{BE}$ = Vcc. Input levels are within 0.2 V of Vcc or ground.
4. Data retention operation requires that Vcc never drops below 2.0 V. $\overline{CE}$ and $\overline{BE}$ must be ≥ Vcc – 0.2 V. For all other inputs, V_{IN} ≥ Vcc – 0.2 V or V_{IN} < 0.2 V is required to ensure full powerdown.
5. This parameter is not 100% tested.

Table 6. Electrical Characteristics by Speed

Parameter	Symbol	Test Conditions	Speed			Unit
			45	35	25	ns
Max Vcc Current, Active	I_{CC1}	*	170	220	300	mA

* Tested with outputs open and all address and data inputs changing at the maximum write-cycle rate. The device is continuously enabled for writing, i.e., $\overline{CE}$, $\overline{BE}$, and $\overline{WE}$ ≤ V_{IL}. Input pulse levels are 0 V to 3.0 V.
Max Icc shown applies over the active operating temperature range.

Timing Characteristics

Table 7. Read Cycle[1, 2, 3, 4]

Over all Recommended Operating Conditions; all measurements in ns. Test conditions assume input transition times of <3 ns, reference levels of 1.5 V, input pulse levels of 0 V to 3.0 V (see Figure 11), and output loading for specified I_{OL} and I_{OH} +100 pF (see Figure 10A).

Symbol	Parameter	Speed					
		45		35		25	
		Min	Max	Min	Max	Min	Max
tLHLH	Read-cycle Time	45	—	35	—	25	—
tADVDOV	Address Valid to Data Valid, A0—A11[5]	—	45	—	35	—	25
tADVDOV-A12	Address Valid to Data Valid, A12[5]	—	35	—	25	—	17
tLHDOX	ALE High to Output Change	3	—	3	—	3	—
tADXDOX	Address Change to Data Output Change	3	—	3	—	3	—
tCELDOV	Chip Enable Low to Output Valid[5, 7]	—	20	—	15	—	12
tBELDOV	Byte Enable Low to Output Valid[5, 7]	—	20	—	15	—	12
tOELDOV	Output Enable Low to Output Valid[5, 7, 8]	—	16	—	14	—	10
tCELDOZ	Chip Enable Low to Output Low-Z[8, 9]	3	—	3	—	3	—
tBELDOZ	Byte Enable Low to Output Low-Z[8, 9]	3	—	3	—	3	—
tOELDOZ	Output Enable Low to Output Low-Z[8, 9]	0	—	0	—	0	—
tCEHDOZ	Chip Enable High to Output High-Z[8, 9]	—	12	—	10	—	8
tBEHDOZ	Byte Enable High to Output High-Z[8, 9]	—	12	—	10	—	8
tOEHDOZ	Output Enable High to Output High-Z[8, 9]	—	12	—	10	—	8
tLHLL	ALE Pulse Width	—	12	—	10	—	8
tADVLL	Address Valid to ALE Low	6	—	6	—	4	—
tOEBL — tOEAH	$\overline{OE_A}$, $\overline{OE_B}$ Overlap Time[8]	0	—	0	—	0	—
tCELICH, tBELICH	$\overline{CE}$, $\overline{BEx}$ Low to Powerup[10, 11]	0	—	0	—	0	—
tLLADX	ALE Low to Address Change	4	—	4	—	4	—
tICHICL	Powerup to Powerdown[10, 11]	—	45	—	35	—	25

1. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. For example, tADVWEH (Table 8) is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.
2. All address timings are referenced from the last valid address line to the first transitioning address line.
3. $\overline{CE}$, $\overline{BE}$, and $\overline{WE}$ must be high during address transitions.
4. This product is a very high-speed device, and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high-inductance leads that cause supply bounce must be avoided by bringing the Vcc and ground planes directly up to the contactor fingers. A 0.01 µF high-frequency capacitor is also required between Vcc and ground. To avoid signal reflections, proper terminations must be used.
5. $\overline{WE}$ is high for the read cycle.
6. During this state, the chip is continuously selected ($\overline{CE}$ and $\overline{BE}$ low).
7. All address lines are valid prior to the $\overline{CE}$ and $\overline{BE}$ transition to active.
8. At any given temperature and voltage condition, output-disable time is less than output-enable time for any given device.
9. Transition is measured ±200 mV from steady-state voltage with specified loading in Figure 11B. This parameter is sampled and not 100% tested.
10. This parameter is not 100% tested.
11. Powerup from I_{CC2} to I_{CC1} occurs as a result of any of the following conditions: (1) falling edge of $\overline{CE}$, $\overline{BE}$, (2) falling edge of $\overline{WE}$ ($\overline{CE}$ and $\overline{BE}$ active), (3) transition on any address line ($\overline{CE}$ and $\overline{BE}$ active), and (4) transition on any data line ($\overline{CE}$, $\overline{BE}$, and $\overline{WE}$ active). The device automatically powers down from I_{CC1} to I_{CC2} after tICHICL has elapsed from any of the prior conditions. Power dissipation is dependent only on cycle rate, not on chip-select pulse width.

Timing Characteristics (continued)

Table 8. Write Cycle[1, 2, 3, 4]

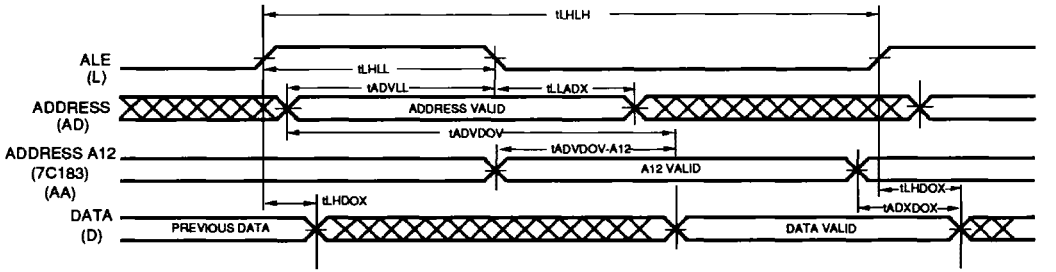
Over all Recommended Operating Conditions; all measurements in ns. Test conditions assume input transition times of <3 ns, reference levels of 1.5 V, input pulse levels of 0 V to 3.0 V (see Figure 11), and output loading for specified I_{OL} and I_{OH} +30 pF (see Figure 10A).

Symbol	Parameter	Speed					
		45		35		25	
		Min	Max	Min	Max	Min	Max
tLHLH	Write-cycle Time	45	—	35	—	25	—
tCELWEH, tCELCEH	Chip Enable Low to End of Write	30	—	20	—	13	—
tBELWEH	Byte Enable Low to End of Write	30	—	20	—	13	—
tADVWEL, tADVCEL	Address Valid to Beginning of Write	0	—	0	—	0	—
tADVWEH, tADVCEH	Address Valid to End of Write	30	—	20	—	13	—
tWELWEH	Write Enable Pulse Width	30	—	20	—	13	—
tDIVWEH, tDIVCEH	Data Change to End of Write	15	—	10	—	10	—
tWEHDIX, tCEHDIX	End of Write to Data Change	0	—	0	—	0	—
tWEHDOZ	Write Enable High to Output Low-Z[5, 6]	0	—	0	—	0	—
tWELDOZ	Write Enable Low to Output High-Z[5, 6]	—	12	—	10	—	8
tLHLL	ALE Pulse Width	12	—	10	—	8	—
tADVLL	Address Change to ALE Low	6	—	6	—	4	—
tCEHVCL	Chip Enable High to Data Retention[7]	0	—	0	—	0	—
tBEHVCL	Byte Enable High to Data Retention[7]	0	—	0	—	0	—
tVCHCEL	End Data Retention to Beginning of Read Cycle	45	—	35	—	25	—
tOEHDOZ	Output Enable High to Output High-Z	—	12	—	10	—	8
tOELDOZ	Output Enable Low to Output Low-Z	0	—	0	—	0	—

1. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. For example, tADVWEH is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.
2. All address timings are referenced from the last valid address line to the first transitioning address line.
3. $\overline{CE}$, $\overline{BE}$, or $\overline{WE}$ must be high during address transitions.
4. This product is a very high-speed device, and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high-inductance leads that cause supply bounce must be avoided by bringing the Vcc and ground planes directly up to the contactor fingers. A 0.01 µF high-frequency capacitor is also required between Vcc and ground. To avoid signal reflections, proper terminations must be used.
5. At any given temperature and voltage condition, output-disable time is less than output-enable time for any given device.
6. Transition is measured ±200 mV from steady-state voltage with specified loading in Figure 11B. This parameter is sampled and not 100% tested.
7. This parameter is not 100% tested.

Timing Characteristics (continued)

Timing Diagrams

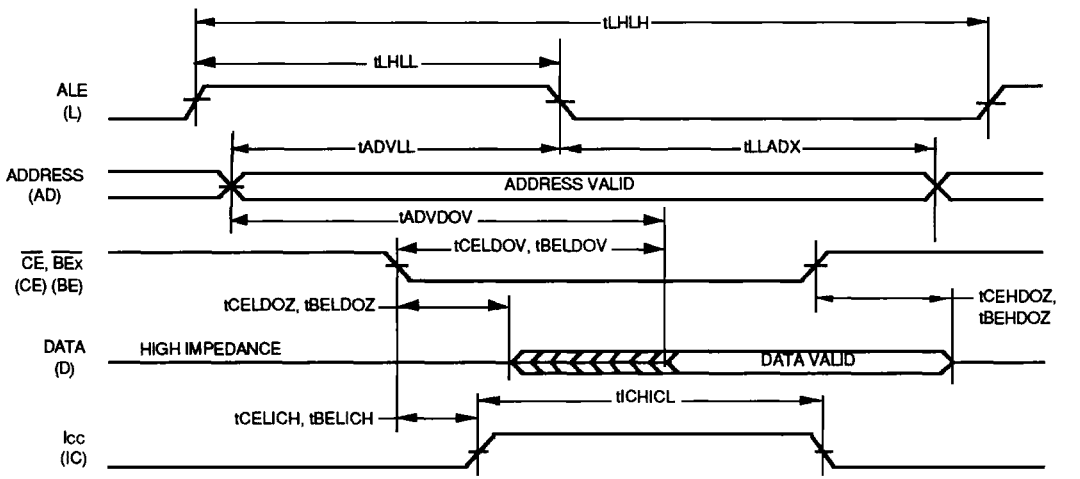


Notes:
$\overline{WE}$ is high for the read cycle.

All address lines are valid prior to or coincident with the $\overline{CE}$, $\overline{BE}$ transition to low.

$\overline{OE}$ is low during the read cycle.

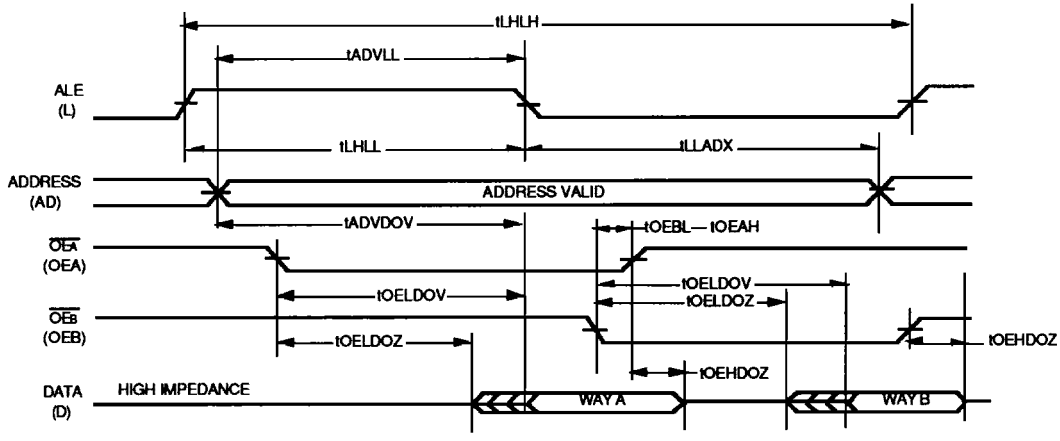
Figure 4. Read Cycle — ALE-Controlled
(See Table 7, Note 6.)



Note: $\overline{OE}$ is low during the read cycle.

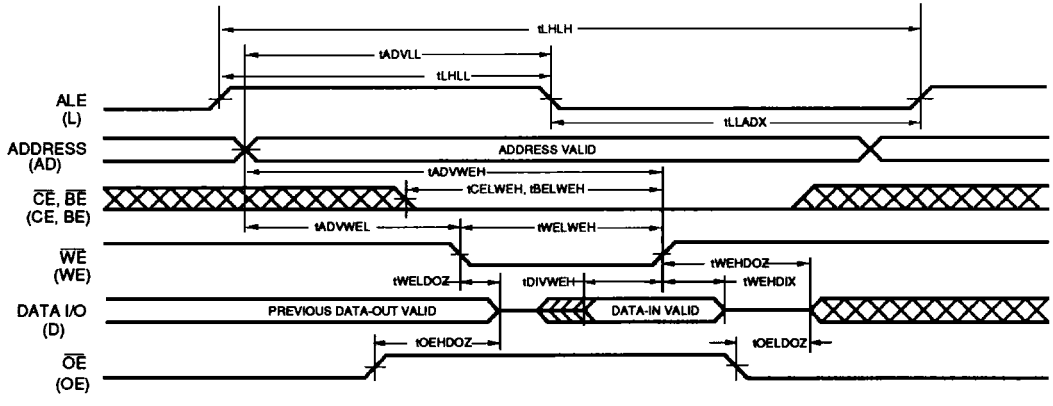
Figure 5. Read Cycle — $\overline{CE}$, $\overline{BEx}$ -Controlled

Timing Characteristics (continued)



Note: $\overline{CE}$ is low continuously during this read cycle.

Figure 6. Read Cycle — $\overline{OE}$-Controlled
(See Table 7, Note 6.)



Notes:
The internal write cycle of the memory is defined by the overlap of $\overline{CE}$, $\overline{BE}$ low, and $\overline{WE}$ low. All signals must be low to initiate a write. Any signal can terminate a write by going high. The data input setup and hold times should be referred to the rising edge of the signal that terminates the write.

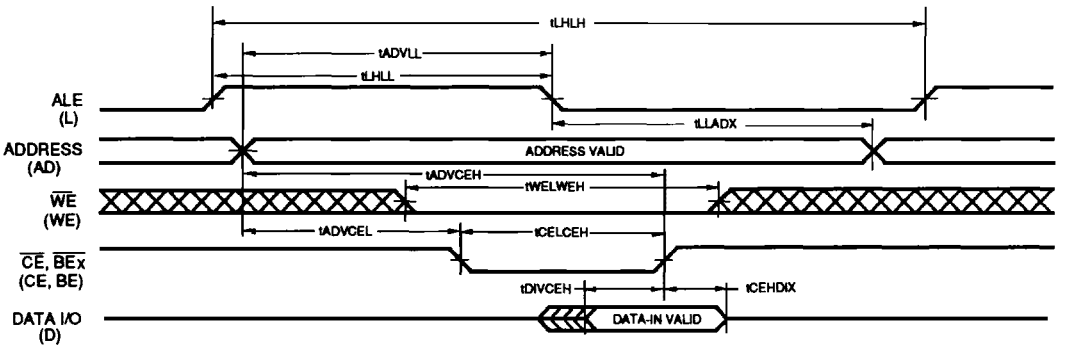
If $\overline{WE}$ goes low before or concurrent with $\overline{CE}$, $\overline{BE}$ going low, the output remains in a high-impedance state.

If $\overline{CE}$, $\overline{BE}$ goes high before or concurrent with $\overline{WE}$ going high, the output remains in a high-impedance state.

Powerup from I_{CC2} to I_{CC1} occurs as a result of any of the following conditions: (1) falling edge of $\overline{CE}$, $\overline{BE}$, (2) falling edge of $\overline{WE}$ ($\overline{CE}$ and $\overline{BE}$ active), (3) transition on any address line ($\overline{CE}$ and $\overline{BE}$ active), and (4) transition on any data line ($\overline{CE}$, $\overline{BE}$, and $\overline{WE}$ active). The device automatically powers down from I_{CC1} to I_{CC2} after t_{ICHICL} has elapsed from any of the prior conditions. Power dissipation is dependent only on cycle rate, not on chip-select pulse width.

Figure 7. Write Cycle — $\overline{WE}$-Controlled

Timing Characteristics (continued)



Notes:
The internal write cycle of the memory is defined by the overlap of $\overline{CE}$, $\overline{BE}$ low, and $\overline{WE}$ low. All signals must be low to initiate a write. Any signal can terminate a write by going high. The data input setup and hold times should be referred to the rising edge of the signal that terminates the write.

If $\overline{WE}$ goes low before or concurrent with $\overline{CE}$, $\overline{BE}$ going low, the output remains in a high-impedance state.

If $\overline{CE}$, $\overline{BE}$ goes high before or concurrent with $\overline{WE}$ going high, the output remains in a high-impedance state.

Powerup from I_{CC2} to I_{CC1} occurs as a result of any of the following conditions: (1) falling edge of $\overline{CE}$, $\overline{BE}$, (2) falling edge of $\overline{WE}$ ($\overline{CE}$ and $\overline{BE}$ active), (3) transition on any address line ($\overline{CE}$ and $\overline{BE}$ active), and (4) transition on any data line ($\overline{CE}$, $\overline{BE}$, and $\overline{WE}$ active). The device automatically powers down from I_{CC1} to I_{CC2} after tICHICL has elapsed from any of the prior conditions. Power dissipation is dependent only on cycle rate, not on chip-select pulse width.

Figure 8. Write Cycle — $\overline{CE}$-Controlled

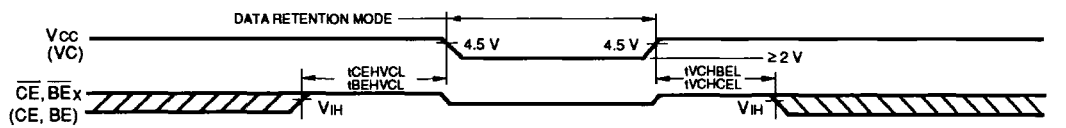


Figure 9. Data Retention

Timing Characteristics (continued)

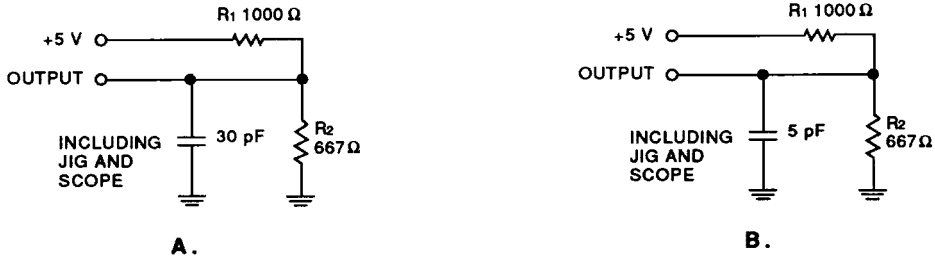


Figure 10. Test Loads

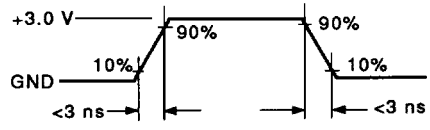


Figure 11. Transition Times

Application Information

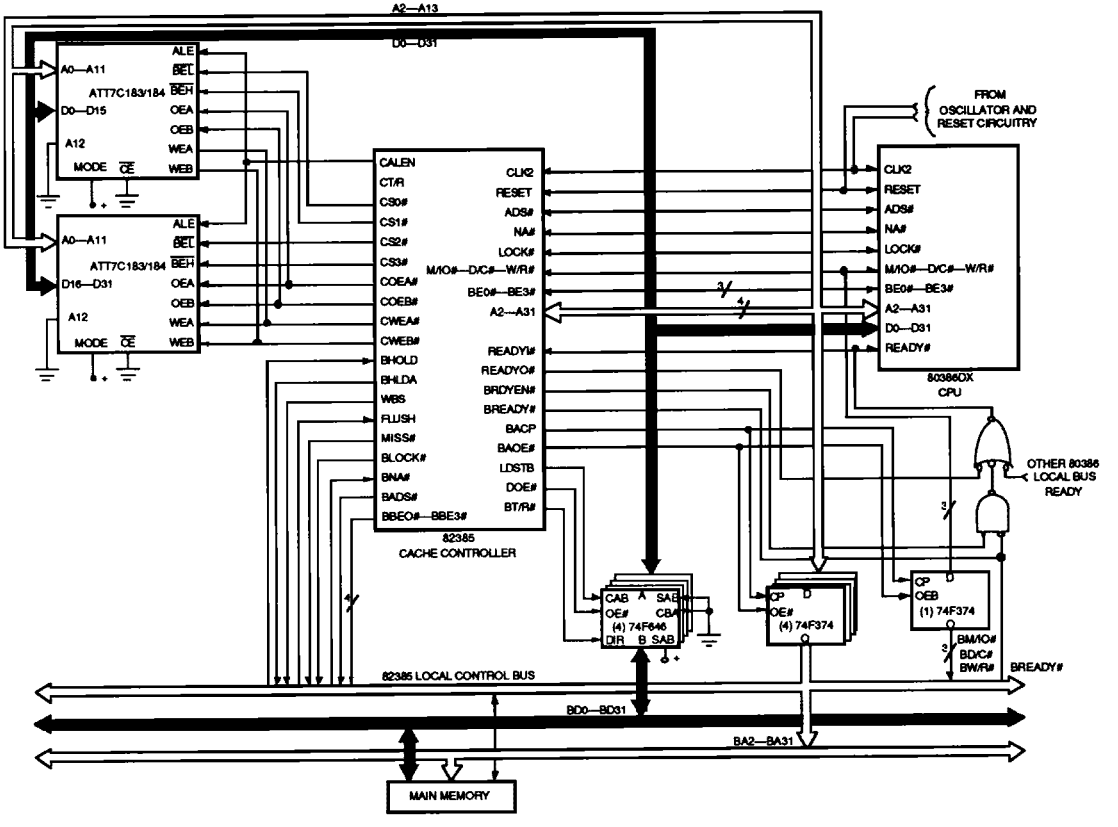


Figure 12. Two-Way Set-Associative Mode 32 Kbit Cache Using the 80386DX CPU and the 82385 Cache Controller

Application Information (continued)

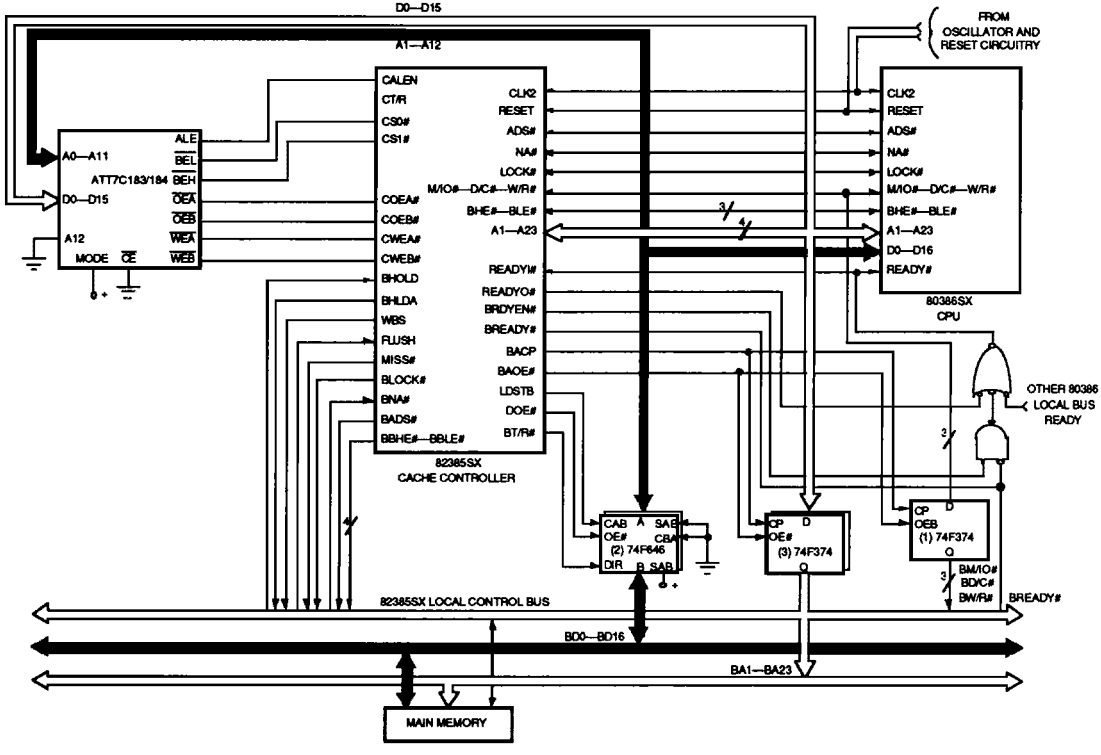
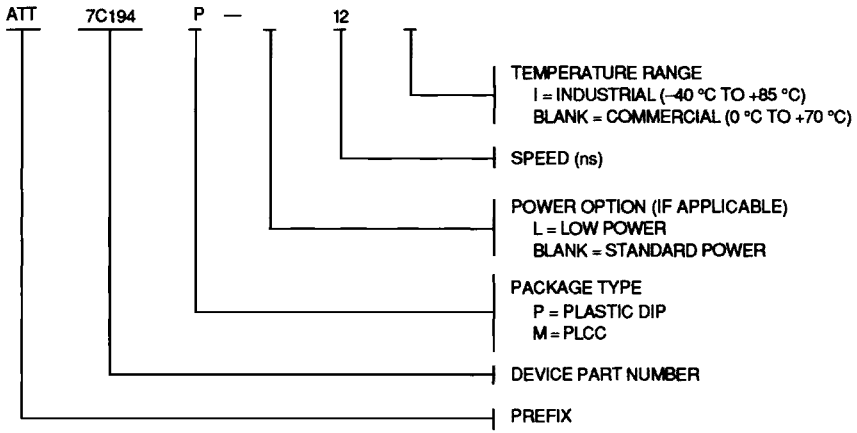


Figure 13. Two-Way Set-Associative 16 Kbit Cache Using the 80386SX CPU and the 82385SX Cache Controller

Ordering Information



ATT7C183

Operating Range 0 °C to 70 °C

Package Style	Performance Speed		
	45 ns	35 ns	25 ns
48-Pin, Plastic DIP	ATT7C183P-45	ATT7C183P-35	ATT7C183P-25
52-Pin, PLCC	ATT7C183M-45	ATT7C183M-35	ATT7C183M-25

ATT7C184

Operating Range 0 °C to 70 °C

Package Style	Performance Speed		
	45 ns	35 ns	25 ns
48-Pin, Plastic DIP	ATT7C184P-45	ATT7C184P-35	ATT7C184P-25
52-Pin, PLCC	ATT7C184M-45	ATT7C184M-35	ATT7C184M-25