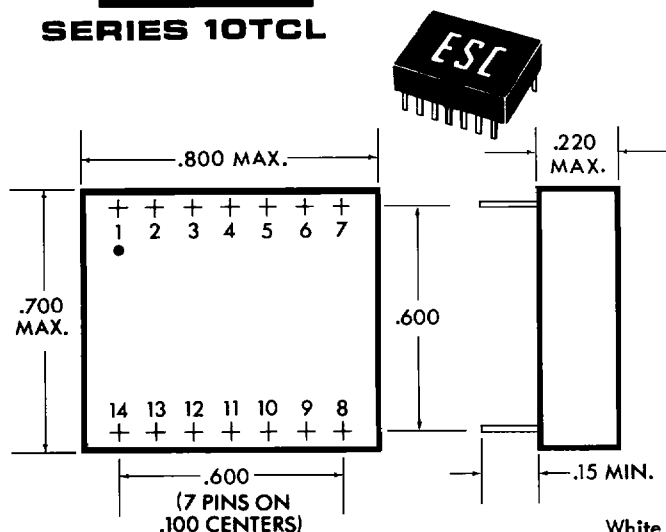


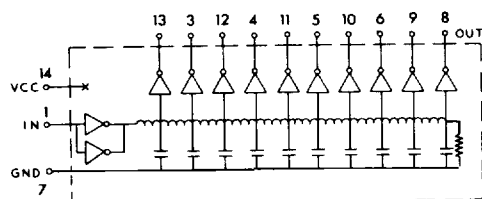


LOW PROFILE MILITARY APPLICATIONS TTL DIGITAL DELAY LINES 10 TAPS • 14 PIN PACKAGE & 5 TAPS • SURFACE MOUNTING

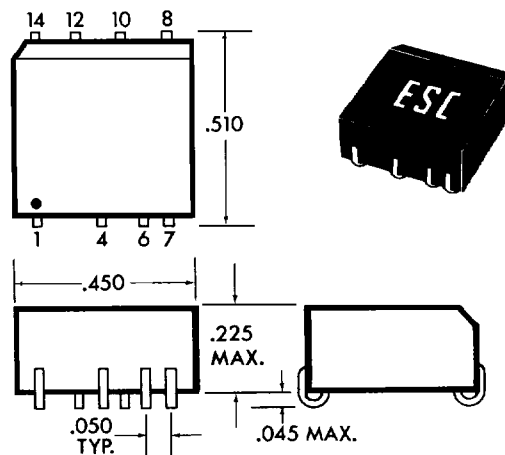
SERIES 10TCL



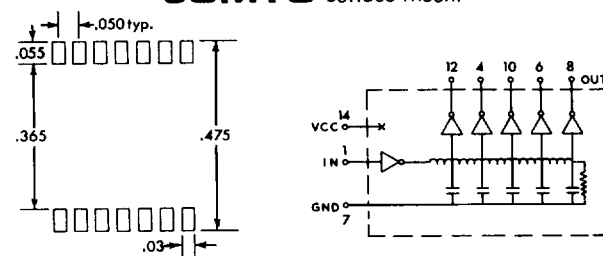
10TCL



SERIES JSMTCL



JSMTCL Surface Mount



Suggested P.C. Board solder pads
for JSMTCL Series

10TCL SERIES		
Model No.	Delay (ns)	Delay/Tap (ns)
10TCL50	50	5
10TCL60	60	6
10TCL70	70	7
10TCL80	80	8
10TCL90	90	9
10TCL100	100	10
10TCL200	200	20
10TCL250	250	25
10TCL300	300	30
10TCL350	350	35
10TCL400	400	40
10TCL450	450	45
10TCL500	500	50

Intermediate delay values available upon request.

JSMTCL SERIES		
Model No.	Delay (ns)	Delay/Tap (ns)
JSMTCL25	25	5
JSMTCL50	50	10
JSMTCL75	75	15
JSMTCL100	100	20
JSMTCL125	125	25
JSMTCL150	150	30
JSMTCL200	200	40
JSMTCL250	250	50

DC PARAMETERS		LIMITS	
		Min.	Max.
V_{oh}	$V_{cc} = \min$ $I_{oh} = 1.0 \text{ mA}$	2.5V	—
V_{ol}	$V_{cc} = \min$ $I_{ol} = 20 \text{ mA}$	—	0.5V
I_{th}	$V_{cc} = \max$ $V_{ih} = 2.7V$	—	50 μA
I_{il}	$V_{cc} = \max$ $V_{il} = 0.5V$	-2.0 mA	—
I_i	$V_{cc} = \max$ $V_i = 5.5V$	—	1.0 mA
V_i	$V_{cc} = \min$ $I_{in} = -18 \text{ mdc}$	-1.2vdc	—
I_{cc}	$V_{cc} = \max$ outputs low	JSMTCL Series 70mA 10TCL Series 140mA	

SPECIFICATIONS:

- Supply voltage (V_{cc}): 5.0VDC $\pm 5\%$
- Delay tolerance: $\pm 2\text{ns}$ or 5% wig
- Rise Time: 4ns max
- Minimum Pulse Width: JSMTCL Series: 40% of T_d
10TCL Series: 20% of T_d
- Maximum Duty Cycle: 50%
- Operating temp. range: -55° to +125°C
- Temp. coeff. of delay: 1.0ns + 500ppm/°C
- Terminals: .018w x .010th

TEST CONDITIONS:

- Temperature: 25° $\pm$ 5°C, $V_{cc}=5.0\text{VDC}$
- Input pulse width: 1.2 times the total delay time
- Pulse spacing: 5 times the total delay time
- Input rise time: 2ns; input pulse amplitude 3.0VDC
- All outputs loaded with 15pf
- Time delays measured at the 1.5 volts level on the leading edges
- Rise time measured from .75 to 2.4V

These devices are supplied with ceramic packaged IC's that have been screened and tested to MIL-STD-883.

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