PCIO

DATA SHEET

PCI I/O Controller

DESCRIPTION

The PCIO chip is a high integration, high performance single chip IO subsystem connected to the PCI local bus. Using a single PCI bus load it integrates high speed Ethernet and EBus2. EBus2 is a generic slave DMA bus (pseudo-ISA bus) to which off-the-shelf peripherals are connected to implement the rest of the Sun core IO system.

PCIO is built around an internal bus (the Channel Engine Interface). This structure is the key to the PCIOs modularity. Above the Channel Engine Interface, the Bus Adapter connects to the PCI bus. The two identical ports on the Channel Engine Interface are used for each of PCIO's functional units: Ethernet and EBus2. Each of these has its own set of control and status registers, data buffers and the core logic function.

Features

- PCI Local Bus master/slave interface, compliant with *PCI Local Bus Specification, Revision 2.1* [1].
- 10baseT (802.3) and 100baseT (802.30) Ethernet, using a derivative of Media Access Control (MAC), with fully buffered transmit and receive channels; media-independent interface (MII).
- Expansion bus interface (EBus2), supporting eight external devices and four buffered slave DMA channels.
- Oscillator for 40 MHz SCSI clock, and free running 10 MHz real-time clock.
- IEEE 1149.1 JTAG compliant test architecture.

The following functions are implemented with off-the-shelf devices, connecting directly to the EBus2:

- PC87303 Super IO, integrating 82077-compatible floppy controller with DMA, parallel port, P1284-compliant, with ECP and EPP with DMA and two 16C550 serial controllers with 16-byte FIFOs for keyboard and mouse.
- Two high performance sync/async serial ports, using Siemens SAB82532, 460.8 KBaud async, 384 KBaud sync.
- Sun compatible NVRAM, MK48T59, with alarm clock interrupt for power management.
- EPROM of flash EPROM, 8-bit wide, up to 16 Mbyte, for OBP and POST code.
- CS4231 Audio CODEC.
- Access to USC and DSC control port.
- Auxiliary IO ports, for power supply control, temperature sensor, frequency calibration and other miscellaneous functions.

Product Summary

The PCIO uses Symbios' VS 500, CMOS 3-layer metal technology. It has 0.75 micron drawn, 0.5 micron effective gate length, and operates at 5 volts. The device is packaged in a 208 Pin PQFP. It has 157 signals and 51 VSS/VDD pads. The PCIO cell has 88k gates and 39k bits of RAM.

The operating frequency for the PCI bus, EBus2 channel engine and the DMA engine of the Ethernet channel is 33.3 MHz. The core, Media Access Control (MAC), operates at 25 MHz.

Maximum power consumption of the PCIO is 2 watts.

1. Although designed to the PCI 2.0 specification, the PCIO controller is compatible with the 2.1 specification as well. However, certain 2.1 recommended features, such as pseudo-split reads and a tighter interpretation of the initial latency rule are not implemented.

BLOCK DIAGRAM

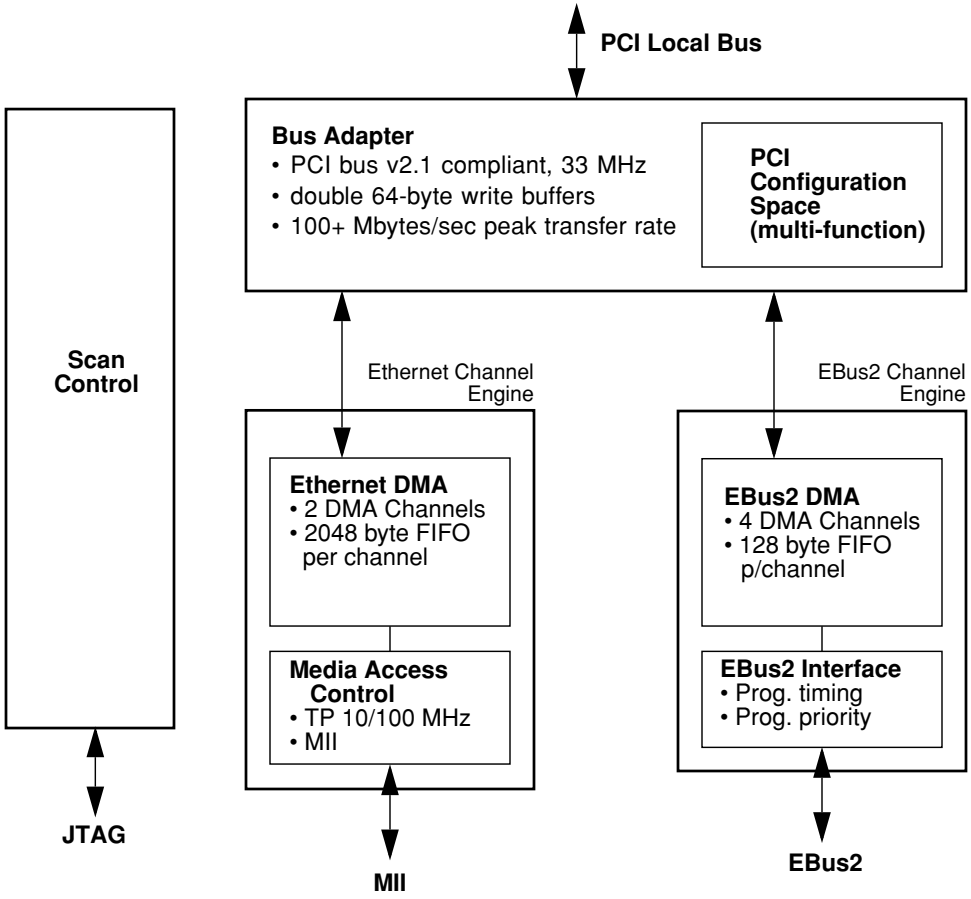


Figure 1. PCIO Block Diagram

Bus Adapter

The Bus Adapter provides a bus-independent layer between the channel engines and the PCI bus. The PCI bus interface is 32-bit and 33 MHz, fully compliant with the *PCI Local Bus Specification, Revision 2.0.* As a master, it is capable of 64-byte (8 word) bursts. DMA writes are buffered in the Bus Adapter to support back to back transactions.

The Bus Adapter also contains the PCI bus Configuration Space. PCIO presents itself to PCI as a multi-function device: EBus2 (a bridge) and Ethernet. Each function has its own area in the configuration space.

Channel Engine Interface

The Bus Adapter contains two identical Channel Engine Interface ports, one for each channel engine. The Channel Engine Interface is a bus independent interface, resulting in a high level of modularity at the design and test level.

EBus2 Channel Engine

The EBus2 Channel Engine interfaces standard off-the-shelf devices to PCIO. Up to eight single or multi-function Intel-style 8-bit devices can be accommodated with a minimum of glue logic. Four internal DMA engines can be attached to any of these devices, buffering data streams in 128-byte FIFOs for each channel.

The standard set of IO devices is: PC87303 or SuperIO (integrates 82077 floppy controller, dual 16C550 serial controllers for keyboard and mouse and ECP / EPP P1284 parallel port), SAB82532 serial communications controller, CS4231 audio CODEC, MK48T59 NVRAM with alarm clock, boot PROM and USC / DSC control port.

The EBus2 Channel Engine provides access to several general purpose IO lines (*a.k.a.* AUXIO), used to control miscellaneous system functions.

Ethernet Channel Engine

The Ethernet Channel Engine provides a buffered full duplex DMA engine and a Media Access Control function based on MAC. The descriptor-based DMA engine contains independent transmit and receive channels, each with 2048 bytes of on-chip buffering. The MAC provides a 10 or 100 Mbps CSMA / CD protocol based network interface conforming to IEEE 802.3, proposed IEEE 802.30 and Ethernet specifications.

Scan Control Block

The Scan Control contains a tap controller.

TYPICAL SYSTEM APPLICATION

The following diagram shows one possible configuration of U2P and PCIO in a PCI based Ultra SPARC system. U2P connects to the System Controller chip and other UPA ports via a UPA address, control and data buses. The system has both PCI and EPCI slots, as well as an on board PCI device (PCIO). Interrupt information is provided by the RIC chip, and a JTAG port is provided for board testing as well as in-circuit testing and debugging of U2P.

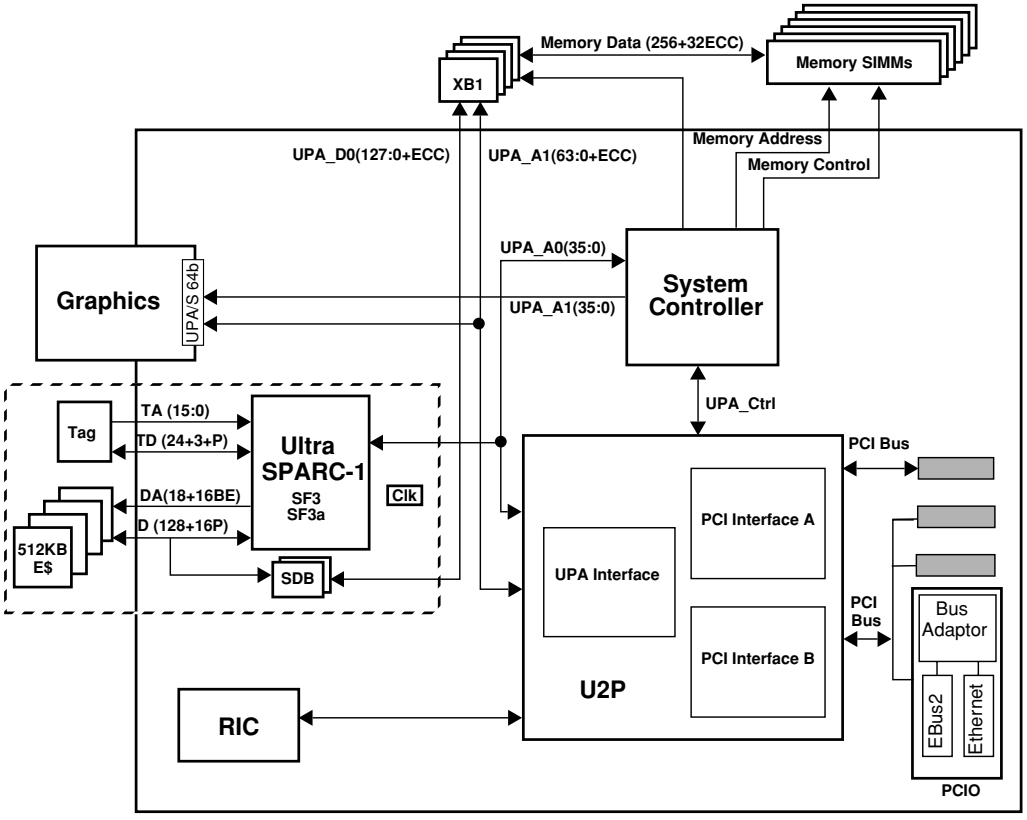


Figure 2. Typical System Application

PINOUT DESCRIPTION

Pin naming conventions

- All pin names are in lower case, except power (VDD) and ground (VSS).
- Active low signals are denoted by an underscore and a letter 'l' —"_l"— following the name.
- Direction is input (I), output (O), tri-state output (T), bidirectional (B), and open drain (D).
- TABLE 1: describes the prefixes used to name signals.

TABLE 1: Signal Name Prefixes

Functional Block	Prefix
PCI Bus	pci_
Ethernet	enet_
EBus2	eb_
JTAG Port	jtag_

Pin Summary

TABLE 2: Pin Count Summary

Section	Pins	What It Includes
PCI Interface	53	Full PCI Bus v2.0; 1BR/BG lines; 4 interrupt lines
Clock Oscillator	7	SCSI clock oscillator
Ethernet Interface	20	MII interface, including transceiver management and serial/nibble selection
EBus2 Interface	41	8 address lines, 8 chip selects
Miscellaneous	25	Mode pin, more interrupts, auxio
Test	11	JTAG port and diagnostics
Signal Total	**157**	
Power/Ground	**51**	**Includes analog power for oscillator**
Total	**208**	

Pinout by Function

TABLE 3: Pinout by Function

Name	Pin	Dir	Type	Description
PCI Interface: 53 pins				
pci_ad[0]	160	BiDir	PCIB	PCI Address/Data Bus (LSB)
pci_ad[1]	158	BiDir	PCIB	PCI Address/Data Bus
pci_ad[2]	157	BiDir	PCIB	PCI Address/Data Bus
pci_ad[3]	156	BiDir	PCIB	PCI Address/Data Bus
pci_ad[4]	155	BiDir	PCIB	PCI Address/Data Bus
pci_ad[5]	154	BiDir	PCIB	PCI Address/Data Bus
pci_ad[6]	153	BiDir	PCIB	PCI Address/Data Bus
pci_ad[7]	152	BiDir	PCIB	PCI Address/Data Bus
pci_ad[8]	149	BiDir	PCIB	PCI Address/Data Bus
pci_ad[9]	148	BiDir	PCIB	PCI Address/Data Bus
pci_ad[10]	147	BiDir	PCIB	PCI Address/Data Bus
pci_ad[11]	146	BiDir	PCIB	PCI Address/Data Bus
pci_ad[12]	144	BiDir	PCIB	PCI Address/Data Bus
pci_ad[13]	142	BiDir	PCIB	PCI Address/Data Bus
pci_ad[14]	140	BiDir	PCIB	PCI Address/Data Bus
pci_ad[15]	139	BiDir	PCIB	PCI Address/Data Bus
pci_ad[16]	125	BiDir	PCIB	PCI Address/Data Bus
pci_ad[17]	123	BiDir	PCIB	PCI Address/Data Bus
pci_ad[18]	122	BiDir	PCIB	PCI Address/Data Bus
pci_ad[19]	121	BiDir	PCIB	PCI Address/Data Bus
pci_ad[20]	120	BiDir	PCIB	PCI Address/Data Bus
pci_ad[21]	118	BiDir	PCIB	PCI Address/Data Bus
pci_ad[22]	115	BiDir	PCIB	PCI Address/Data Bus
pci_ad[23]	114	BiDir	PCIB	PCI Address/Data Bus
pci_ad[24]	111	BiDir	PCIB	PCI Address/Data Bus
pci_ad[25]	110	BiDir	PCIB	PCI Address/Data Bus
pci_ad[26]	108	BiDir	PCIB	PCI Address/Data Bus
pci_ad[27]	107	BiDir	PCIB	PCI Address/Data Bus
pci_ad[28]	106	BiDir	PCIB	PCI Address/Data Bus
pci_ad[29]	105	BiDir	PCIB	PCI Address/Data Bus
pci_ad[30]	104	BiDir	PCIB	PCI Address/Data Bus
pci_ad[31]	103	BiDir	PCIB	PCI Address/Data Bus (MSB)
pci_c_be_l[0]	150	BiDir	PCIB	PCI Command/Byte Enable
pci_c_be_l[1]	138	BiDir	PCIB	PCI Command/Byte Enable

TABLE 3: Pinout by Function (Continued)

Name	Pin	Dir	Type	Description
pci_c_be_l[2]	126	BiDir	PCIB	PCI Command/Byte Enable
pci_c_be_l[3]	112	BiDir	PCIB	PCI Command/Byte Enable
pci_clk	99	In	I	PCI Clock (33.3 MHz)
pci_frame_l	127	BiDir	PCIB	PCI Frame
pci_devsel_l	132	BiDir	PCIB	PCI Device Select
pci_idsel	113	BiDir	PCIB	PCI Device Select - Configuration cycle
pci_irdy_l	130	BiDir	PCIB	PCI Initiator Ready
pci_trdy_l	128	BiDir	PCIB	PCI Target Ready
pci_stop_l	133	BiDir	PCIB	PCI Transaction Terminator
pci_par	136	BiDir	PCIB	PCI Data Parity
pci_perr_l	134	BiDir	PCIB	PCI Parity Error
pci_serr_l	135	BiDir	PCIB	PCI System Error
pci_gnt_l	101	BiDir	PCIB	PCI Bus Grant
pci_req_l	102	BiDir	PCIB	PCI Bus Request
pci_rst_l	97	BiDir	PCIB	PCI Reset
pci_inta_l	95	BiDir	PCIB	PCI Interrupt Request A
pci_intb_l	94	BiDir	PCIB	PCI Interrupt Request B
pci_intc_l	93	BiDir	PCIB	PCI Interrupt Request C
pci_intd_l	92	BiDir	PCIB	PCI Interrupt Request D
EBus2 Interface: 41 pins				
eb_a[0]	203	Out	O4S	EBus2 Address Bus (LSB)
eb_a[1]	202	Out	O4S	EBus2 Address Bus
eb_a[2]	201	Out	O4S	EBus2 Address Bus
eb_a[3]	200	Out	O4S	EBus2 Address Bus
eb_a[4]	198	Out	O4S	EBus2 Address Bus
eb_a[5]	197	Out	O4S	EBus2 Address Bus
eb_a[6]	196	Out	O4S	EBus2 Address Bus
eb_a[7]	194	Out	O4S	EBus2 Address Bus (MSB)
eb_clken	162	Out	O4S	EBus2 Address Latch Enable (bits 23:8)
eb_cs_l[0]	181	Tri	T4S	EPROM Chip Select
eb_cs_l[1]	180	Tri	T4S	TOD Chip Select
eb_cs_l[2]	179	Tri	T4S	General Purpose Chip Select 0
eb_cs_l[3]	177	Tri	T4S	Audio Codec Chip Select
eb_cs_l[4]	176	Tri	T4S	SuperIO Chip Select
eb_cs_l[5]	175	Tri	T4S	85C30 SCC Chip Select
eb_cs_l[6]	174	Tri	T4S	UltraSPARC System Controller Chip Select

TABLE 3: Pinout by Function (Continued)

Name	Pin	Dir	Type	Description
eb_cs_l[7]	172	Tri	T4S	General Purpose Chip Select 1
eb_d[0]	193	BiDir	B8S	EBus2 Data Bus (LSB)
eb_d[1]	192	BiDir	B8S	EBus2 Data Bus
eb_d[2]	190	BiDir	B8S	EBus2 Data Bus
eb_d[3]	188	BiDir	B8S	EBus2 Data Bus
eb_d[4]	187	BiDir	B8S	EBus2 Data Bus
eb_d[5]	186	BiDir	B8S	EBus2 Data Bus
eb_d[6]	185	BiDir	B8S	EBus2 Data Bus
eb_d[7]	184	BiDir	B8S	EBus2 Data Bus (MSB)
eb_dack_l[0]	170	Tri	T4S	EBus2 DMA Acknowledge 0 (Parallel Port)
eb_dack_l[1]	168	Tri	T4S	EBus2 DMA Acknowledge 1 (Floppy)
eb_dack_l[2]	167	Tri	T4S	EBus2 DMA Acknowledge 2 (AudioIn)
eb_dack_l[3]	166	Tri	T4S	EBus2 DMA Acknowledge 3 (AudioOut)
eb_dreq[0]	207	In	I	EBus2 DMA Request 0 (Parallel Port)
eb_dreq[1]	206	In	I	EBus2 DMA Request 1 (Floppy)
eb_dreq[2]	205	In	I	EBus2 DMA Request 2 (Audio In)
eb_dreq[3]	204	In	I	EBus2 DMA Request 3 (Audio Out)
eb_irq1	76	In	I	EBus2 Interrupt 0 (Parallel Port)
eb_irq2	75	In	I	EBus2 Interrupt 1 (Floppy)
eb_irq3	74	In	I	EBus2 Interrupt 2 (Audio Playback)
eb_irq4	73	In	I	EBus2 Interrupt 3 (Audio Capture)
eb_rd_l	163	Tri	T8S	EBus2 Read
eb_wr_l	164	Tri	T8S	EBus2 Write
eb_rdy	77	In	I	EBus2 Ready Input (25 mA pull-up)
eb_tcs	165	Tri	T4S	EBus2 DMA Terminal Count
Ethernet Interface: 20 pins				
enet_exvr_en	31	Tri	T4S	External Transceiver Enable
enet_mgt_clk	32	Tri	T16	Transceiver Management Clock
enet_mgt_d0	34	BiDir	B4S	Transceiver Management Data
enet_mgt_d1	33	BiDir	B4S	Transceiver Management Data
enet_rx_clk	21	In	I	100baseT Receive Clock
enet_rx_dv	22	In	I	100baseT Receive Frame Delimit
enet_rx_er	23	In	I	100baseT Receive Error
enet_rxd[0]	19	In	I	100baseT Receive Data
enet_rxd[1]	18	In	I	100baseT Receive Data
enet_rxd[2]	17	In	I	100baseT Receive Data

TABLE 3: Pinout by Function (Continued)

Name	Pin	Dir	Type	Description
enet_rxd[3]	16	In	I	100baseT Receive Data
enet_tx_clki	10	In	I	10baseT Transmit Clock In
enet_tx_clko	8	Tri	T16	100baseT Transmit Clock Out
enet_tx_col	14	In	I	100baseT Colision Detect
enet_tx_crs	11	In	I	100baseT Carrier Sense
enet_tx_en	9	Tri	T16	100baseT Transmit Enable
enet_txd[0]	30	Tri	T16	100baseT Transmit Data
enet_txd[1]	28	Tri	T16	100baseT Transmit Data
enet_txd[2]	26	Tri	T16	100baseT Transmit Data
enet_txd[3]	24	Tri	T16	100baseT Transmit Data
Miscellaneous & AuxIO: 25 pins				
au_cap_irq_l	72	Out	O4S	Audio Capture Int (Motherboard Mode)
au_pb_irq_l	71	Out	O4S	Audio Playback Int (Motherboard Mode)
aux_ps_off	52	Out	O4S	Power Off Output to Courtesy Outlet
boot[0]	90	In	I	Boot PROM Reset Address
boot[1]	89	In	I	Boot PROM Reset Address
cod_pdwn_l	45	Out	O4S	Audio CODEC Powerdown Output
fpy_dsel	53	Out	O4S	Floppy Density Select Output
fpy_dsens	54	In	I	Floppy Density Sense Input
freq0	70	In	I	Frequency Margining 0
freq1	69	In	I	Frequency Margining 1
freq2	67	In	I	Frequency Margining 2
mode	35	In	I	PCIO Mode = 1 for Add-in PCIO Mode = 0 for Motherboard
pci_s0_prsnt1	65	In	I	PCI Slot 0 Preset - bit 1
pci_s0_prsnt2	63	In	I	PCI Slot 0 Preset - bit 2
pci_s1_prsnt1	62	In	I	PCI Slot 1 Preset - bit 1
pci_s1_prsnt2	61	In	I	PCI Slot 1 Preset - bit 2
pci_s2_prsnt1	60	In	I	PCI Slot 2 Preset - bit 1
pci_s2_prsnt2	59	In	I	PCI Slot 2 Preset - bit 2
pci_s3_prsnt1	58	In	I	PCI Slot 3 Preset - bit 1
pci_s3_prsnt2	57	In	I	PCI Slot 3 Preset - bit 2
sys_ps_off	51	Out	O4S	Power Off Output to Power Supply
system_led	55	Out	O4S	System LED Output
tsens_clk	49	Out	O4S	Temp Sensor Clock
tsens_cs_l	47	Out	O4S	Temp Sensor Chip Select
tsens_d	48	BiDir	B4S	Temp Sensor Data

TABLE 3: Pinout by Function (Continued)

Name	Pin	Dir	Type	Description
SCSI Clock Oscillator: 7 pins				
osc_rst_l	1	In	I	Oscillator Reset
scsi_clk	83	Out	O4S	40/80 MHz SCSI Clock Output
scsi_oscen	82	In	I	SCSI Oscillator Enable
scsi_x1	85	In	C	40/80 MHz SCSI Crystal - X1
scsi_x2	86	Out	N	40/80 MHz SCSI Crystal - X2
clk_10m	81	Out	O4S	Real Time Clock Time Base - 10 MHz
clk_5m	79	Out	O4S	Real Time Clock Time Base - 5 MHz
JTAG Port & Diagnostics: 11 pins				
clock_stop	44	In	I	Stop Clock Input
diag[0]	7	Out	O4S	No Function
diag[1]	5	Out	O4S	No Function
diag[2]	4	Out	O4S	No Function
diag[3]	3	Out	O4S	No Function
diag[4]	2	Out	O4S	No Function
jtag_clk	40	In	I	JTAG Clock
jtag_tdi	38	In	I	JTAG Test Data Input(100mA pull-up)
jtag_tdo	36	Out	O4S	JTAG Test Data Output
jtag_tms	42	In	I	JTAG Test Mode Select (100 mA pull-up)
jtag_trst_l	43	In	I	JTAG Reset (100 mA pull-up)
Power and Ground: 51 pins				
BSINVSSIO BSVSSIO	37 96 131 183			VSS - Pad Ring
BSVSSIO_1	6 12 20 27 46 50 56 66 78 84 98 100 109			VSS - Pad Ring

TABLE 3: Pinout by Function (Continued)

Name	Pin	Dir	Type	Description
BSVSSIO_1	116 124 137 145 151 161 171 178 189 199 208			VSS - Pad Ring
PCIVDDIO	91 119 143 159			VDD - PCI Pad Ring - Socket Compliant
VDDIO	15 29 41 68 87 173 191			VDD - Pad Ring
VSSCORE	13 39 80 117 141 182			Vss - Logic Core
VDDCORE	25 64 88 129 169 195			VDD - Logic Core

Pinout by Pin Number

TABLE 4: Pinout by Pin Number

Name	Pin	Dir	Type	Description
osc_rst_l	1	In	I	Oscillator Reset
diag[4]	2	Out	O4S	No Function
diag[3]	3	Out	O4S	No Function
diag[2]	4	Out	O4S	No Function
diag[1]	5	Out	O4S	No Function
BSVSSIO_1	6			
diag[0]	7	Out	O4S	No Function
enet_tx_clko	8	Tri	T16	100baseT Transmit Clock Out
enet_tx_en	9	Tri	T16	100baseT Transmit Enable
enet_tx_clki	10	In	I	10baseT Transmit Clock In
enet_tx_crs	11	In	I	100baseT Carrier Sense
BSVSSIO_1	12			
VSSCORE	13			
enet_tx_col	14	In	I	100baseT Colision Detect
VDDIO	15			
enet_rxd[3]	16	In	I	100baseT Receive Data
enet_rxd[2]	17	In	I	100baseT Receive Data
enet_rxd[1]	18	In	I	100baseT Receive Data
enet_rxd[0]	19	In	I	100baseT Receive Data
BSVSSIO_1	20			
enet_rx_clk	21	In	I	100baseT Receive Clock
enet_rx_dv	22	In	I	100baseT Receive Frame Delimit
enet_rx_er	23	In	I	100baseT Receive Error
enet_txd[3]	24	Tri	T16	100baseT Transmit Data
VDDCORE	25			
enet_txd[2]	26	Tri	T16	100baseT Transmit Data
BSVSSIO_1	27			
enet_txd[1]	28	Tri	T16	100baseT Transmit Data
VDDIO	29			
enet_txd[0]	30	Tri	T16	100baseT Transmit Data
enet_exvr_en	31	Tri	T4S	External Transceiver Enable
enet_mgt_clk	32	Tri	T16	Transceiver Management Clock
enet_mgt_d1	33	BiDir	B4S	Transceiver Management Data
enet_mgt_d0	34	BiDir	B4S	Transceiver Management Data
mode	35	In	I	PCIO Mode: Add-in/Motherboard

TABLE 4: Pinout by Pin Number (Continued)

Name	Pin	Dir	Type	Description
jtag_tdo	36	Out	O4S	JTAG Test Data Output
BSINVSSIO	37			
jtag_tdi	38	In	I	JTAG Test Data Input(100mA pull-up)
VSSCORE	39			
jtag_clk	40	In	I	JTAG Clock
VDDIO	41			
jtag_tms	42	In	I	JTAG Test Mode Select (100 mA pull-up)
jtag_trst_l	43	In	I	JTAG Reset (100 mA pull-up)
clock_stop	44	In	I	Stop Clock Input
cod_pdwn_l	45	Out	O4S	Audio CODEC Powerdown Output
BSVSSIO_1	46			
tsens_cs_l	47	Out	O4S	Temp Sensor Chip Select
tsens_d	48	BiDir	B4S	Temp Sensor Data
tsens_clk	49	Out	O4S	Temp Sensor Clock
BSVSSIO_1	50			
sys_ps_off	51	Out	O4S	Power Off Output to Power Supply
aux_ps_off	52	Out	O4S	Power Off Output to Courtesy Outlet
fpy_dsel	53	Out	O4S	Floppy Density Select Output
fpy_dsens	54	In	I	Floppy Density Sense Input
system_led	55	Out	O4S	System LED Output
BSVSSIO_1	56			
pci_s3_prsnt2	57	In	I	PCI Slot 3 Preset - bit 2
pci_s3_prsnt1	58	In	I	PCI Slot 3 Preset - bit 1
pci_s2_prsnt2	59	In	I	PCI Slot 2 Preset - bit 2
pci_s2_prsnt1	60	In	I	PCI Slot 2 Preset - bit 1
pci_s1_prsnt2	61	In	I	PCI Slot 1 Preset - bit 2
pci_s1_prsnt1	62	In	I	PCI Slot 1 Preset - bit 1
pci_s0_prsnt2	63	In	I	PCI Slot 0 Preset - bit 2
VDDCORE	64			
pci_s0_prsnt1	65	In	I	PCI Slot 0 Preset - bit 1
BSVSSIO_1	66			
freq2	67	In	I	Frequency Margining 2
VDDIO	68			
freq1	69	In	I	Frequency Margining 1
freq0	70	In	I	Frequency Margining 0
au_pb_irq_l	71	Out	O4S	Audio Playback Int (Motherboard Mode)

TABLE 4: Pinout by Pin Number (Continued)

Name	Pin	Dir	Type	Description
au_cap_irq_l	72	Out	O4S	Audio Capture Int (Motherboard Mode)
eb_irq4	73	In	I	EBus2 Interrupt 3 (Audio Capture)
eb_irq3	74	In	I	EBus2 Interrupt 2 (Audio Playback)
eb_irq2	75	In	I	EBus2 Interrupt 1 (Floppy)
eb_irq1	76	In	I	EBus2 Interrupt 0 (Parallel Port)
eb_rdy	77	In	I	EBus2 Ready Input (25 mA pull-up)
BSVSSIO	78			
clk_5m	79	Out	O4S	Real Time Clock Time Base - 5 MHz
VSSCORE	80			
clk_10m	81	Out	O4S	Real Time Clock Time Base - 10 MHz
scsi_oscen	82	In	I	SCSI Oscillator Enable
scsi_clk	83	Out	O4S	40/80 MHz SCSI Clock Output
BSVSSIO_1	84			
scsi_x1	85	In		40/80 MHz SCSI Crystal - X1
scsi_x2	86	Out		40/80 MHz SCSI Crystal - X2
VDDIO	87			
VDDCORE	88			
boot[1]	89	In	I	Boot PROM Reset Address
boot[0]	90	In	I	Boot PROM Reset Address
PCIVDDIO	91			
pci_intd_l	92	BiDir	PCIB	PCI Interrupt Request D
pci_intc_l	93	BiDir	PCIB	PCI Interrupt Request C
pci_intb_l	94	BiDir	PCIB	PCI Interrupt Request B
pci_inta_l	95	BiDir	PCIB	PCI Interrupt Request A
BSVSSIO	96			
pci_rst_l	97	BiDir	PCIB	PCI Reset
BSVSSIO_1	98			
pci_clk	99	In	I	PCI Clock (33 MHz)
BSVSSIO_1	100			
pci_gnt_l	101	BiDir	PCIB	PCI Bus Grant
pci_req_l	102	BiDir	PCIB	PCI Bus Request
pci_ad[31]	103	BiDir	PCIB	PCI Address/Data Bus (MSB)
pci_ad[30]	104	BiDir	PCIB	PCI Address/Data Bus
pci_ad[29]	105	BiDir	PCIB	PCI Address/Data Bus
pci_ad[28]	106	BiDir	PCIB	PCI Address/Data Bus
pci_ad[27]	107	BiDir	PCIB	PCI Address/Data Bus

TABLE 4: Pinout by Pin Number (Continued)

Name	Pin	Dir	Type	Description
pci_ad[26]	108	BiDir	PCIB	PCI Address/Data Bus
BSVSSIO_1	109			
pci_ad[25]	110	BiDir	PCIB	PCI Address/Data Bus
pci_ad[24]	111	BiDir	PCIB	PCI Address/Data Bus
pci_c_be_l[3]	112	BiDir	PCIB	PCI Command/Byte Enable
pci_idsel	113	BiDir	PCIB	PCI Device Select - Configuration cycle
pci_ad[23]	114	BiDir	PCIB	PCI Address/Data Bus
pci_ad[22]	115	BiDir	PCIB	PCI Address/Data Bus
BSVSSIO_1	116			
VSSCORE	117			
pci_ad[21]	118	BiDir	PCIB	PCI Address/Data Bus
PCIVDDIO	119			
pci_ad[20]	120	BiDir	PCIB	PCI Address/Data Bus
pci_ad[19]	121	BiDir	PCIB	PCI Address/Data Bus
pci_ad[18]	122	BiDir	PCIB	PCI Address/Data Bus
pci_ad[17]	123	BiDir	PCIB	PCI Address/Data Bus
BSVSSIO_1	124			
pci_ad[16]	125	BiDir	PCIB	PCI Address/Data Bus
pci_c_be_l[2]	126	BiDir	PCIB	PCI Command/Byte Enable
pci_frame_l	127	BiDir	PCIB	PCI Frame
pci_trdy_l	128	BiDir	PCIB	PCI Target Ready
VDDCORE	129			
pci_irdy_l	130	BiDir	PCIB	PCI Initiator Ready
BSVSSIO	131			
pci_devsel_l	132	BiDir	PCIB	PCI Device Select
pci_stop_l	133	BiDir	PCIB	PCI Transaction Terminator
pci_perr_l	134	BiDir	PCIB	PCI Parity Error
pci_serr_l	135	BiDir	PCIB	PCI System Error
pci_par	136	BiDir	PCIB	PCI Data Parity
BSVSSIO_1	137			
pci_c_be_l[1]	138	BiDir	PCIB	PCI Command/Byte Enable
pci_ad[15]	139	BiDir	PCIB	PCI Address/Data Bus
pci_ad[14]	140	BiDir	PCIB	PCI Address/Data Bus
VSSCORE	141			
pci_ad[13]	142	BiDir	PCIB	PCI Address/Data Bus
PCIVDDIO	143			

TABLE 4: Pinout by Pin Number (Continued)

Name	Pin	Dir	Type	Description
pci_ad[12]	144	BiDir	PCIB	PCI Address/Data Bus
BSVSSIO_1	145			
pci_ad[11]	146	BiDir	PCIB	PCI Address/Data Bus
pci_ad[10]	147	BiDir	PCIB	PCI Address/Data Bus
pci_ad[9]	148	BiDir	PCIB	PCI Address/Data Bus
pci_ad[8]	149	BiDir	PCIB	PCI Address/Data Bus
pci_c_be_l[0]	150	BiDir	PCIB	PCI Command/Byte Enable
BSVSSIO_1	151			
pci_ad[7]	152	BiDir	PCIB	PCI Address/Data Bus
pci_ad[6]	153	BiDir	PCIB	PCI Address/Data Bus
pci_ad[5]	154	BiDir	PCIB	PCI Address/Data Bus
pci_ad[4]	155	BiDir	PCIB	PCI Address/Data Bus
pci_ad[3]	156	BiDir	PCIB	PCI Address/Data Bus
pci_ad[2]	157	BiDir	PCIB	PCI Address/Data Bus
pci_ad[1]	158	BiDir	PCIB	PCI Address/Data Bus
PCIVDDIO	159			
pci_ad[0]	160	BiDir	PCIB	PCI Address/Data Bus (LSB)
BSVSSIO_1	161			
eb_clken	162	Out	O4S	EBus2 Address Latch Enable (bits 23:12)
eb_rd_l	163	Tri	T8S	EBus2 Read
eb_wr_l	164	Tri	T8S	EBus2 Write
eb_tcs	165	Tri	T4S	EBus2 DMA Terminal Count
eb_dack_l[3]	166	Tri	T4S	EBus2 DMA Acknowledge 3 (AudioOut)
eb_dack_l[2]	167	Tri	T4S	EBus2 DMA Acknowledge 2 (Audio In)
eb_dack_l[1]	168	Tri	T4S	EBus2 DMA Acknowledge 1 (Floppy)
VDDCORE	169			
eb_dack_l[0]	170	Tri	T4S	EBus2 DMA Acknowledge 0 (Parallel Port)
BSVSSIO_1	171			
eb_cs_l[7]	172	Tri	T4S	General Purpose Chip Select 1
VDDIO	173			
eb_cs_l[6]	174	Tri	T4S	UltraSPARC System Controller Chip Select
eb_cs_l[5]	175	Tri	T4S	85C30 SCC Chip Select
eb_cs_l[4]	176	Tri	T4S	SuperIO Chip Select
eb_cs_l[3]	177	Tri	T4S	Audio Codec Chip Select
BSVSSIO_1	178			
eb_cs_l[2]	179	Tri	T4S	General Purpose Chip Select 0

TABLE 4: Pinout by Pin Number (Continued)

Name	Pin	Dir	Type	Description
eb_cs_l[1]	180	Tri	T4S	TOD Chip Select
eb_cs_l[0]	181	Tri	T4S	EPROM Chip Select
VSSCORE	182			
BSVSSIO	183			
eb_d[7]	184	BiDir	B8S	EBus2 Data Bus (MSB)
eb_d[6]	185	BiDir	B8S	EBus2 Data Bus
eb_d[5]	186	BiDir	B8S	EBus2 Data Bus
eb_d[4]	187	BiDir	B8S	EBus2 Data Bus
eb_d[3]	188	BiDir	B8S	EBus2 Data Bus
BSVSSIO_1	189			
eb_d[2]	190	BiDir	B8S	EBus2 Data Bus
VDDIO	191			
eb_d[1]	192	BiDir	B8S	EBus2 Data Bus
eb_d[0]	193	BiDir	B8S	EBus2 Data Bus (LSB)
eb_a[7]	194	Out	O4S	EBus2 Address Bus (MSB)
VDDCORE	195			
eb_a[6]	196	Out	O4S	EBus2 Address Bus
eb_a[5]	197	Out	O4S	EBus2 Address Bus
eb_a[4]	198	Out	O4S	EBus2 Address Bus
BSVSSIO_1	199			
eb_a[3]	200	Out	O4S	EBus2 Address Bus
eb_a[2]	201	Out	O4S	EBus2 Address Bus
eb_a[1]	202	Out	O4S	EBus2 Address Bus
eb_a[0]	203	Out	O4S	EBus2 Address Bus (LSB)
eb_dreq[3]	204	In	I	EBus2 DMA Request 3 (Audio Out)
eb_dreq[2]	205	In	I	EBus2 DMA Request 2 (Audio In)
eb_dreq[1]	206	In	I	EBus2 DMA Request 1 (Floppy)
eb_dreq[0]	207	In	I	EBus2 DMA Request 0 (Parallel Port)
BSVSSIO_1	208			

Pinout by Pin Name

TABLE 5: Pinout by Pin Name

Name	Pin	Dir	Type	Description
BSINVSSIO	37			VSS - Pad Ring
BSVSSIO	131 183 78 96			VSS - Pad Ring
BSVSSIO_1	100 109 116 12 124 137 145 151 161 171 178 189 199 20 208 27 46 50 56 6 66 84 98			VSS - Pad Ring
PCIVDDIO	119 143 159 91			VDD - PCI Pad Ring
VDDCORE	129 169 195 25 64 88			VDD - Logic Core

TABLE 5: Pinout by Pin Name (Continued)

Name	Pin	Dir	Type	Description
VDDIO	15 173 191 29 41 68 87			VDD - Pad Ring
VSSCORE	117 13 141 182 39 80			VSS - Logic Core
au_cap_irq_l	72	Out	O4S	Audio Capture Int (Motherboard Mode)
au_pb_irq_l	71	Out	O4S	Audio Playback Int (Motherboard Mode)
aux_ps_off	52	Out	O4S	Power Off Output to Courtesy Outlet
boot[0]	90	In	I	Boot PROM Reset Address
boot[1]	89	In	I	Boot PROM Reset Address
clk_10m	81	Out	O4S	Real Time Clock Time Base - 10 MHz
clk_5m	79	Out	O4S	Real Time Clock Time Base - 5 MHz
clock_stop	44	In	I	Stop Clock Input
cod_pdwn_l	45	Out	O4S	Audio CODEC Powerdown Output
diag[0]	7	Out	O4S	No Function
diag[1]	5	Out	O4S	No Function
diag[2]	4	Out	O4S	No Function
diag[3]	3	Out	O4S	No Function
diag[4]	2	Out	O4S	No Function
eb_a[0]	203	Out	O4S	EBus2 Address Bus (LSB)
eb_a[1]	202	Out	O4S	EBus2 Address Bus
eb_a[2]	201	Out	O4S	EBus2 Address Bus
eb_a[3]	200	Out	O4S	EBus2 Address Bus
eb_a[4]	198	Out	O4S	EBus2 Address Bus
eb_a[5]	197	Out	O4S	EBus2 Address Bus
eb_a[6]	196	Out	O4S	EBus2 Address Bus
eb_a[7]	194	Out	O4S	EBus2 Address Bus (MSB)
eb_clken	162	Out	O4S	EBus2 Address Latch Enable (bits 23:12)
eb_cs_l[0]	181	Tri	T4S	EPROM Chip Select
eb_cs_l[1]	180	Tri	T4S	TOD Chip Select

TABLE 5: Pinout by Pin Name (Continued)

Name	Pin	Dir	Type	Description
eb_cs_l[2]	179	Tri	T4S	General Purpose Chip Select 0
eb_cs_l[3]	177	Tri	T4S	Audio Codec Chip Select
eb_cs_l[4]	176	Tri	T4S	SuperIO Chip Select
eb_cs_l[5]	175	Tri	T4S	85C30 SCC Chip Select
eb_cs_l[6]	174	Tri	T4S	UltraSPARC System Controller Chip Select
eb_cs_l[7]	172	Tri	T4S	General Purpose Chip Select 1
eb_d[0]	193	BiDir	B8S	EBus2 Data Bus (LSB)
eb_d[1]	192	BiDir	B8S	EBus2 Data Bus
eb_d[2]	190	BiDir	B8S	EBus2 Data Bus
eb_d[3]	188	BiDir	B8S	EBus2 Data Bus
eb_d[4]	187	BiDir	B8S	EBus2 Data Bus
eb_d[5]	186	BiDir	B8S	EBus2 Data Bus
eb_d[6]	185	BiDir	B8S	EBus2 Data Bus
eb_d[7]	184	BiDir	B8S	EBus2 Data Bus (MSB)
eb_dack_l[0]	170	Tri	T4S	EBus2 DMA Acknowledge 0 (Parallel Port)
eb_dack_l[1]	168	Tri	T4S	EBus2 DMA Acknowledge 1 (Floppy)
eb_dack_l[2]	167	Tri	T4S	EBus2 DMA Acknowledge 2 (Audio In)
eb_dack_l[3]	166	Tri	T4S	EBus2 DMA Acknowledge 3 (AudioOut)
eb_dreq[0]	207	In	I	EBus2 DMA Request 0 (Parallel Port)
eb_dreq[1]	206	In	I	EBus2 DMA Request 1 (Floppy)
eb_dreq[2]	205	In	I	EBus2 DMA Request 2 (Audio In)
eb_dreq[3]	204	In	I	EBus2 DMA Request 3 (Audio Out)
eb_irq1	76	In	I	EBus2 Interrupt 0 (Parallel Port)
eb_irq2	75	In	I	EBus2 Interrupt 1 (Floppy)
eb_irq3	74	In	I	EBus2 Interrupt 2 (Audio Playback)
eb_irq4	73	In	I	EBus2 Interrupt 3 (Audio Capture)
eb_rd_l	163	Tri	T8S	EBus2 Read
eb_rdy	77	In	I	EBus2 Ready Input (25 mA pull-up)
eb_tcs	165	Tri	T4S	EBus2 DMA Terminal Count
eb_wr_l	164	Tri	T8S	EBus2 Write
enet_exvr_en	31	Tri	T4S	External Transceiver Enable
enet_mgt_clk	32	Tri	T16	Transceiver Management Clock
enet_mgt_d0	34	BiDir	B4S	Transceiver Management Data
enet_mgt_d1	33	BiDir	B4S	Transceiver Management Data
enet_rx_clk	21	In	I	100baseT Receive Clock
enet_rx_dv	22	In	I	100baseT Receive Frame Delimit

TABLE 5: Pinout by Pin Name (Continued)

Name	Pin	Dir	Type	Description
enet_rx_er	23	In	I	100baseT Receive Error
enet_rxd[0]	19	In	I	100baseT Receive Data
enet_rxd[1]	18	In	I	100baseT Receive Data
enet_rxd[2]	17	In	I	100baseT Receive Data
enet_rxd[3]	16	In	I	100baseT Receive Data
enet_tx_clki	10	In	I	10baseT Transmit Clock In
enet_tx_clko	8	Tri	T16	100baseT Transmit Clock Out
enet_tx_col	14	In	I	100baseT Colision Detect
enet_tx_crs	11	In	I	100baseT Carrier Sense
enet_tx_en	9	Tri	T16	100baseT Transmit Enable
enet_txd[0]	30	Tri	T16	100baseT Transmit Data
enet_txd[1]	28	Tri	T16	100baseT Transmit Data
enet_txd[2]	26	Tri	T16	100baseT Transmit Data
enet_txd[3]	24	Tri	T16	100baseT Transmit Data
fpy_dsel	53	Out	O4S	Floppy Density Select Output
fpy_dsens	54	In	I	Floppy Density Sense Input
freq0	70	In	I	Frequency Margining 0
freq1	69	In	I	Frequency Margining 1
freq2	67	In	I	Frequency Margining 2
jtag_clk	40	In	I	JTAG Clock
jtag_tdi	38	In	I	JTAG Test Data Input(100mA pull-up)
jtag_tdo	36	Out	O4S	JTAG Test Data Output
jtag_tms	42	In	I	JTAG Test Mode Select (100 mA pull-up)
jtag_trst_l	43	In	I	JTAG Reset (100 mA pull-up)
mode	35	In	I	PCIO Mode: Add-in/Motherboard
osc_rst_l	1	In	I	Oscillator Reset
pci_ad[0]	160	BiDir	PCIB	PCI Address/Data Bus (LSB)
pci_ad[1]	158	BiDir	PCIB	PCI Address/Data Bus
pci_ad[2]	157	BiDir	PCIB	PCI Address/Data Bus
pci_ad[3]	156	BiDir	PCIB	PCI Address/Data Bus
pci_ad[4]	155	BiDir	PCIB	PCI Address/Data Bus
pci_ad[5]	154	BiDir	PCIB	PCI Address/Data Bus
pci_ad[6]	153	BiDir	PCIB	PCI Address/Data Bus
pci_ad[7]	152	BiDir	PCIB	PCI Address/Data Bus
pci_ad[8]	149	BiDir	PCIB	PCI Address/Data Bus
pci_ad[9]	148	BiDir	PCIB	PCI Address/Data Bus

TABLE 5: Pinout by Pin Name (Continued)

Name	Pin	Dir	Type	Description
pci_ad[10]	147	BiDir	PCIB	PCI Address/Data Bus
pci_ad[11]	146	BiDir	PCIB	PCI Address/Data Bus
pci_ad[12]	144	BiDir	PCIB	PCI Address/Data Bus
pci_ad[13]	142	BiDir	PCIB	PCI Address/Data Bus
pci_ad[14]	140	BiDir	PCIB	PCI Address/Data Bus
pci_ad[15]	139	BiDir	PCIB	PCI Address/Data Bus
pci_ad[16]	125	BiDir	PCIB	PCI Address/Data Bus
pci_ad[17]	123	BiDir	PCIB	PCI Address/Data Bus
pci_ad[18]	122	BiDir	PCIB	PCI Address/Data Bus
pci_ad[19]	121	BiDir	PCIB	PCI Address/Data Bus
pci_ad[20]	120	BiDir	PCIB	PCI Address/Data Bus
pci_ad[21]	118	BiDir	PCIB	PCI Address/Data Bus
pci_ad[22]	115	BiDir	PCIB	PCI Address/Data Bus
pci_ad[23]	114	BiDir	PCIB	PCI Address/Data Bus
pci_ad[24]	111	BiDir	PCIB	PCI Address/Data Bus
pci_ad[25]	110	BiDir	PCIB	PCI Address/Data Bus
pci_ad[26]	108	BiDir	PCIB	PCI Address/Data Bus
pci_ad[27]	107	BiDir	PCIB	PCI Address/Data Bus
pci_ad[28]	106	BiDir	PCIB	PCI Address/Data Bus
pci_ad[29]	105	BiDir	PCIB	PCI Address/Data Bus
pci_ad[30]	104	BiDir	PCIB	PCI Address/Data Bus
pci_ad[31]	103	BiDir	PCIB	PCI Address/Data Bus (MSB)
pci_c_be_l[0]	150	BiDir	PCIB	PCI Command/Byte Enable
pci_c_be_l[1]	138	BiDir	PCIB	PCI Command/Byte Enable
pci_c_be_l[2]	126	BiDir	PCIB	PCI Command/Byte Enable
pci_c_be_l[3]	112	BiDir	PCIB	PCI Command/Byte Enable
pci_clk	99	In	I	PCI Clock (33 MHz)
pci_devsel_l	132	BiDir	PCIB	PCI Device Select
pci_frame_l	127	BiDir	PCIB	PCI Frame
pci_gnt_l	101	BiDir	PCIB	PCI Bus Grant
pci_idsel	113	BiDir	PCIB	PCI Device Select - Configuration cycle
pci_inta_l	95	BiDir	PCIB	PCI Interrupt Request A
pci_intb_l	94	BiDir	PCIB	PCI Interrupt Request B
pci_intc_l	93	BiDir	PCIB	PCI Interrupt Request C
pci_intd_l	92	BiDir	PCIB	PCI Interrupt Request D
pci_irdy_l	130	BiDir	PCIB	PCI Initiator Ready

TABLE 5: Pinout by Pin Name (Continued)

Name	Pin	Dir	Type	Description
pci_par	136	BiDir	PCIB	PCI Data Parity
pci_perr_l	134	BiDir	PCIB	PCI Parity Error
pci_req_l	102	BiDir	PCIB	PCI Bus Request
pci_rst_l	97	BiDir	PCIB	PCI Reset
pci_s0_prsnt1	65	In	I	PCI Slot 0 Preset - bit 1
pci_s0_prsnt2	63	In	I	PCI Slot 0 Preset - bit 2
pci_s1_prsnt1	62	In	I	PCI Slot 1 Preset - bit 1
pci_s1_prsnt2	61	In	I	PCI Slot 1 Preset - bit 2
pci_s2_prsnt1	60	In	I	PCI Slot 2 Preset - bit 1
pci_s2_prsnt2	59	In	I	PCI Slot 2 Preset - bit 2
pci_s3_prsnt1	58	In	I	PCI Slot 3 Preset - bit 1
pci_s3_prsnt2	57	In	I	PCI Slot 3 Preset - bit 2
pci_serr_l	135	BiDir	PCIB	PCI System Error
pci_stop_l	133	BiDir	PCIB	PCI Transaction Terminator
pci_trdy_l	128	BiDir	PCIB	PCI Target Ready
scsi_clk	83	Out	O4S	40/80 MHz SCSI Clock Output
scsi_oscen	82	In	I	SCSI Oscillator Enable
scsi_x1	85	In	C	40/80 MHz SCSI Crystal - X1
scsi_x2	86	Out	N	40/80 MHz SCSI Crystal - X2
sys_ps_off	51	Out	O4S	Power Off Output to Power Supply
system_led	55	Out	O4S	System LED Output
tsens_clk	49	Out	O4S	Temp Sensor Clock
tsens_cs_l	47	Out	O4S	Temp Sensor Chip Select
tsens_d	48	BiDir	B4S	Temp Sensor Data

ELECTRICAL SPECIFICATIONS

TABLE 6: Absolute Maximum Ratings

Symbol	Parameter	Limit	Unit
VDD	DC Power Supply Voltage	-0.5 to 7.0	V
Vin, Vout	DC Input, Output Voltage	-0.5 to VDD + 0.5	V
I	DC Current Drain per VDD and VSS pair	100	mA
Tstg	Storage Temperature	-55 to 150	°C
Tcm	Maximum Case Temperature	85	°C
Pd	Power dissipation	2.0	Watts

Note: Stresses beyond those listed in the above table may cause physical damage to the device and should be avoided.

TABLE 7: Recommended Operating Conditions

Symbol	Parameter	Limit	Unit
VDD	DC Power Supply Voltage	4.75 to 5.25	V
Vin, Vout	DC Input, Output Voltage	0 to VDD	V
Tco	Operating Case Temperature	0 to 70	°C

TABLE 8: DC Characteristics [1]

Symbol	Parameter	Conditions	Min	Max	Unit
Vil	Input Low Voltage				
	TTL			0.8	V
	CMOS			VDD*0.3	V
Vih	Input High Voltage				
	TTL		2.0		V
	CMOS		VDD*0.7		V
Voh	Output High Voltage				
	TTL	Ioh = -4,-8,-16 mA	2.4		V
	CMOS	Ioh = -4,-8,-16 mA	VDD -0.8		V
	PCI (DC)	Ioh = -2 mA	2.4		V
Vol	Output Low Voltage				
	TTL	Iol = -4, -8, -16 mA		0.4	V
	CMOS	Iol = -4, -8, -16 mA		0.5	V
	PCI (DC)	Iol = -3, -6 mA [2]		0.5	V
Ii	Input Leakage (non PCI pins)	Vin=VDD or GND		+/- 10	µA
Iih	Input High Leakage (PCI pins)	Vin=2.7V		70	µA
Iil	InputLow Leakage (PCI pins)	Vin=0.5V		- 70	µA
Cin	Input Pin Capacitance (PCI)			10	pF
Cclk	CLK Pin Capacitance (PCI)			12	pF
Cidsel	IDSEL Pin Capacitance (PCI)			8	pF

1. JTAG are TTL input levels
2. Signals without pullup must have 3 mA Iol. Signals requiring pullup must have 6 mA Iol.

TABLE 9: Environmental Electrical Protection

ESD	Latch UP
Minimum	Minimum
2KV	150 mA

AC CHARACTERISTICS

AC Timing Characteristics have been obtained with operating conditions exceeding the recommended limits. A 10% voltage variation, 4.5V to 5.5V, is factored into the vendors BCCOM and WCCOM timing libraries and is specified in Table 10 through Table 13.

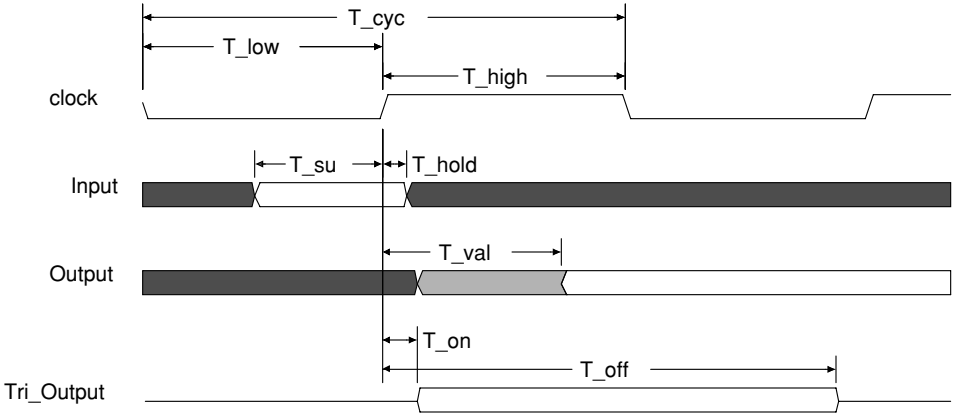


Figure 3. General Timing Waveforms

TABLE 10: PCI AC Timing Characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
T_cyc	pci_clk Cycle Time		30	DC	ns
T_high	pci_clk High Time		11		ns
T_low	pci_clk Low Time		11		ns
PCI Inputs					
T_su	Input Setup Time to pci_clk - bused	See Note 1	7.5		ns
T_su(ptp)	Input Setup Time to pci_clk - pci_gnt_l		10		ns
T_hold	Input Hold Time from pci_clk	See Note 2	0.5		ns
PCI Outputs					
T_val	pci_clk to Signal Valid Delay - bused	50pF Load	2	11	ns
T_val(ptp)	pci_clk to Signal Valid Delay - pci_req_l	50pF Load	2	12	ns
T_on	Float to Active Delay		2		ns
T_off	Active to Float Delay			28	ns

1. Static Timing analysis indicates 350ps T_su requirement. Test vector extraction software required 1ns granularity. PCI T_su specification currently being tested to 7.5 ns value.
2. Static Timing analysis shows 250ps T_hold requirement. Test vector extraction software required 1ns granularity. PCI T_hold specification currently being tested to 0.5 ns value

TABLE 11: Ethernet Timing Characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
RX and TX Clocks					
T_cyc	rx/tx clk Cycle Time		40		ns
	Duty Cycle		35	65	%
MII Interface					
T_su(rx)	MII RX Inputs Setup Time to rx_clk		8.0		ns
T_hld(rx)	MII RX Inputs Hold Time to rx_clk		8.0		ns
T_su(tx)	MII TX Inputs Setup Time to tx_clk		8.0		ns
T_hld(tx)	MII TX Inputs Hold Time to tx_clk		8.0		
T_val	MII TX Output Valid Time from tx_clk	30pF Load		15	ns

TABLE 12: JTAG Timing Characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
JTAG clock					
T_cyc	JTAG clk Cycle Time		100		ns
JTAG Inputs					
T_su(rx)	JTAG Inputs Setup Time to jtag_clk		0		ns
T_hld(rx)	JTAG Inputs Hold Time to jtag_clk		44		ns
T_val	JTAG Output Valid Time from jtag_clk negative edge	30pF Load		20	ns

EBus2 Timing

The EBus2 is an asynchronous bus. Its timing is self regulated handshaking, having no fixed relationship to the PCIO clock.

The EBus2 timing is programmable via three timing control registers in the Ebus2 channel engine. The timing control registers programming is detailed in the PCIO User's Manual: see Chapter 7 "EBus2 Channel Engine," section 7.5.2, section 7.6 and section 7.7.

The three timing control registers enable the following functions:

- SETUP TIME (Tsu) and HOLD TIME (Thld) of EB_CSx_ or DACKx_ with respect to the EB_RD_ or EB_WR_ strobes.
- Minimum deassertion time or RECOVERY TIME (Thld) between consecutive EB_RD_ or EB_WR_ strobes.
- WIDTH (Tstrb) of EB_RD_ or EB_WR_ strobes.
- Selection of DMA priority algorithm

Figure 4 illustrates the timing parameters which can be controlled through timing control registers.

Timing control registers are programmable at boot time. *DO NOT* alter them after boot time. The timing given in the timing control register tables is in terms of the number of EBus2 clocks. Note that the EBus2 clock is the same as the PCI clock which has a duration of 30ns.

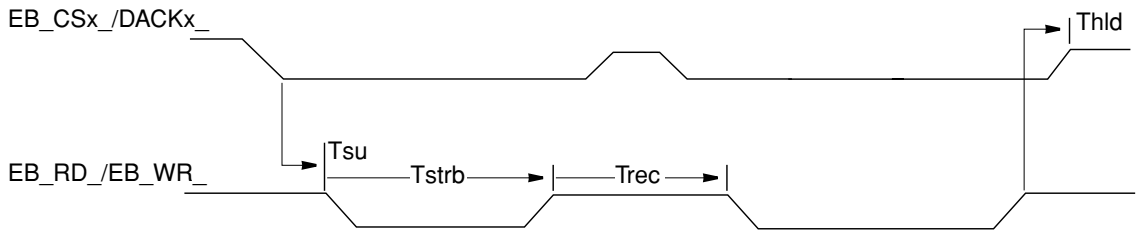


Figure 4. Programmable Timing Paramaters

EBus2 Output and Input Signals: AC Timing Characteristics

Table 13 specifies the AC tming characteristics required on the EBus2 input and output signals.

TABLE 13: EBus2 Timing Characteristics

Symbol	Parameter	Condition	Minimum	Maximum	Units
Tcyc	EBus2 Clock Cycle Time	[1]	30		ns
T_high	EBus2 Clock High Time	[1]	11		ns
T_low	EBus2 Clock Low Time	[1]	11		ns
EBus2 Inputs					
Tsu	Input setup time to the EB_CLK		8		ns
Th	Input hold time from the EB_CLK		8		ns
EBus2 Outputs					
Tdo	EB_CLK to output valid delay	50 pf load		13	ns

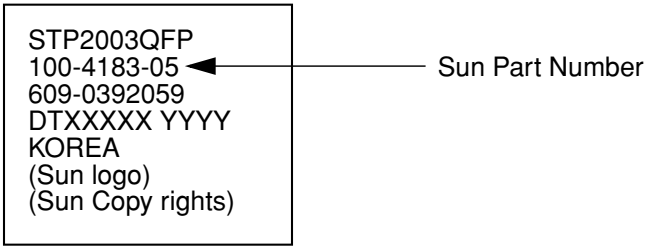
1. The EBus2 clock is an EBus2 channel engine internal clock used in PCIO chips. EBus 2 is the same as the PCI clock which has a duration of 30ns.

MECHANICAL INFORMATION

Package Information and Drawings

PCIO is packaged in a 208-pin, molded PQFP with copper fused lead frame and heat spreader for enhanced thermal dissipation. The die attach pad is 512 x 512 Mil. Package drawings and mechanical data are shown below.

Package Marking (Production Version)



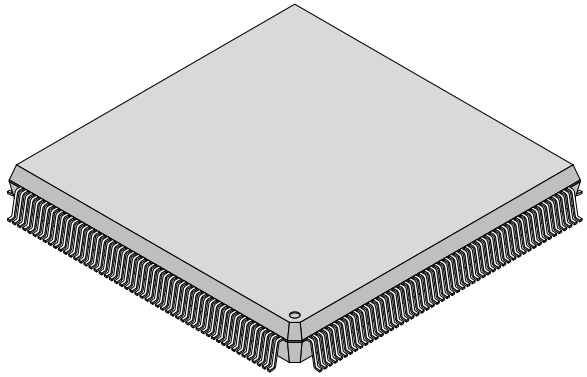
DTXXXXX: Lot trace number (e.g. DT06551)

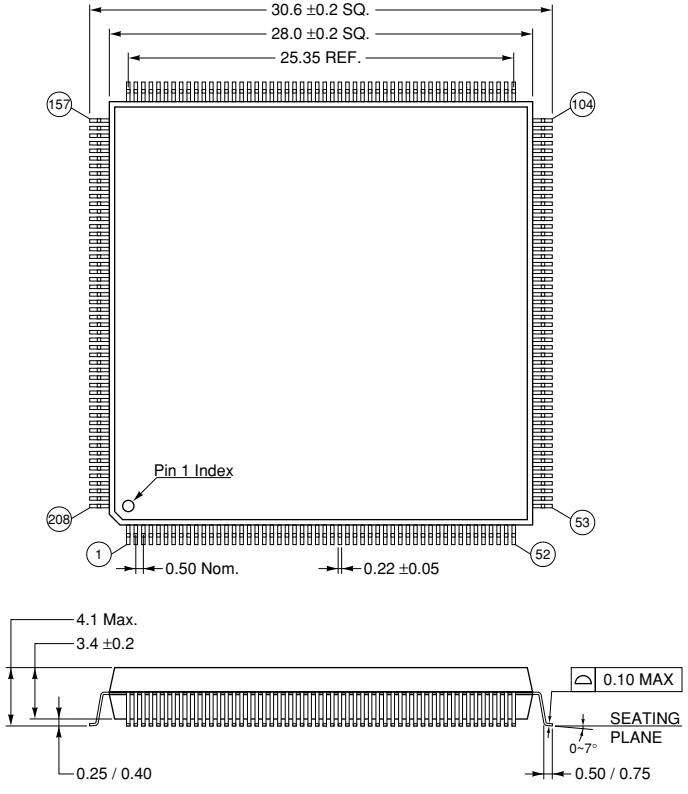
YYYY: Assembly date code (for example: 9542; and only for dates 96XX and later)

TABLE 14: Thermal Characteristics (extrapolated - no air flow)

Package type	Theta_JA	Theta_JC	Unit
fused lead frame + heat spreader	20.0	5.0	°C/W

208-Pin PQFP Package Dimensions





Dimensions in millimeters.

ORDERING INFORMATION

Part Number	Description
STP2003PQFP	PCIO Controller, 208-Pin Plastic Quad Flat Pack (PQFP)

Document Part Number: 802-7836-02