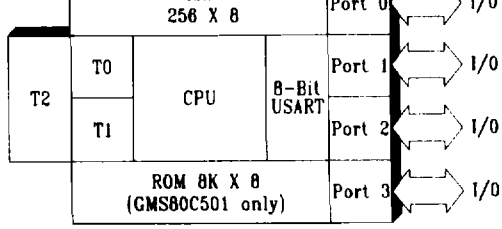
1. General Description

The GMS80C501 contains a non-volatile 8K x 8 read-only program memory, a volatile 256 x 8 read/write data memory, four ports, three 16-bit timers/counters a six-source two-priority-level interrupt structure, and a serial port.
The GMS80C301 is identical, except that it lacks the program memory on chip (ROM). Therefore the term GMS80C501 refers to both versions within this specification unless otherwise noted.

2. Feature

- Fully compatible to standard 8051 microcontroller
- Versions for 12/24/40 MHz operating frequency
- 8K x 8 ROM (GMS80C501 only)
- 256 x 8 RAM
- Four 8-bit ports
- Three 16-bit Timers/Counters (Timer 2 with Up/Down Counter feature)
- USART
- Six interrupt sources, two priority levels
- Power Saving Modes
- P-DIP-40, P-LCC-44, and P-MQFP-44 package
- Temperature ranges: T_A = 0°C~70°C

GMS80501/301



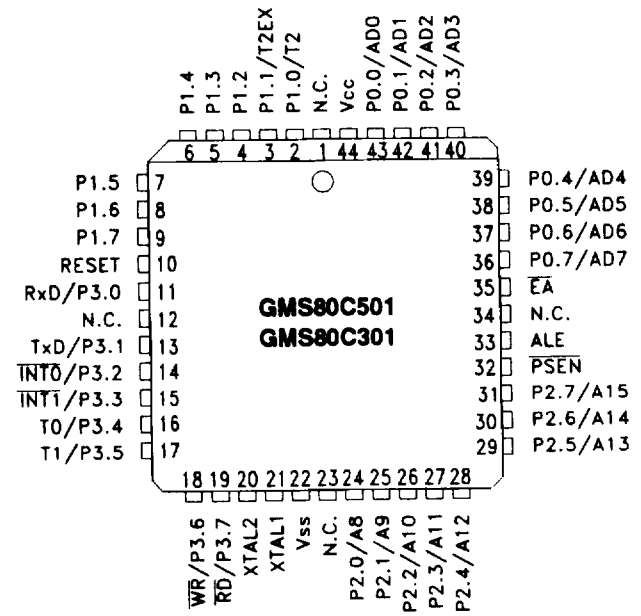
The GMS80C501/301 described in this document is compatible with the standard 80C52/32 and can be used for all present standard 80C52/32 applications.

Ordering Information

Type	Package	Description (8-Bit CMOS microcontroller)
GMS80C501 GMS80C501-PL GMS80C501-Q	P-DIP-40 P-LCC-44 P-MQFP-44	with mask-programmable ROM 12 MHz
GMS80C301 GMS80C301-PL GMS80C301-Q	P-DIP-40 P-LCC-44 P-MQFP-44	for external memory 12MHz
GMS80C501-24 GMS80C501-24-PL GMS80C501-24-Q	P-DIP-40 P-LCC-44 P-MQFP-44	with mask-programmable ROM 24 MHz
GMS80C301-24 GMS80C301-24-PL GMS80C301-24-Q	P-DIP-40 P-LCC-44 P-MQFP-44	for external memory 24MHz
GMS80C501-40 GMS80C501-40-PL GMS80C501-40-Q	P-DIP-40 P-LCC-44 P-MQFP-44	with mask-programmable ROM 40MHz
GMS80C301-40 GMS80C301-40-PL GMS80C301-40-Q	P-DIP-40 P-LCC-44 P-MQFP-44	for external memory 40MHz

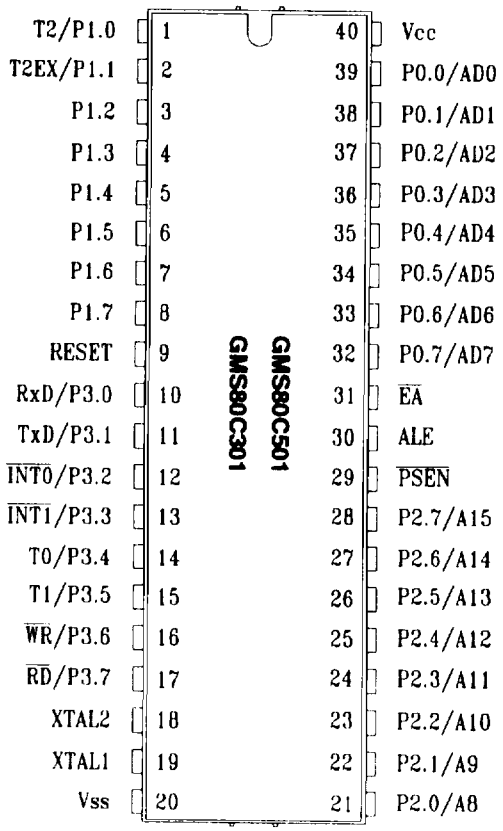
Pin Configuration
(top view)

(P-LCC-44)

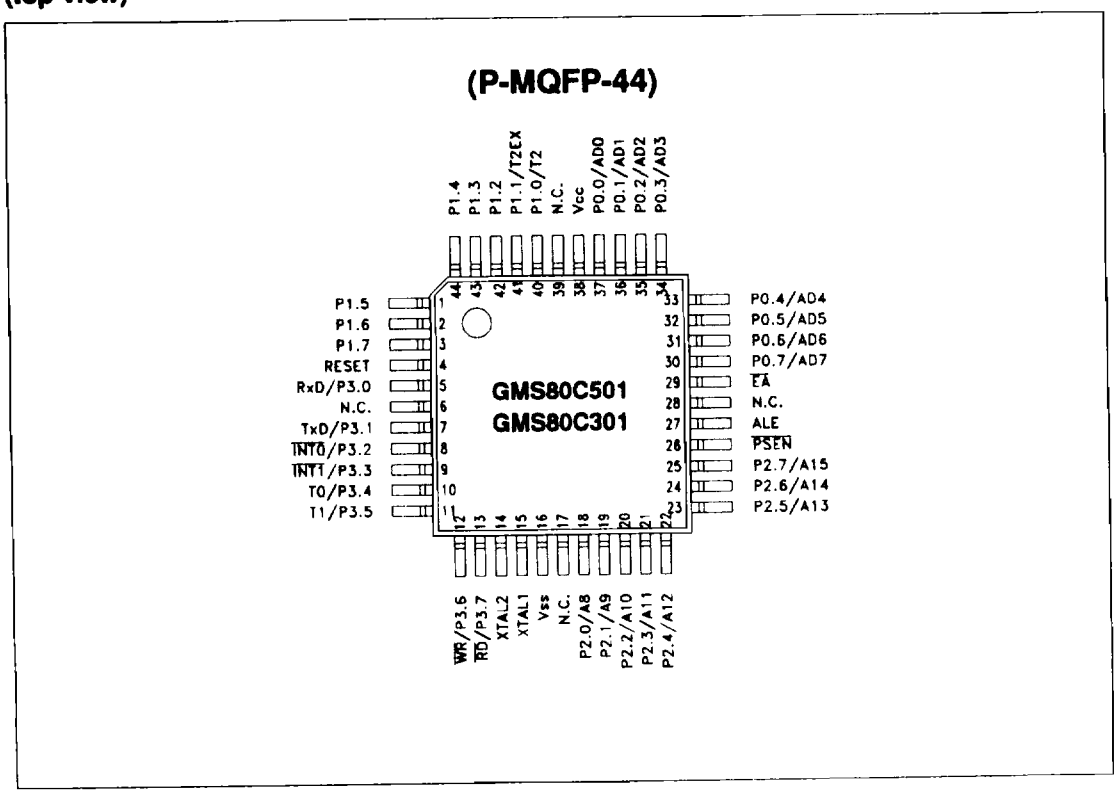


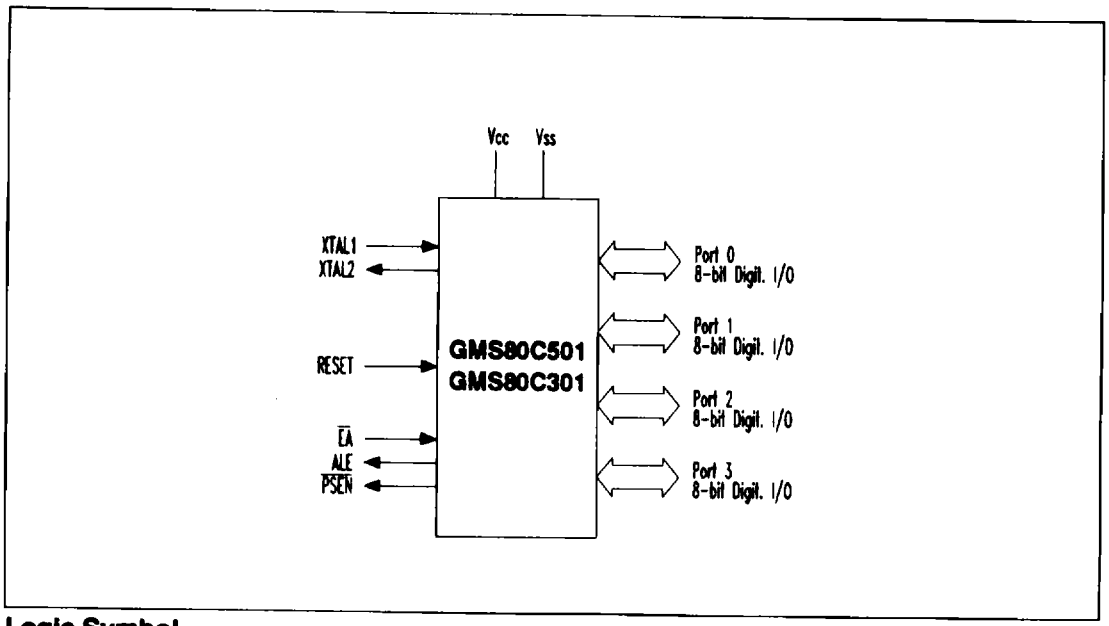
Pin Configuration
(top view)

(P-DIP-40)



Pin Configuration
(top view)





Logic Symbol

Pin Definitions and Functions

Symbol	Pin Number			I/O*)	Function
	P-LCC-44	P-DIP-40	P-MQFP-44		
P1.0 - P1.7	2-9	1-8	40-44, 1-3,	I/O	**Port1** is a bidirectional I/O port with internal pull-up resistors. Port 1 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, port 1 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pull-up resistors. Port 1 also contains the timer 2 pins as secondary function. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. The secondary functions are assigned to the pins of port 1, as follows: P1.0 T2 Input to counter 2 P1.1 T2EX Capture - Reload trigger of timer 2 / Up-Down count
	2 3	1 2	40 41		

*) I = Input
O = Output

Pin Definitons and Functions (cont'd)

Symbol	Pin Number			I/O*)	Function
	P-LCC-44	P-DIP-40	P-MQFP-44		
P3.0 - P3.7	11, 13-19	10-17	5, 7-13	I/O	**Port 3** is a bidirectional I/O port with internal pull-up resistors. Port 3 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state they can be used as inputs. As inputs, port 3 pins being externally pulled low will source current. (I_{IL}, in the DC characteristics) because of the internal pull-up resistors. Port 3 also contains the interrupt, timer, serial port 0 and external memory strobe pins which are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. The secondary functions are assigned to the pins of port 3, as follows:
	11	10	5		P3.0 RxD receiver data input (asynchronous) or data input output(synchronous) of serial interface 0
	13	11	7		P3.1 TxD transmitter data output (asynchronous) or clock output (synchronous) of the serial interface 0
	14	12	8		P3.2 $\overline{INT0}$ interrupt 0 input/timer 0 gate control
	15	13	9		P3.3 $\overline{INT1}$ interrupt 1 input/timer 1 gate control
	16	14	10		P3.4 T0 counter 0 input
	17	15	11		P3.5 $\overline{T1}$ counter 1 input
	18	16	12		P3.6 $\overline{WR}$ the write control signal latches the data byte from port 0 into the external data memory
	19	17	13		P3.7 $\overline{RD}$ the read control signal enables the external data memory to port 0
XTAL2	20	18	14	-	**XTAL2** Output of the inverting oscillator amplifier.

*) I = Input
O = Output

Pin Definitions and Functions (cont'd)

Symbol	Pin Number			I/O*)	Function
	P-LCC-44	P-DIP-40	P-MQFP-44		
XTAL1	21	19	15	-	**XTAL1** Input to the inverting oscillator amplifier and input to the internal clock generator circuits. To drive the device from an external clock source, XTAL1 should be driven, while XTAL2 is left unconnected. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is divided down by a divide-by-two flip-flop. Minimum and maximum high and low times as well as rise fall times specified in the AC characteristics must be observed.
P2.0-P2.7	24-31	21-28	18-25	I/O	**Port2** is a bidirectional I/O port with internal pull-up resistors. Port 2 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state they can be used as inputs. As inputs, port 2 pins being externally pulled low will source current(I_{IL}, in the DC characteristics) because of the internal pull-up resistors. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses(MOVX @DPTR). In this application it uses strong internal pull-up resistors when issuing 1s. During accesses to external data memory that use 8-bit addresses (MOVX @RI), port 2 issues the contents of the P2 special function register.
$\overline{PSEN}$	32	29	26	O	**The $\overline{Program\ Store\ Enable}$** output is a control signal that enables the external program memory to the bus during external fetch operations. It is activated every six oscillator periods except during external data memory accesses. Remains high during internal program execution.

*) I = Input
O = Output

Pin Definitons and Functions (cont'd)

Symbol	Pin Number			I/O*)	Function
	P-LCC-44	P-DIP-40	P-MQFP-44		
RESET	10	9	4	I	**RESET** A high level on this pin for two machine cycles while the oscillator is running resets the device. An internal diffused resistor to V_{SS} permits power-on reset using only an external capacitor to V_{CC}.
ALE	33	30	27	O	The **Address Latch Enable** output is used for latching the low-byte of the address into external memory during normal operation. It is activated every six oscillator periods except during an external data memory access
$\overline{EA}$	35	31	29	I	**External Access Enable** When held at high level, instructions are fetched from the internal ROM (GMS80C501only) when the PC is less than 2000_H. When held at low level, the GMS80C501 fetches all instructions from external program memory. For the GMS80C301 this pin must be tied low.
P0.0 - P0.7	43-36	39-32	37-30	I/O	**Port 0** is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float, and in that state can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program or data memory. In this application it uses strong internal pull-up resistors when issuing 1s. Port 0 also outputs the code bytes during program verification in the GMS80C501. External pull-up resistors are required during program verification
V_{SS}	22	20	16	-	**Circuit ground potential**
V_{CC}	44	40	38	-	**Supply terminal** for all operating modes
N.C.	1, 12 23, 34	-	6, 17, 28,39	-	**No connection**

*) I = Input
O = Output

Functional Description

The GMS80C501/301 is fully compatible to the standard 8051 microcontroller family.

It is compatible with the general 80C52/32. While maintaining all architectural and operational characteristics of the general 80C52/32 the GMS80C501/301 incorporates some enhancements in the Timer2 Unit.

Figure 1 shows a block diagram of the GMS80C501/301

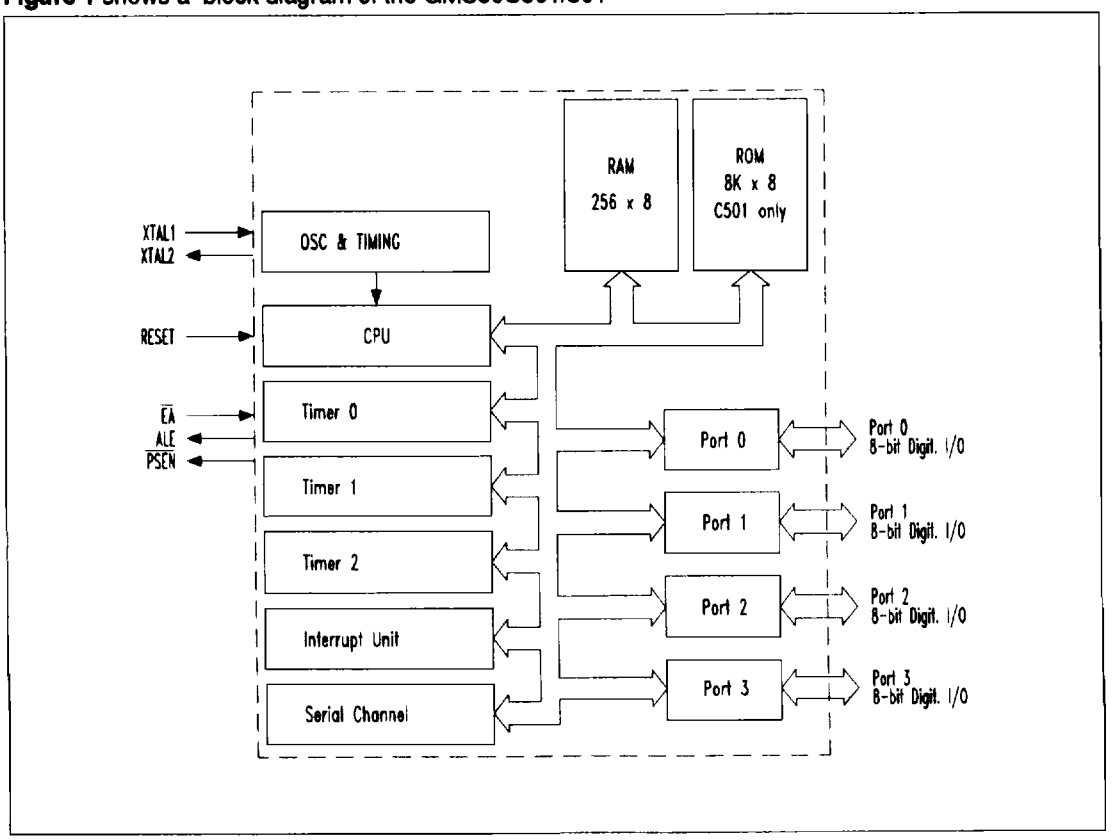


Figure 1
Block Diagram of the GMS80C501/301

CPU

The GMS80C501/301 is efficient both as a controller and as an arithmetic processor. It has extensive facilities for binary and BCD arithmetic and excels in its bit-handling capabilities. Efficient use of program memory results from an instruction set consisting of 44% one-byte, 41% two-byte, and 15% three-byte instructions. with a 12 MHz crystal, 58% of the instructions are executed in 1.0μs 24MHz : 500ns, 40MHz : 300ns).

Special Function Register PSW

	MSB							LSB	
Bit No.	7	6	5	4	3	2	1	0	
Addr. $D0_H$	CY	AC	F0	RS1	RS0	OV	F1	P	PSW

Bit		Function
CY		**Carry Flag**
AC		**Auxiliary Carry Flag** (for BCD operations)
F0		**General Purpose Flag**
RS1	**RS0**	**Register Bank select control bits**
0	0	Bank 0 selected, data address 00_H - 07_H
0	1	Bank 1 selected, data address 08_H - $0F_H$
1	0	Bank 2 selected, data address 10_H - 17_H
1	1	Bank 3 selected, data address 18_H - $1F_H$
OV		**Overflow Flag**
F1		**General Purpose Flag**
P		**Parity Flag** Set/cleared by hardware each instruction cycle to indicate an odd/ even number of "one" bits in the accumulator, i.e. even parity.

Reset value of PSW is 00H.

Special Function Registers

All registers, except the program counter and the four general purpose register banks, reside in the special function register area.

The 27 special function registers (SFR) include pointers and registers that provide an interface between the CPU and the other on-chip peripherals. There are also 128 directly addressable bits within the SFR area.

All SFRs are listed in **table 1**, **table 2**, and **table 3.**

In **table 1** they are organized in numeric order of their addresses. In **table 2** they are orgainzed in groups which refer to the functional blocks of the GMS80C501/301. **Table 3** illustrates the contents of the SFRs.

Table 1

Special Function Registers in Numeric Order of their Addresses

Address	Register	Contents after Reset	Address	Register	Contents after Reset
80H	**P0**[1]	**FFH**	**98H**	**SCON**[1]	**00H**
81H	SP	07H	99H	SBUF	XXH[2]
82H	DPL	00H	9AH	reserved	XXH[2]
83H	DPH	00H	9BH	reserved	XXH[2]
84H	reserved	XXH[2]	9CH	reserved	XXH[2]
85H	reserved	XXH[2]	9DH	reserved	XXH[2]
86H	reserved	XXH[2]	9EH	reserved	XXH[2]
87H	PCON	0XXX000B[2]	9FH	reserved	XXH[2]
88H	**TCON**[1]	**00H**	**A0H**	**P2**[1]	**FFH**
89H	TMOD	00H	A1H	reserved	XXH[2]
8AH	TL0	00H	A2H	reserved	XXH[2]
8BH	TL1	00H	A3H	reserved	XXH[2]
8CH	TH0	00H	A4H	reserved	XXH[2]
8DH	TH1	00H	A5H	reserved	XXH[2]
8EH	reserved	XXH[2]	A6H	reserved	XXH[2]
8FH	reserved	XXH[2]	A7H	reserved	XXH[2]
90H	**P1**[1]	**FFH**	**A8H**	**IE**[1]	**0X000000B**[2]
91H	reserved	00H	A9H	reserved	XXH[2]
92H	reserved	XXH[2]	AAH	reserved	XXH[2]
93H	reserved	XXH[2]	ABH	reserved	XXH[2]
94H	reserved	XXH[2]	ACH	reserved	XXH[2]
95H	reserved	XXH[2]	ADH	reserved	XXH[2]
96H	reserved	XXH[2]	AEH	reserved	XXH[2]
97H	reserved	XXH[2]	AFH	reserved	XXH[2]

[1] : Bit-addressable Special Function Register
[2] : X means that the value is indeterminate and the location is reserved

[1] : Bit-addressable Special Function Register
[2] : X means that the value is indeterminate and the location is reserved

Table 1
Special Function Registers in Numeric Order of their Addresses (cont'd)

Address	Register	Contents after Reset	Address	Register	Contents after Reset
$B0_H$	**P3**[1]	**FF_H**	**$D8_H$**	reserved	XX_H[2]
$B1_H$	reserved	XX_H[2]	$D9_H$	reserved	XX_H[2]
$B2_H$	reserved	XX_H[2]	DA_H	reserved	XX_H[2]
$B3_H$	reserved	XX_H[2]	DB_H	reserved	XX_H[2]
$B4_H$	reserved	XX_H[2]	DC_H	reserved	XX_H[2]
$B5_H$	reserved	XX_H[2]	DD_H	reserved	XX_H[2]
$B6_H$	reserved	XX_H[2]	DE_H	reserved	XX_H[2]
$B7_H$	reserved	XX_H[2]	DF_H	reserved	XX_H[2]
$B8_H$	**IP**[1]	**$XX000000_B$**[2]	**$E0_H$**	**ACC**[1]	**00_H**
$B9_H$	reserved	XX_H[2]	$E1_H$	reserved	XX_H[2]
BA_H	reserved	XX_H[2]	$E2_H$	reserved	XX_H[2]
BB_H	reserved	XX_H[2]	$E3_H$	reserved	XX_H[2]
BC_H	reserved	XX_H[2]	$E4_H$	reserved	XX_H[2]
BD_H	reserved	XX_H[2]	$E5_H$	reserved	XX_H[2]
BE_H	reserved	XX_H[2]	$E6_H$	reserved	XX_H[2]
BF_H	reserved		$E7_H$	reserved	XX_H[2]
$C0_H$	reserved	**XX_H**[2]	**$E8_H$**	reserved	XX_H[2]
$C1_H$	reserved	XX_H[2]	$E9_H$	reserved	XX_H[2]
$C2_H$	reserved	XX_H[2]	EA_H	reserved	XX_H[2]
$C3_H$	reserved	XX_H[2]	EB_H	reserved	XX_H[2]
$C4_H$	reserved	XX_H[2]	EC_H	reserved	XX_H[2]
$C5_H$	reserved	XX_H[2]	ED_H	reserved	XX_H[2]
$C6_H$	reserved	XX_H[2]	EE_H	reserved	XX_H[2]
$C7_H$	reserved	XX_H[2]	EF_H	reserved	XX_H[2]
$C8_H$	**T2CON**	**00_H**	**$F0_H$**	**B**[1]	**00_H**
$C9_H$	T2MOD	$XXXXXXX0_B$[2]	$F1_H$	reserved	XX_H[2]
CA_H	RC2L	00_H	$F2_H$	reserved	XX_H[2]
CB_H	RC2H	00_H	$F3_H$	reserved	XX_H[2]
CC_H	TL2	00_H	$F4_H$	reserved	XX_H[2]
CD_H	TH2	00_H	$F5_H$	reserved	XX_H[2]
CE_H	reserved	XX_H[2]	$F6_H$	reserved	XX_H[2]
CF_H	reserved	XX_H[2]	$F7_H$	reserved	XX_H[2]
$D0_H$	**PSW**[1]	**00_H**	**$F8_H$**	reserved	XX_H[2]
$C1_H$	reserved	XX_H[2]	$F9_H$	reserved	XX_H[2]
$C2_H$	reserved	XX_H[2]	FA_H	reserved	XX_H[2]
$C3_H$	reserved	XX_H[2]	FB_H	reserved	XX_H[2]
$C4_H$	reserved	XX_H[2]	FC_H	reserved	XX_H[2]
$C5_H$	reserved	XX_H[2]	FD_H	reserved	XX_H[2]
$C6_H$	reserved	XX_H[2]	FE_H	reserved	XX_H[2]
$C7_H$	reserved	XX_H[2]	FF_H	reserved	XX_H[2]

Table 2

Special Function Registers - Functional Blocks

Block	Symbol	Name	Address	Contents after Reset
CPU	ACC	Accumulator	**E0H**[1]	00H
	B	B-Register	**F0H**[1]	00H
	DPH	Data Pointer, High Byte	83H	00H
	DPL	Data Pointer, Low Byte	82H	00H
	PSW	Program Status Word Register	**D0H**[1]	00H
	SP	Stack Pointer	81H	07H
Interrupt System	IE	Interrupt Enable Register	**A8H**[1]	0X000000B[2]
	IP	Interrupt Priority Register	**B8H**[1]	XX000000B[2]
Ports	P0	Port 0	**80H**[1]	FFH
	P1	Port 1	**90H**[1]	XXH[3]
	P2	port 2	**A0H**[1]	FFH
	P3	Port 3	**B0H**[1]	FFH
Serial Channels	PCON[2]	Power Control Register	87H	0XXX0000B[2]
	SBUF	Serial Channel Buffer Reg.	99H	XXH[3]
	SCON	Serial Channel 0 Control Reg.	**98H**[1]	00H
Timer 0 / Timer 1	TCON	Timer 0/1 Control Register	**88H**[1]	00H
	TH0	Timer 0, High Byte	8CH	00H
	TH1	Timer 1, High Byte	8DH	00H
	TL0	Timer 0, Low Byte	8AH	00H
	TL1	Timer 1, Low Byte	8BH	00H
	TMOD	Timer Mode Register	89H	00H
Timer 2	T2CON	Timer 2 Control Register	**C8H**[1]	00H
	T2MOD	Timer 2 Mode Register	C9H	00H
	RC2H	Timer 2 Reload Capture Reg., High Byte	CBH	00H
	RC2L	Timer 2 Reload Capture Reg., Low Byte	CAH	00H
	TH2	Timer 2, High Byte	CDH	00H
	TL2	Timer 2, Low Byte	CCH	00H
Pow Sav Modes	PCON	Power Control Register	87H	0XXX0000B[2]

1) Bit-addressable Special Function register
2) Thig special function register is listed repeatedly since some bit of it also belong to other functional blocks
3) X means that the value is indeterminate and the location is reserved

Table 3
Contents of SFRs, SFRs In Numeric Order

Address	Register	Bit7	6	5	4	3	2	1	0
80H	P0								
81H	SP								
82H	DPL								
83H	DPH								
87H	PCON	SMOD	-	-	-	GF1	GF0	PDE	IDLE
88H	TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
89H	TMOD	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0
8AH	TL0								
8BH	TL1								
8CH	TH0								
8DH	TH1								
90H	P1								
98H	SCON	SM0	SM1	SM2	REN	TB8	RB8	TI	RI
99H	SBUF								
A0H	P2								
A8H	IE	EA	-	ET2	ES	ET1	EX1	ET0	EX0
B0H	P3								
B8H	IP	-	-	PT2	PS	PT1	PX1	PT0	PX0
C8H	T2CON	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$
C9H	T2MOD	-	-	-	-	-	-	-	DCEN

SFR bit and byte addressable

SFR not bit addressable

- : = this bit location is reserved

Table 3
Contents of SFRs, SFRs In Numeric Order (cont'd)

Address	Register	Bit7	6	5	4	3	2	1	0
CA_H	RC2L								
CB_H	RC2H								
CC_H	TL2								
CD_H	TH2								
$D0_H$	PSW	CY	AC	F0	RS1	RS0	OV	F1	P
$E0_H$	ACC								
$F0_H$	B								


SFR bit and byte addressable


SFR not bit addressable

- : = this bit location is reserved

Timer / Counter 0 and 1

Timer/Counter 0 and 1 can be used in four operating modes as listed in **table 4:**

Table 4

Timer/Counter 0 and 1 Operating Modes

Mode	Description	TMOD				Input Clock	
		Gate	C/$\overline{T}$	M1	M0	Internal	external (max)
0	8-bit timer/counter with a divide-by-32 prescaler	X	X	0	0	f_{OSC}/ 12×32	f_{OSC}/ 24×32
1	16-bit timer/counter	X	X	0	1	f_{OSC}/ 12	f_{OSC}/ 24
2	8-bit timer/counter with 8-bit autoreload	X	X	1	0	f_{OSC}/ 12	f_{OSC}/ 24
3	Timer/counter 0 used as one 8-bit timer/counter and one 8-bit timer Timer 1 stops	X	X	1	1	f_{OSC}/ 12	f_{OSC}/ 23

In the "timer" function (C/$\overline{T}$ = '0') the register is incremented every machine cycle. therefore the count rate is $f_{OSC}/12$.

In the "counter" function the register is incremented in response to a 1-to-0 transition at its corresponding external input pin (P3.4/T0, P3.5/T1). Since it takes two machine cycles to detect a falling edge the max. count rate is $f_{OSC}/24$. External inputs $\overline{INT0}$ and $\overline{INT1}$ (P3.2, P3.3) can be programmed to function as a gate to facilitate pulse width measurements. **Figure 2** illustrates the input clock logic.

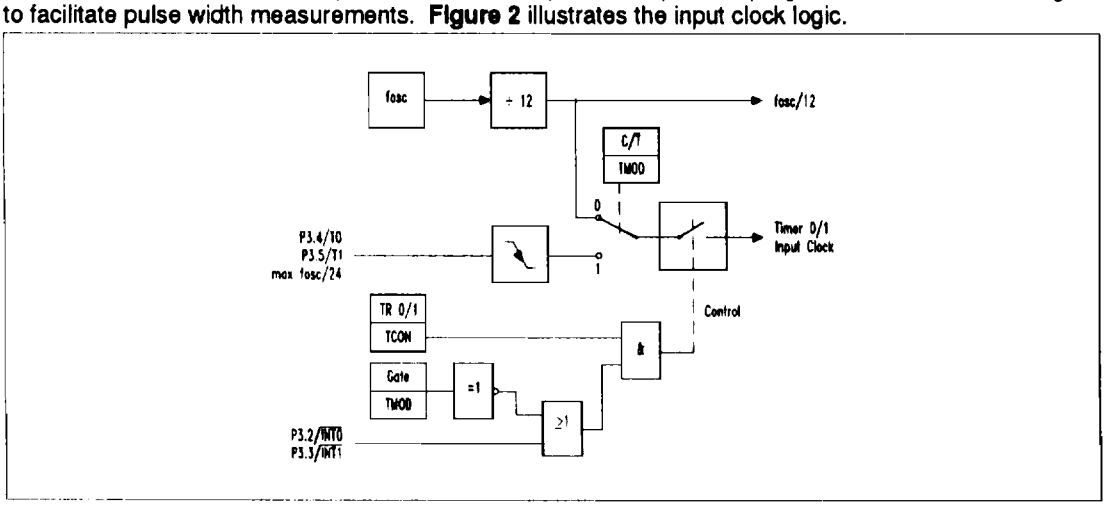


Figure 2

Timer/Counter 0 and 1 Input Clock Logic

Timer 2

Timer 2 is a 16-bit timer/Counter with an up/down count feature. It can operate either as timer or as an event counter which is selected by bit C/$\overline{T2}$ (T2CON.1). It has three operating modes as shown in **table 5.**

Table 5.

Timer/Counter 2 Operating Modes

Mode	T2CON			T2MOD	T2CON	P1.1/ T2EX	Remarks	Input Clock	
	RxCLK or TxCLK	CP/ $\overline{RL2}$	TR2	DCEN	EXEN			Internal	external (P1.0/T2)
16-bit Auto-reload	0	0	1	0	0	X	Reload upon overflow	fosc/ 12	max fosc/ 24
	0	0	1	0	1	↓	Reload trigger (falling edge)		
	0	0	1	1	X	0	Down counting		
	0	0	1	1	X	1	Up counting		
16-bit Capture	0	1	1	X	0	X	16 bit Timer/ Counter (only up-counting) Capture TH2, TL2 → RC2H, RC2L	fosc/ 12	max fosc/ 24
	0	1	1	X	1	↓			
Baud Rate Generator	1	X	1	X	0	X	No overflow interrupt request (TF2) Extra external interrupt ("Timer 2")	fosc/ 2	max fosc/ 24
	1	X	1	X	1	↓			
off	X	X	0	X	X	X	Timer 2 stops	-	-

Note : ↓ = falling edge

Serial Interface (USART)

The serial port is full duplex and can operate in four modes (one synchronous mode, three asynchronous modes) as illustrated in **table 6.** The possible baud rates can be calculated using the formulas given in **table 7.**

Table 6
USART Operating Modes

Mode	SCON		Baud rate	Description
	SM0	SM1		
0	0	0	fosc/ 12	Serial data enters and exits through RxD. TxD outputs the shift clock. 8-bit are transmitted/received (LSB first)
1	0	1	Timer 1/2 overflow rate	8-bit UART 10 bits are transmitted (through TxD) or received (RxD)
2	1	0	fosc/ 32 or fosc/ 64	9-bit UART 11bits are transmitted (TxD) or received (RxD)
3	1	1	Timer 1/2 overflow rate	9-bit UART Like mode 2 except the variable baud rate

Table 7
Formulas for Calculating Baud rates

Baud Rate derived from	Interface Mode	Baud rate
Oscillator	0 2	fosc/ 12 $(2^{SMOD} \times f_{OSC}) / 64$
Timer 1 (16-bit timer) (8-bit timer with 8-bit autoreload)	1,3 1,3	$(2^{SMOD} \times$ timer 1 overflow rate) /32 $(2^{SMOD} \times f_{OSC}) /(32 \times 12 \times (256-TH1))$
Timer2	1,3	fosc / (32 × (65536-(RC2H, RC2L))

Interrupt System

The GMS80C501/301 provides 6 interrupt sources with two priority levels. **Figure 3** gives a general overview of the interrupt sources and illustrates the request and control flags.

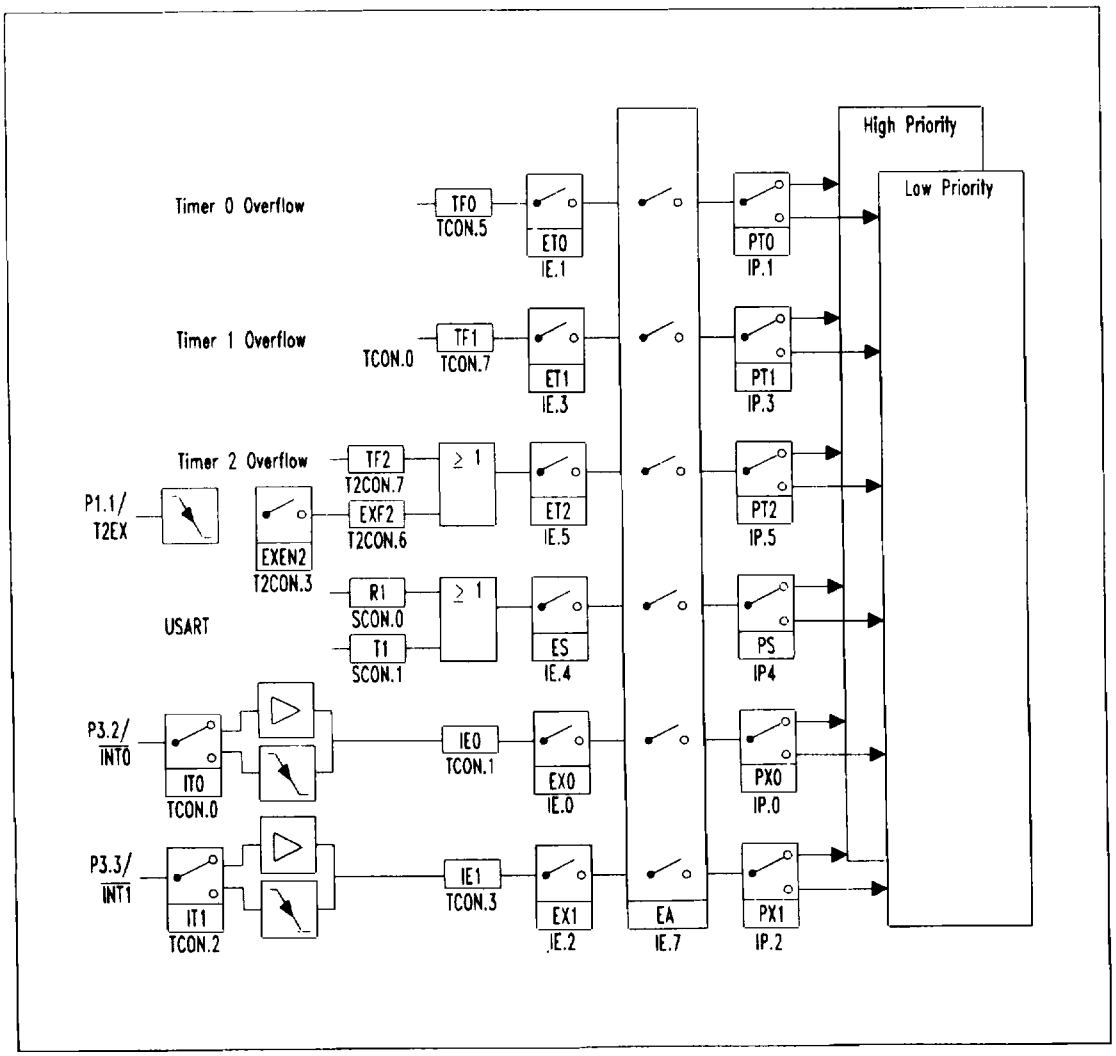


Figure 3
Interrupt Request Sources

Table 8

Interrupt Sources and their Corresponding Interrupt Vectors

Source (Request Flags)	Vector	Vector Address
IE0	External interrupt 0	0003_H
TF0	Timer 0 interrupt	$000B_H$
IE1	External interrupt 1	0013_H
TF1	Timer 1 interrupt	$001B_H$
RI + TI	Serial port interrupt	0023_H
TF2 + EXF2	Timer 2 interrupt	002BH

A low-priority interrupt can itself be interrupted by a high-priority interrupt, but not by another low priority interrupt. A high-priority interrupt cannot be interrupted by any other interrupt source.

If two requests of different priority level are received simultaneously, the request of higher priority is serviced. If requests of the same priority are received simultaneously, an internal polling sequence determines which request is serviced. Thus within each priority level there is a second priority structure determined by the polling sequence as shown in **table 9.**

Table 9

Interrupt Priority-Within-Level

Interrupt Source		Priority
External Interrupt 0,	IE0	High
Timer 0 Interrupt,	TF0	
External Interrupt 1,	IE1	
Timer 1 Interrupt,	TF1	
Serial Channel,	RI + TI	
Timer 2 Interrupt	TF2 + EXF2	Low

Power Saving Modes

Two power down modes are available, the Idle Mode and Power Down Mode.
The bits PDE and IDLE of the register PCON select the Power Down mode or the Idle mode, respectively. If the Power Down mode and the Idle mode are set at the same time, the Power Down mode takes precedence. **Table 10** gives a general overview of the power saving modes.

Table 10
Power Saving Modes Overview

Mode	Entering Instruction Example	Leaving by	Remarks
Idle mode	ORL PCON, #01H	- enabled interrupt - Hardware Reset	CPU is gated off CPU status registers maintain their data. Peripherals are active
Power-down Mode	ORL PCON, #02H	Hardware Reset	Oscillator is stopped, contents of on-chip RAM and SFR's are maintained (leaving Power Down Mode means redefinition of SFR contents).

In the Power Down mode of operation, V_{CC} can be reduced to minimize power consumption. It must be ensured, however, that V_{CC} is not reduced before the Power Down mode is invoked, and that V_{CC} is restored to its normal operating level, before the Power Down mode is terminated. The reset signal that terminates the Power down mode also restarts the oscillator. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize (similar to power-on reset).

Absolute Maximum Ratings

Ambient temperature under bias (T_A) .....-40 to + 85℃
Storage temperature (T_{ST}) .....-65 to + 150 ℃

Voltage on V_{CC} pins with respect to ground (V_{SS}) .....-0.5 V to 6.5 V
Voltage on any pin with respect to ground (V_{SS}) .....-0.5 to V_{CC} + 0.5 V

Input current on any pin during overload condition .....-10 mA to + 10 mA
Absolute sum of all input currents during overload condition ..... | 100 mA |

Power dissipation .....TBD

***Note** : Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for longer periods may affect device reliability. During overload conditions ($V_{IN} > V_{CC}$ or $V_{IN} < V_{SS}$) the Voltage on V_{CC} pins with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.*

DC Characteristics

V_{CC} = 5 V + 10%, - 15%; V_{SS} = 0 V; T_A = 0℃ to 70℃ for the GMS80C501/301

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input low voltage (except $\overline{EA}$, RESET)	V_{IL}	-0.5	0.2 V_{CC} - 0.1	V	-
Input low voltage ($\overline{EA}$)	$V_{IL\,1}$	-0.5	0.2 V_{CC} - 0.3	V	-
Input low voltage (RESET)	$V_{IL\,2}$	-0.5	0.2 V_{CC} + 0.1	V	-
Input high voltage (except XTAL1, $\overline{EA}$, RESET)	V_{IH}	0.2V_{CC} + 0.9	V_{CC} + 0.5	V	-
Input high voltage to XTAL1	$V_{IH\,1}$	0.7V_{CC}	V_{CC} + 0.5	V	
Input high voltage to $\overline{EA}$, RESET	$V_{IH\,2}$	0.6V_{CC}	V_{CC} + 0.5	V	-
Output low voltage (ports 1, 2, 3)	V_{OL}	-	0.45	V	I_{OL} = 1.6mA[1]
Output high voltage (port 0, ALE, $\overline{PSEN}$)	$V_{OL\,1}$	-	0.45	V	I_{OL} = 3.2mA[1]
Output high voltage (ports 1, 2, 3)	V_{OH}	2.4 0.9 V_{CC}	- -	V	I_{OH} = - 80 μA , I_{OH} = - 10 μA
Output high voltage (port 0 in external bus mode, ALE, $\overline{PSEN}$)	$V_{OH\,1}$	2.4 0.9V_{CC}	- -	V	I_{OH} = - 800 μA [2], I_{OH} = - 80 μA [2]
Logic 0 input current (ports 1, 2, 3)	I_{IL}	-10	-50	μA	V_{IN} = 0.45V
Logical 1-to-0 transition current (ports 1, 2, 3)	I_{TL}	-65	-650	μA	V_{IN} = 2V
Input leakage current (port 0, $\overline{EA}$)	I_{LI}	-	±1	μA	0.45 < V_{IN} < V_{CC}
Pin capacitance	C_{IO}	-	10	pF	f_C = 1MHz T_A = 25℃
Power supply current: Active mode, 12MHz[6] Idle mode, 12MHz[6] Active mode, 24 MHz[6] Idle mode, 24MHz[6] Active mode, 40 MHz[6] Idle mode, 40 MHz[6] Power Down Mode	 I_{CC} I_{CC} I_{CC} I_{CC} I_{CC} I_{CC} I_{PD}	 - - - - - - -	 21 4.8 36.2 8.2 56.5 12.5 50	 mA mA mA mA mA mA mA	 V_{CC} = 5V, [4] V_{CC} = 5V, [5] V_{CC} = 5V, [4] V_{CC} = 5V, [5] V_{CC} = 5V, [4] V_{CC} = 5V, [5] V_{CC} = 2 ... 5.5V[3]

1) Capacitive loading on ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL} of ALE and port 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operation. In the worst case (capacitive loading > 100pF), the noise pulse on ALE line may exceed 0.8V. In such cases it may be desirable to qualify ALE with a schmitt-trigger, or use an address latch with a schmitt-trigger strobe input.

2) Capacitive loading on ports0 and 2 may cause the V_{OH} on ALE and $\overline{PSEN}$ to momentarily fall bellow the $0.9V_{CC}$ specification when the address lines are stabilizing.

3) I_{PD} (Power Down Mode) is measured under following conditions:
$\overline{EA}$ = Port0 = V_{CC}; RESET = V_{SS}; XTAL2 = N.C.; XTAL1 = V_{SS}; all other pins are disconnected.

4) I_{CC} (active mode) is measured with:
XTAL1 driven with t_{CLCH}, t_{CHCL} = 5ns, V_{IL} = V_{SS} + 0.5V, V_{IH} = V_{CC} - 0.5V; XTAL2 = N.C.;
$\overline{EA}$ = Port0 = RESET = V_{CC}; all other pins are disconnected. I_{CC} would be slightly higher if a crystal oscillator is used (appr. 1mA).

5) I_{CC} (Idle mode) is measured with all output pins disconnected and with all peripherals disabled;
XTAL1 driven with t_{CLCH}, t_{CHCL} = 5ns, V_{IL} = V_{SS} + 0.5V, V_{IH} = V_{CC} - 0.5V; XTAL2 = N.C.;
RESET = $\overline{EA}$ = V_{SS}; Port0 = V_{CC}; all other pins are disconnected;

6) $I_{CC\ max}$ at other frequencies is given by:
active mode: $I_{CC} = 1.27 \times f_{OSC} + 5.73$
idle mode: $I_{CC} = 0.28 \times f_{OSC} + 1.45$
where f_{OSC} is the oscillator frequency in MHz. I_{CC} values are given in mA and measured at V_{CC} = 5V.

AC Characteristics for GMS80C501/301

V_{CC} = 5V + 10%, -15%; V_{SS} = 0V

T_A = 0℃ to 70℃ for the GMS80C501/301

(C_L for port 0, ALE and $\overline{PSEN}$ outputs = 100pF; C_L for all other outputs = 80 pF)

Program Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		12 MHz Clock		Variable Clock $1/t_{CLCL}$ = 3.5 MHz to 12 MHz		
		min.	max.	min.	max.	
ALE pulse width	t_{LHLL}	127	-	$2t_{CLCL}$ - 40	-	ns
Address setup to ALE	t_{AVLL}	43	-	t_{CLCL} - 40	-	ns
Address hold after ALE	t_{LLAX}	30	-	t_{CLCL} -53	-	ns
ALE low to valid instr in	t_{LLIV}	-	233	-	$4t_{CLCL}$ - 100	ns
ALE to $\overline{PSEN}$	t_{LLPL}	58	-	t_{CLCL} - 25	-	ns
$\overline{PSEN}$ pulse width	t_{PLPH}	215	-	$3t_{CLCL}$ - 35	-	ns
$\overline{PSEN}$ to valid instr in	t_{PLIV}	-	150	-	$3t_{CLCL}$ - 100	ns
Input instruction hold after $\overline{PSEN}$	t_{PXIX}	0	-	0	-	ns
Input instruction float after $\overline{PSEN}$	t_{PXIZ}*)	-	63	-	t_{CLCL} - 20	ns
Address valid after $\overline{PSEN}$	t_{PXAV}*)	75	-	t_{CLCL} - 8	-	ns
Address to valid instr in	t_{AVIV}	-	302	-	$5t_{CLCL}$ - 115	ns
Address float to $\overline{PSEN}$	t_{AZPL}	0	-	0	-	ns

*) Interfacing the GMS80C501/301 to devices with float times up to 75 ns is permissible. This limited bus contention will not cause any damage to port 0 Drivers.

AC Characteristics for GMS80C501/301

External Data Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		12 MHz Clock		Variable Clock $1/t_{CLCL}$ = 3.5 MHz to 12 MHz		
		min.	max.	min.	max.	
$\overline{RD}$ pulse width	t_{RLRH}	400	-	$6t_{CLCL}$ - 100	-	ns
$\overline{WR}$ pulse width	t_{WLWH}	400	-	$6t_{CLCL}$ - 100	-	ns
Address hold after ALE	t_{LLAX2}	30	-	t_{CLCL} -53	-	ns
$\overline{RD}$ to valid data in	t_{RLDV}	-	252	-	$5t_{CLCL}$ - 165	ns
Data hold after $\overline{RD}$	t_{RHDX}	0	-	0	-	ns
Data float after $\overline{RD}$	t_{RHDZ}	-	97	-	$2t_{CLCL}$ - 70	ns
ALE to valid data in	t_{LLDV}	-	517	-	$8t_{CLCL}$ - 150	ns
Address to valid data in	t_{AVDV}	-	585	-	$9t_{CLCL}$ - 165	ns
ALE to $\overline{WR}$ or $\overline{RD}$	t_{LLWL}	200	300	$3t_{CLCL}$ - 50	$3t_{CLCL}$ +50	ns
Address valid to $\overline{WR}$ or $\overline{RD}$	t_{AVWL}	203	-	$4t_{CLCL}$ - 130	-	ns
$\overline{WR}$ or $\overline{RD}$ high to ALE high	t_{WHLH}	43	123	t_{CLCL} - 40	t_{CLCL} +40	ns
Data valid to $\overline{WR}$ transition	t_{QVWX}	33	-	t_{CLCL} - 50	-	ns
Data setup before $\overline{WR}$	t_{QVWH}	433	-	$7t_{CLCL}$ - 150	-	ns
Data hold after $\overline{WR}$	t_{WHQX}	33	-	t_{CLCL} - 50	-	ns
Address float after $\overline{RD}$	t_{RLAZ}	-	0	-	0	ns

External Clock Drive

Parameter	Symbol	Limit Values		Unit
		Variable Clock Freq. = 3.5 MHz to 12 MHz		
		min.	max.	
Oscillator period	t_{CLCL}	83.3	285.7	ns
High time	t_{CHCX}	20	$t_{CLCL} - t_{CLCX}$	ns
Low time	t_{CLCX}	20	$t_{CLCL} - t_{CHCX}$	ns
Rise time	t_{CLCH}	-	20	ns
Fall time	t_{CHCL}	-	20	ns

AC Characteristics for GMS80C501-24/301-24

V_{CC} = 5V + 10%, - 15%; V_{SS} = 0 V

T_A = 0℃ to 70℃ for the GMS80C501-24/301-24

(C_L for port 0, ALE and $\overline{PSEN}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

Program Memory characteristics

Parameter	Symbol	Limit Values				Unit
		24 MHz Clock		Variable Clock $1/t_{CLCL}$ = 3.5 MHz to 24 MHz		
		min.	max.	min.	max.	
ALE pulse width	t_{LHLL}	43	-	$2t_{CLCL}$ - 40	-	ns
Address setup to ALE	t_{AVLL}	17	-	t_{CLCL} - 25	-	ns
Address hold after ALE	t_{LLAX}	17	-	t_{CLCL} - 25	-	ns
ALE low to valid instr in	t_{LLIV}	-	80	-	$4t_{CLCL}$ - 87	ns
ALE to $\overline{PSEN}$	t_{LLPL}	22	-	t_{CLCL} - 20	-	ns
$\overline{PSEN}$ pulse width	t_{PLPH}	95	-	$3t_{CLCL}$ - 30	-	ns
$\overline{PSEN}$ to valid instr in	t_{PLIV}	-	60	-	$3t_{CLCL}$ - 65	ns
Input instruction hold after $\overline{PSEN}$	t_{PXIX}	0	-	0	-	ns
Input instruction float after $\overline{PSEN}$	t_{PXIZ}*)	-	32	-	t_{CLCL} - 10	ns
Address valid after $\overline{PSEN}$	t_{PXAV}*)	37	-	t_{CLCL} - 5	-	ns
Address to valid instr in	t_{AVIV}	-	148	-	$5t_{CLCL}$ - 60	ns
Address float to $\overline{PSEN}$	t_{AZPL}	0	-	0	-	ns

*) Interfacing the GMS80C501/301 to devices with float times up to 35 ns is permissible. This limited bus contention wil not cause any damage to port 0 Drivers.

AC characteristics for GMS80C501-24/C301-24

External Data Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		24 MHz Clock		Variable Clock $1/t_{CLCL}$ = 3.5 MHz to 24 MHz		
		min.	max.	min.	max.	
$\overline{RD}$ pulse width	t_{RLRH}	180	-	$6t_{CLCL}$ - 70	-	ns
$\overline{WR}$ pulse width	t_{WLWH}	180	-	$6t_{CLCL}$ - 70	-	ns
Address hold after ALE	t_{LLAX2}	15	-	t_{CLCL} - 27	-	ns
$\overline{RD}$ to valid data in	t_{RLDV}	-	118	-	$5t_{CLCL}$ - 90	ns
Data hold after $\overline{RD}$	t_{RHDX}	0	-	0	-	ns
Data float after $\overline{RD}$	t_{RHDZ}	-	63	-	$2t_{CLCL}$ - 20	ns
ALE to valid data in	t_{LLDV}	-	200	-	$8t_{CLCL}$ - 133	ns
Address to valid data in	t_{AVDV}	-	220	-	$9t_{CLCL}$ - 155	ns
ALE to $\overline{WR}$ or $\overline{RD}$	t_{LLWL}	75	175	$3t_{CLCL}$ - 50	$3t_{CLCL}$ + 50	ns
Address valid to $\overline{WR}$ or $\overline{RD}$	t_{AVWL}	67	-	$4t_{CLCL}$ - 97	-	ns
$\overline{WR}$ or $\overline{RD}$ high to ALE high	t_{WHLH}	17	67	t_{CLCL} - 25	t_{CLCL} + 25	ns
Data valid to $\overline{WR}$ transition	t_{QVWX}	5	-	t_{CLCL} - 37	-	ns
Data setup before $\overline{WR}$	t_{QVWH}	170	-	$7t_{CLCL}$ - 122	-	ns
Data hold after $\overline{WR}$	t_{WHQX}	15	-	t_{CLCL} - 27	-	ns
Address float after $\overline{RD}$	t_{RLAZ}	-	0	-	0	ns

External Clock Drive

Parameter	Symbol	Limit Values		Unit
		Variable Clock Freq. = 3.5 MHz to 24 MHz		
		min.	max.	
Oscillator period	t_{CLCL}	41.7	285.7	ns
High time	t_{CHCX}	12	$t_{CLCL} - t_{CLCX}$	ns
Low time	t_{CLCX}	12	$t_{CLCL} - t_{CHCX}$	ns
Rise time	t_{CLCH}	-	12	ns
Fall time	t_{CHCL}	-	12	ns

AC Characteristics for GMS80C501-40/301-40

Advance Information

V_{CC} = 5V + 10%, -15%; V_{SS} = 0V

T_A = 0℃ to 70℃ for the GMS80C501-40/301-40

(C_L for port 0, ALE and $\overline{PSEN}$ outputs = 100pF; C_L for all other outputs =80pF)

Program Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		40 MHz Clock		Variable Clock $1/t_{CLCL}$ = 3.5 MHz to 40 MHz		
		min.	max.	min.	max.	
ALE pulse width	t_{LHLL}	35	-	$2t_{CLCL}$ - 15	-	ns
Address setup to ALE	t_{AVLL}	10	-	t_{CLCL} - 15	-	ns
Address hold after ALE	t_{LLAX}	10	-	t_{CLCL} - 15	-	ns
ALE low to valid instr in	t_{LLIV}	-	55	-	$4t_{CLCL}$ - 45	ns
ALE to $\overline{PSEN}$	t_{LLPL}	10	-	t_{CLCL} - 15	-	ns
$\overline{PSEN}$ pulse width	t_{PLPH}	60	-	$3t_{CLCL}$ - 15	-	ns
$\overline{PSEN}$ to valid instr in	t_{PLIV}	-	25	-	$3t_{CLCL}$ - 50	ns
Input instruction hold after $\overline{PSEN}$	t_{PXIX}	0	-	0	-	ns
Input instruction float after $\overline{PSEN}$	t_{PXIZ}*)	-	15	-	t_{CLCL} - 10	ns
Address valid after $\overline{PSEN}$	t_{PXAV}*)	20	-	t_{CLCL} - 5	-	ns
Address to valid instr in	t_{AVIV}	-	65	-	$5t_{CLCL}$ - 60	ns
Address float to $\overline{PSEN}$	t_{AZPL}	-5	-	- 5	-	ns

*) Interfacing the GMS80C501/301 to devices with float times up to 35 ns is permissible. This limited bus contention will not cause any damage to port 0 Drivers.

AC Characteristics for GMS80C501-40/301-40 (cont'd)

Advance Information

External Data Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		40 MHz Clock		Variable Clock $1/t_{CLCL}$ = 3.5 MHz to 40 MHz		
		min.	max.	min.	max.	
$\overline{RD}$ pulse width	t_{RLRH}	120	-	$6t_{CLCL}$ - 30	-	ns
$\overline{WR}$ pulse width	t_{WLWH}	120	-	$6t_{CLCL}$ - 30	-	ns
Address hold after ALE	t_{LLAX2}	10	-	$2t_{CLCL}$ - 15	-	ns
$\overline{RD}$ to valid data in	t_{RLDV}	-	75	-	$5t_{CLCL}$ - 50	ns
Data hold after $\overline{RD}$	t_{RHDX}	0	-	0	-	ns
Data float after $\overline{RD}$	t_{RHDZ}	-	38	-	$2t_{CLCL}$ - 12	ns
ALE to valid data in	t_{LLDV}	-	150	-	$8t_{CLCL}$ - 50	ns
Address to valid data in	t_{AVDV}	-	150	-	$9t_{CLCL}$ - 75	ns
ALE to $\overline{WR}$ or $\overline{RD}$	t_{LLWL}	60	90	$3t_{CLCL}$ - 15	$3t_{CLCL}$ + 15	ns
Address valid to $\overline{WR}$ or $\overline{RD}$	t_{AVWL}	70	-	$4t_{CLCL}$ - 30	-	ns
$\overline{WR}$ or $\overline{RD}$ high to ALE high	t_{WHLH}	10	40	t_{CLCL} - 15	t_{CLCL} + 15	ns
Data valid to $\overline{WR}$ transition	t_{QVWX}	5	-	t_{CLCL} - 20	-	ns
Data setup before $\overline{WR}$	t_{QVWH}	125	-	$7t_{CLCL}$ - 50	-	ns
Data hold after $\overline{WR}$	t_{WHQX}	5	-	t_{CLCL} - 20	-	ns
Address float after $\overline{RD}$	t_{RLAZ}	-	0	-	0	ns

Advance Information

External Clock Drive

Parameter	Symbol	Limit Values		Unit
		Variable Clock Freq. = 3.5 MHz to 40 MHz		
		min.	max.	
Oscillator period	t_{CLCL}	25	285.7	ns
High time	t_{CHCX}	10	$t_{CLCL} - t_{CLCX}$	ns
Low time	t_{CLCX}	10	$t_{CLCL} - t_{CHCX}$	ns
Rise time	t_{CLCH}	-	10	ns
Fall time	t_{CHCL}	-	10	ns

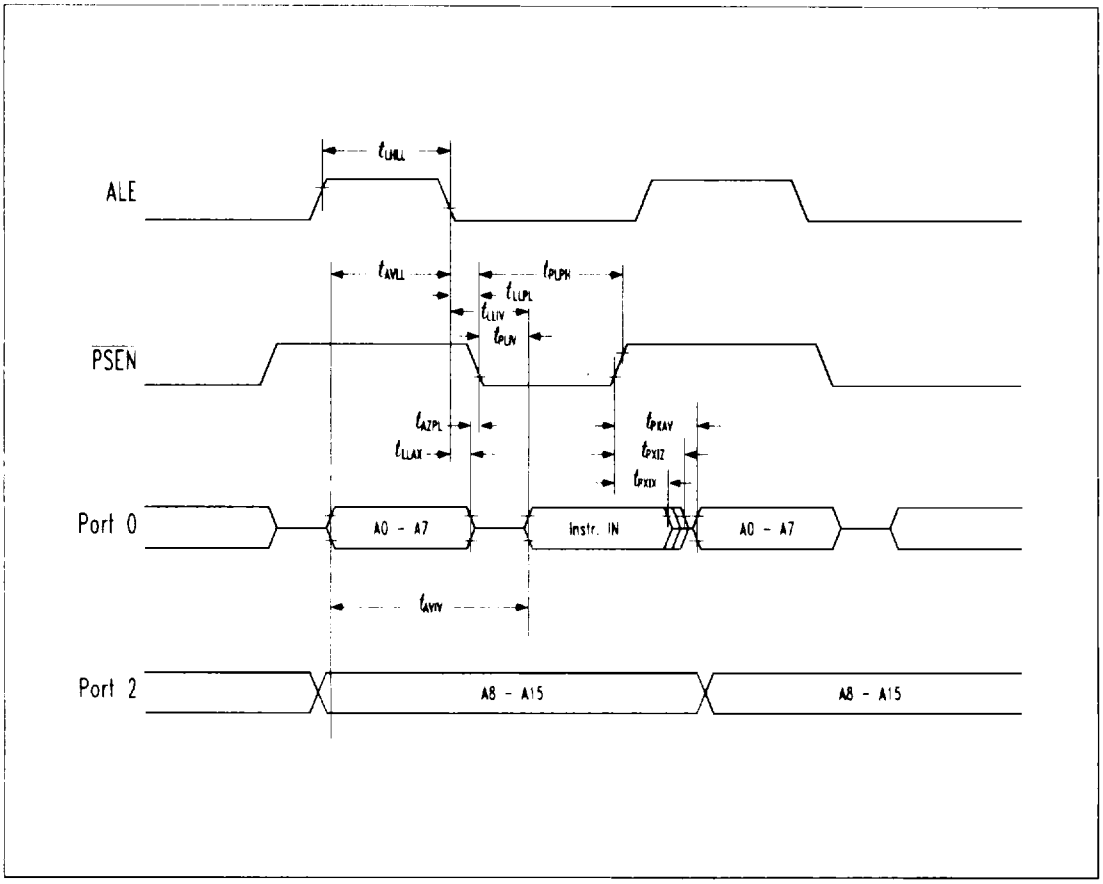


Figure4
Program Memory Read Cycle

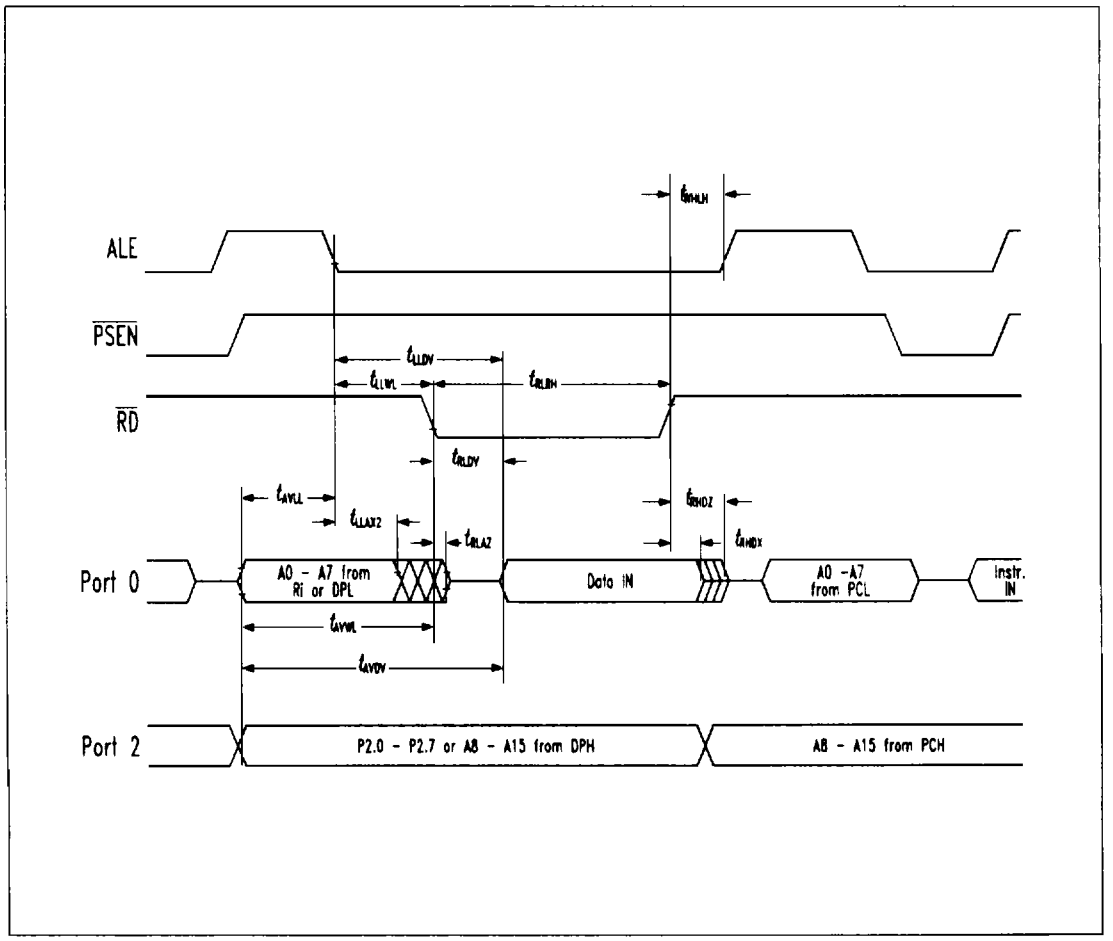


Figure 5
Data Memory Read Cycle

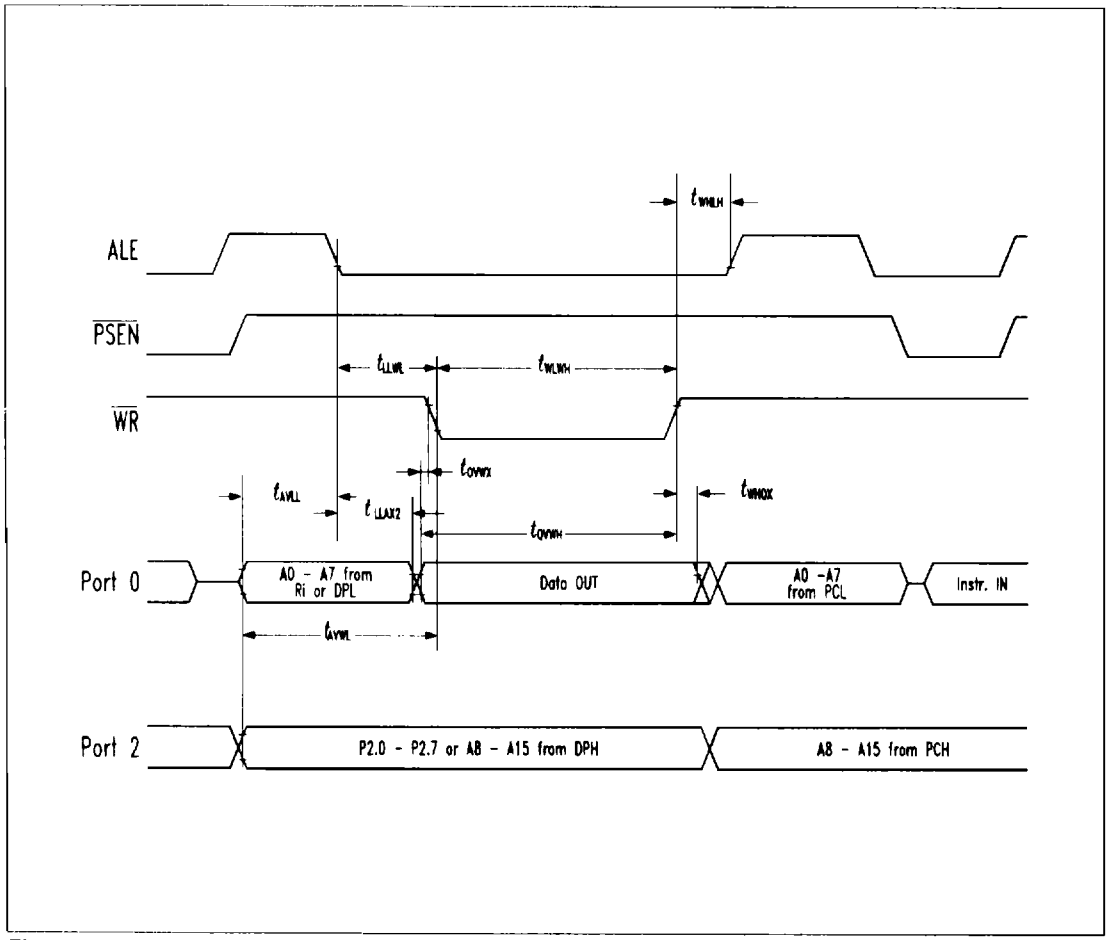


Figure 6
Data Memory Write Cycle

ROM Verification Characteristics for GMS80C301

ROM Verification Mode 1

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Address to valid data	t_{AVQV}	-	$48t_{CLCL}$	ns
ENABLE to valid data	t_{ELQV}	-	$48t_{CLCL}$	ns
Data float after ENABLE	t_{EHQZ}	0	$48t_{CLCL}$	ns
Oscillator frequency	$1/t_{CLCL}$	4	6	MHz

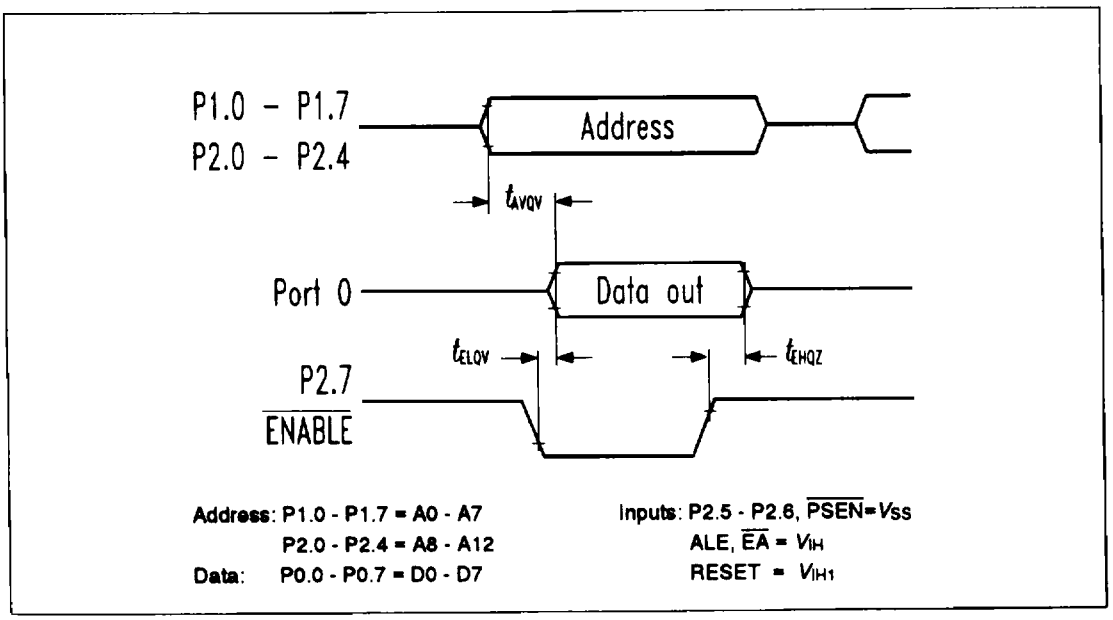
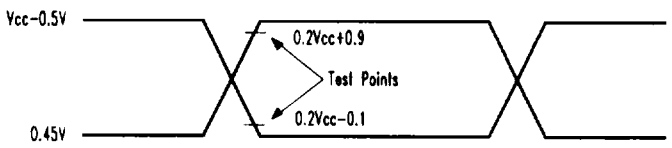


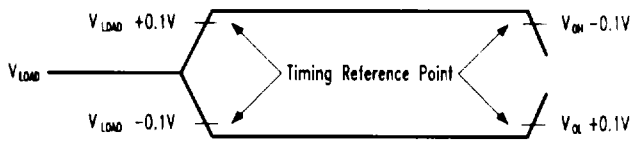
Figure 7
ROM Verification Mode 1



AC Inputs during testing are driven at V_{CC} - 0.5V for a logic '1' and 0.45V for a logic '0'. Timing measurements are made at V_{IHmin} for a logic '1' and V_{ILmax} for a logic '0'.

Figure8

AC Testing : Input, Output Waveforms



For timing purposes a port pin is no longer floating when a 100mV change from load voltage occurs and begins to float when a 100mV change from the loaded V_{OH} / V_{OL} level occurs.
I_{OL} / I_{OH} ≥ 20mA.

Figure 9

AC Testing : Float Waveforms

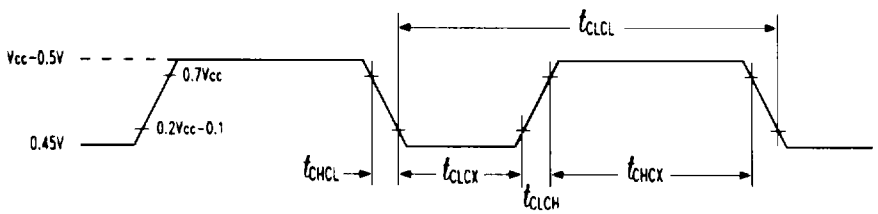


Figure 10

External Clock Cycle

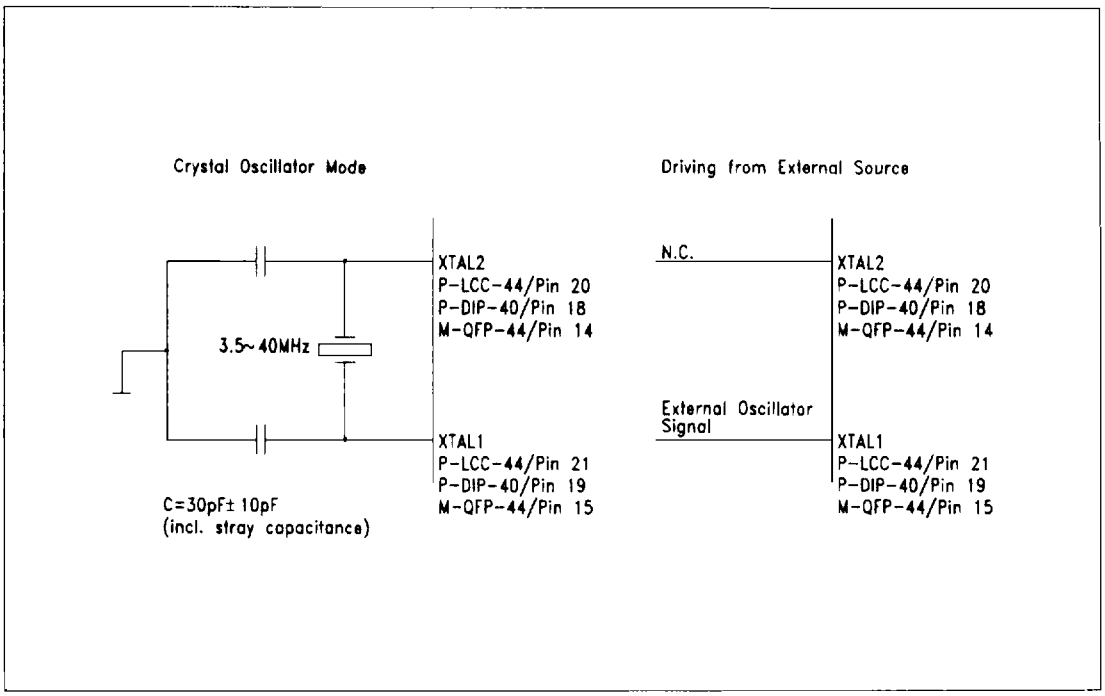
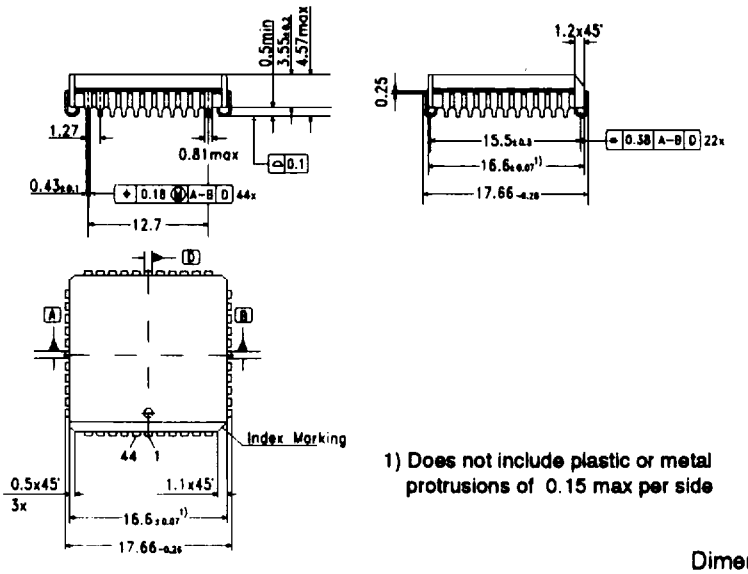


Figure 11
Recommended Oscillator Circuits

Package Outlines

Plastic Package, P-LCC-44-SMD
(Plastic Leaded Chip-Carrier)



1) Does not include plastic or metal protrusions of 0.15 max per side

Dimensions in mm

SMD = Surface Mounted Device

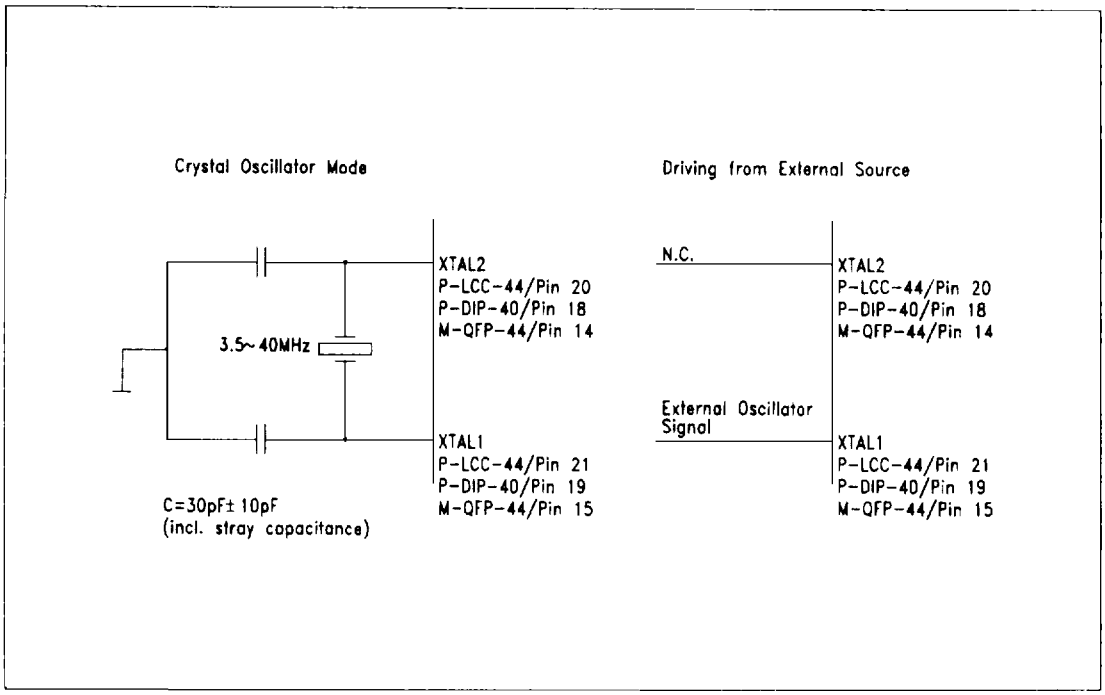
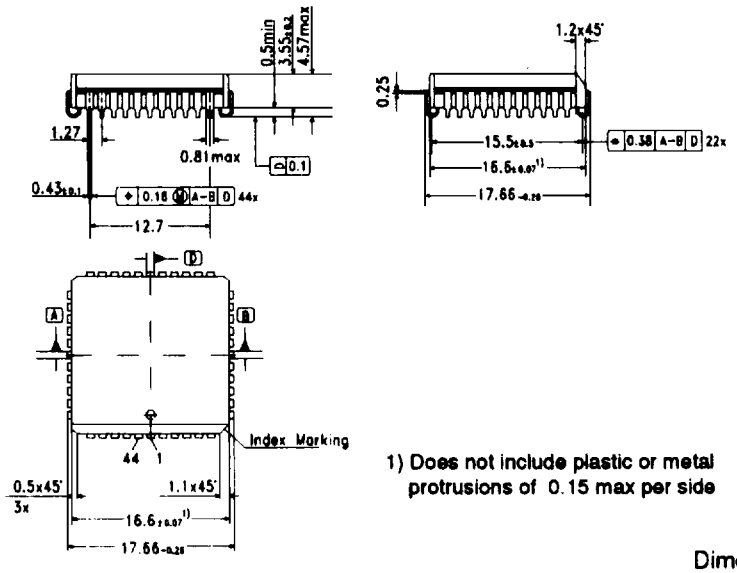


Figure 11
Recommended Oscillator Circuits

Package Outlines

Plastic Package, P-LCC-44-SMD
(Plastic Leaded Chip-Carrier)

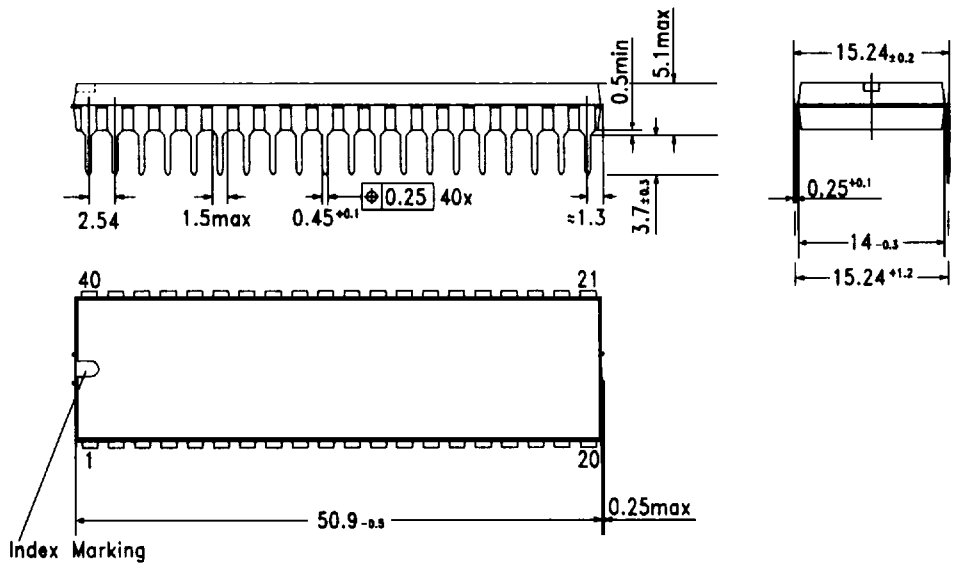


1) Does not include plastic or metal protrusions of 0.15 max per side

Dimensions in mm

SMD = Surface Mounted Device

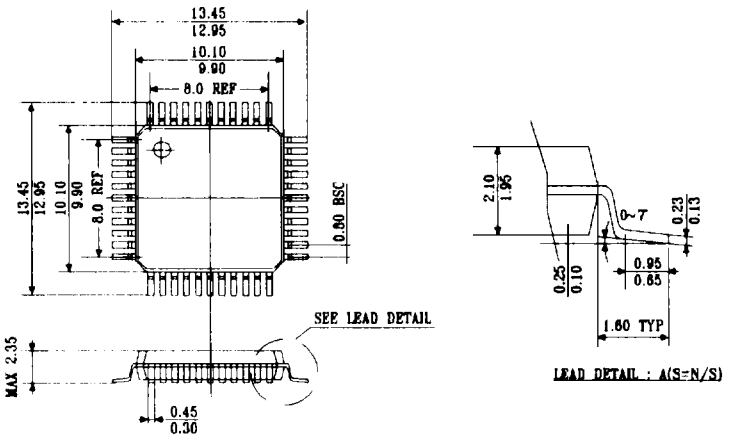
Plastic Package, P-DIP-40
(Plastic Dual in-Line Package)



Dimensions in mm

Package Outlines

Plastic Package, P-MQFP-44 (SMD)
(Plastic Metric Quad Flat Package)



1) Does not include plastic or metal protrusions of 0.25 max per side

Dimensions in mm

SMD = Surface Mounted Device