10-bit, 500 Msps Digital-to-Analog Converter (DAC)

TDA8776

FEATURES

- 10-bit resolution
- Conversion rate up to 500 MHz
- 10K/100K ECL input levels
- Internal reference voltage generator
- No deglitching circuit required
- Internal input register
- Power dissipation only 925 mW (typical)
- Internal 50 Ω output load (connected to the analog ground)
- Very few external components required.

APPLICATIONS

High-speed digital-to-analog conversion for:

- High resolution video and graphics
- Direct Digital Synthesis (DDS)
- Telecommunication
- High-speed modems.

GENERAL DESCRIPTION

The TDA8776 is a 10-bit Digital-to-Analog Converter (DAC) for high resolution video and other high frequency applications. It converts the digital input signal into an analog output voltage at a maximum conversion rate of 500 Msps. No external reference voltage is required and all digital inputs are 10K/100K-ECL compatible.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{EEA}	analog supply voltage		−5.46	−5.20	−4.94	V
V_{EED}	digital supply voltage		−5.46	−5.20	−4.94	V
V_{EEI}	input stages digital supply voltage	note 1	−5.46	−5.20	−4.94	V
I_{EEA}	analog supply current	note 1	–	108	145	mA
I_{EED}	digital supply current	note 1	–	60	85	mA
I_{EEI}	input stages digital supply current	note 1	–	10	15	mA
$V_{OUT} - V_{\overline{OUT}}$	full-scale analog output voltage (peak-to-peak value)	notes 1 and 2; Z_L = 50 Ω	1.7	2.0	2.5	V
INL	DC integral non-linearity	note 3	–	±0.3	±0.5	LSB
DNL	DC differential non-linearity	note 3	–	±0.2	±0.45	LSB
$f_{clk(max)}$	maximum clock frequency		500	–	–	MHz
t_{S1}	settling time (differential)	10% to 90% full scale; Fig.9	–	0.5	–	ns
P_{tot}	total power dissipation		–	925	–	mW

Notes

1. D0 to D9 connected to either HIGH or LOW level, CLK is HIGH and $\overline{CLK}$ is LOW.
2. The analog output voltages (V_{OUT} and $V_{\overline{OUT}}$) are negative with respect to AGND (see Table 1). The external output resistance between AGND and each of these outputs is typically 50 Ω.
3. A warm-up time is necessary to reach optimal performances.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8776K	PLCC28	plastic leaded chip carrier; 28 leads	SOT261-2

10-bit, 500 Msps Digital-to-Analog Converter (DAC) — TDA8776

BLOCK DIAGRAM

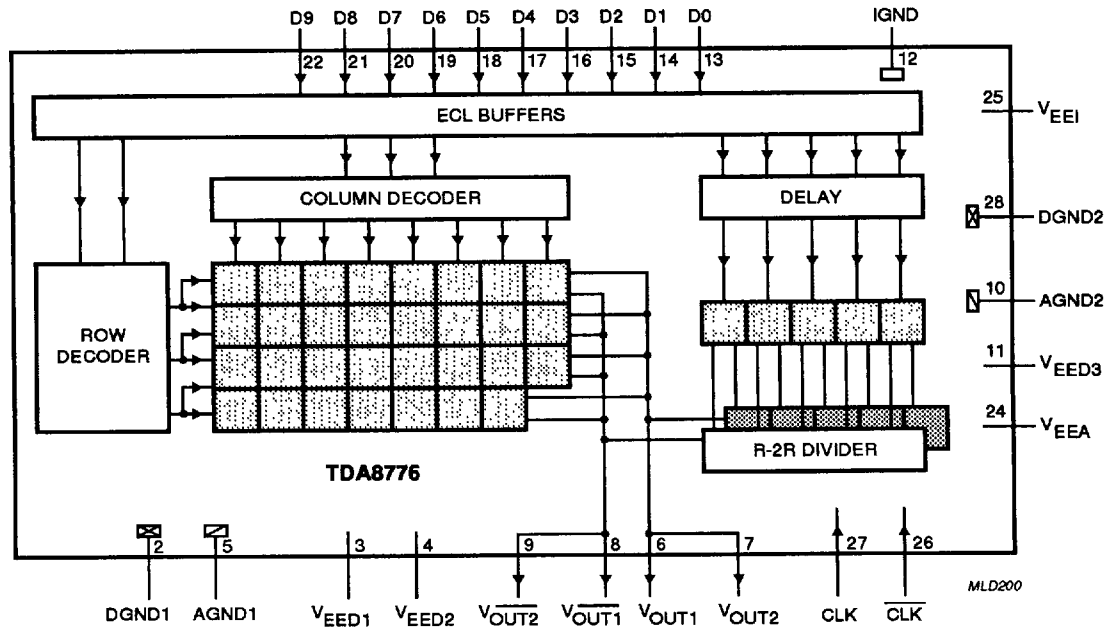


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
DGND1	2	digital ground 1
V_{EED1}	3	digital supply voltage 1 (−5.2 V)
V_{EED2}	4	digital supply voltage 2 (−5.2 V)
AGND1	5	analog ground 1
V_{OUT1}	6	analog voltage output 1
V_{OUT2}	7	analog voltage output 2
$V_{\overline{OUT1}}$	8	complementary analog voltage output 1
$V_{\overline{OUT2}}$	9	complementary analog voltage output 2
AGND2	10	analog ground 2
V_{EED3}	11	digital supply voltage 3 (−5.2 V)
IGND	12	input ground for ECL input buffers
D0	13	data input; bit 0 (LSB)
D1	14	data input; bit 1

SYMBOL	PIN	DESCRIPTION
D2	15	data input; bit 2
D3	16	data input; bit 3
D4	17	data input; bit 4
D5	18	data input; bit 5
D6	19	data input; bit 6
D7	20	data input; bit 7
D8	21	data input; bit 8
D9	22	data input; bit 9 (MSB)
n.c.	23	not connected
V_{EEA}	24	analog supply voltage (−5.2 V)
V_{EEI}	25	input supply voltage for ECL input buffers (−5.2 V)
$\overline{CLK}$	26	complementary clock input
CLK	27	clock input
DGND2	28	digital ground 2

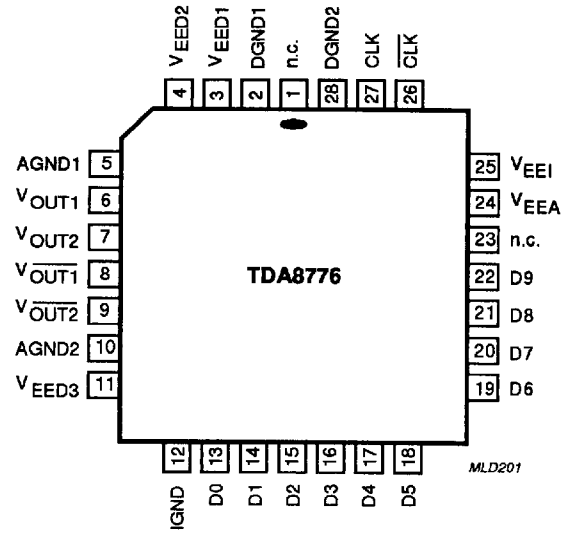


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{EEA}	analog supply voltage		−7.0	±0.3	V
V_{EED}	digital supply voltage		−7.0	±0.3	V
V_{EEI}	input stages digital supply voltage		−7.0	±0.3	V
$V_{EEA} - V_{EED}$	supply voltage differential		−0.5	+0.5	V
AGND − DGND	ground voltage differential		−0.1	+0.1	V
V_I	input voltage		V_{EEI}	±0.3	V
$I_{OUT}/\overline{I_{OUT}}$	total output current	Z_L = 50 Ω	−5	+50	mA
T_{stg}	storage temperature		−55	+150	°C
T_{amb}	operating ambient temperature		0	+70	°C
T_j	junction temperature		−	+150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	55 (typ.)	K/W

CHARACTERISTICS

V_{EEA} = V_{24} to V_5 and V_{10} = −5.46 to −4.94 V; V_{EED} = V_3, V_4 and V_{11} to V_2 and V_{28} = −5.46 to −4.94 V; V_{EEI} = V_{25} to V_{12} = −5.46 to −4.94 V; V_{EED} and V_{EEI} shorted together; T_{amb} = 0 to +70 °C; AGND, DGND and IGND shorted together; $V_{OUT} - V_{\overline{OUT}}$ = 2 V (p-p); Z_L = 50 Ω; unless otherwise specified (typical values measured at V_{EEA} = V_{EED} = −5.2 V and T_{amb} = 25 °C).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{EEA}	analog supply voltage		−5.46	−5.20	−4.94	V
V_{EED}	digital supply voltage		−5.46	−5.20	−4.94	V
V_{EEI}	input stages digital supply voltage	note 1	−5.46	−5.20	−4.94	V
I_{EEA}	analog supply current	note 1	–	108	145	mA
I_{EED}	digital supply current	note 1	–	60	85	mA
I_{EEI}	input stages digital supply current	note 1	–	10	15	mA
AGND – DGND	ground voltage differential		−0.1	–	+0.1	V
Inputs						
DIGITAL INPUTS (D9 TO D0) AND CLOCK INPUTS (CLK AND $\overline{CLK}$)						
V_{IL}	LOW level input voltage		−1.9	−1.8	−1.6	V
V_{IH}	HIGH level input voltage		−1.2	−0.9	−0.8	V
I_{IL}	LOW level input current	V_I = −1.8 V	–	–	10	µA
I_{IH}	HIGH level input current	V_I = −0.9 V	–	–	20	µA
$f_{clk(max)}$	maximum clock frequency		500	–	–	MHz
Outputs (referenced to AGND); notes 1 and 2						
$V_{OUT} - V_{\overline{OUT}}$	full-scale analog output voltage (peak-to-peak value)	Z_L = 50 Ω	1.7	2.0	2.5	V
Z_O	output impedance		–	50	–	Ω
Transfer function						
INL	DC integral non-linearity	note 3	–	±0.3	±0.5	LSB
DNL	DC differential non-linearity	note 3	–	±0.2	±0.45	LSB
Spurious free dynamic range (f_{clk} = 500 MHz); V_{EEA} = V_{EED} = 5.2 V; T_{amb} = 25 °C; note 4; see Fig.3						
SFDR	spurious free dynamic range					
	f_{OUT} = 10 MHz		−65	−69	–	dB
	f_{OUT} = 50 MHz		–	−60	–	dB
	f_{OUT} = 80 MHz		–	−59	–	dB
	f_{OUT} = 100 MHz		−52	−59	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Switching characteristics (f_{clk} = 500 MHz); notes 5 and 6; see Figs 8 and 9						
$t_{SU;DAT}$	data set-up time		–	400	500	ps
$t_{HD;DAT}$	data hold time		100	150	–	ps
t_{PD}	propagation delay time		–	0.8	0.9	ns
t_{S1}	settling time	10% to 90% full scale	–	0.5	–	ns
t_{S2}	settling time	change to ±1 LSB	–	2.0	–	ns
t_d	input to 50% output delay time		–	1.4	1.5	ns
Output transients; glitches (f_{clk} = 500 MHz); note 7; see Fig.10						
E_g	differential glitch energy from code	transition 511 to 512	–	1	2	pV.s

Notes

1. D0 to D9 connected to either HIGH or LOW level, CLK is HIGH and $\overline{CLK}$ is LOW.
2. The analog output voltages (V_{OUT} and $V_{\overline{OUT}}$) are negative with respect to AGND (see Table 1). The external output resistance between AGND and each of these outputs is typically 50 Ω.
3. Due to on-chip regulator behaviour a warm-up time is necessary to reach optimal performances; a typical time is 1 minute.
4. Devices with higher SFDR (min.) can be delivered on request.
5. The worst case characteristics are obtained at the transition from input code 0 to 1023 and if an external load impedance greater than 50 Ω is connected between V_{OUT} or $V_{\overline{OUT}}$ and AGND in parallel with the external 50 Ω load. The specified values have been measured directly on a 50 Ω load between V_{OUT} and AGND. No further load impedance between V_{OUT} and AGND has been applied. All input data is latched at the falling edge of the clock.
6. The data set-up ($t_{SU;DAT}$) is the minimum period preceding the falling edge of the clock that the input data must be stable in order to be correctly registered. A negative set-up time indicates that the data may be initiated after the falling edge of the clock and still be recognized. The data hold time ($t_{HD;DAT}$) is the minimum period following the falling edge of the clock that the input data must be stable in order to be correctly registered. A negative hold time indicates that the data may be released prior to the falling edge of the clock and still be recognized.
7. The definition of glitch energy and the measurement set-up are shown in Fig.10. The glitch energy is measured at the input transition between code 511 to 512.

Table 1 Input coding and DAC output voltages (typical values; referenced to AGND regardless of the offset voltage)

CODE	BINARY INPUT DATA										DAC OUTPUT VOLTAGES (V) Z_L = 50 Ω	
	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	V_{OUT}	$V_{\overline{OUT}}$
0	0	0	0	0	0	0	0	0	0	0	0	−1.0
1	0	0	0	0	0	0	0	0	0	1	−0.0010	−0.9990
.	.	.	.	.	.	.	.	.	.	.	.	.
512	1	0	0	0	0	0	0	0	0	0	−0.5	−0.5
.	.	.	.	.	.	.	.	.	.	.	.	.
1022	1	1	1	1	1	1	1	1	1	0	−0.9990	−0.0010
1023	1	1	1	1	1	1	1	1	1	1	−1.0	0

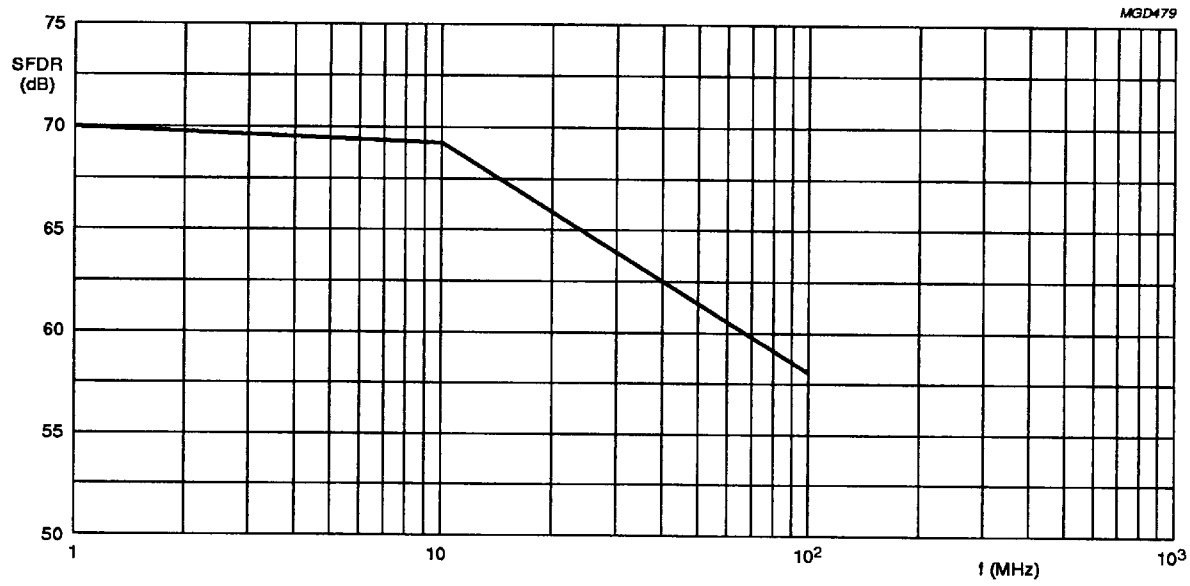


Fig.3 Typical spurious free dynamic range (SFDR) as a function of output frequency.

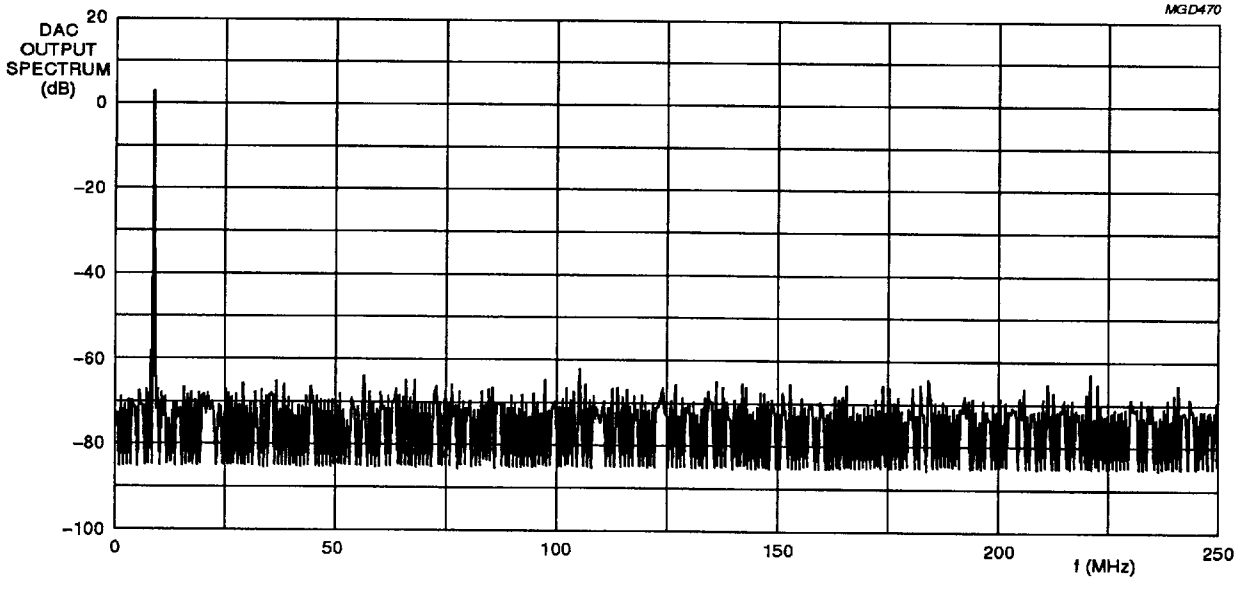


Fig.4 Typical output spectrum; f_{clk} = 500 MHz; f_{OUT} = 10 MHz.

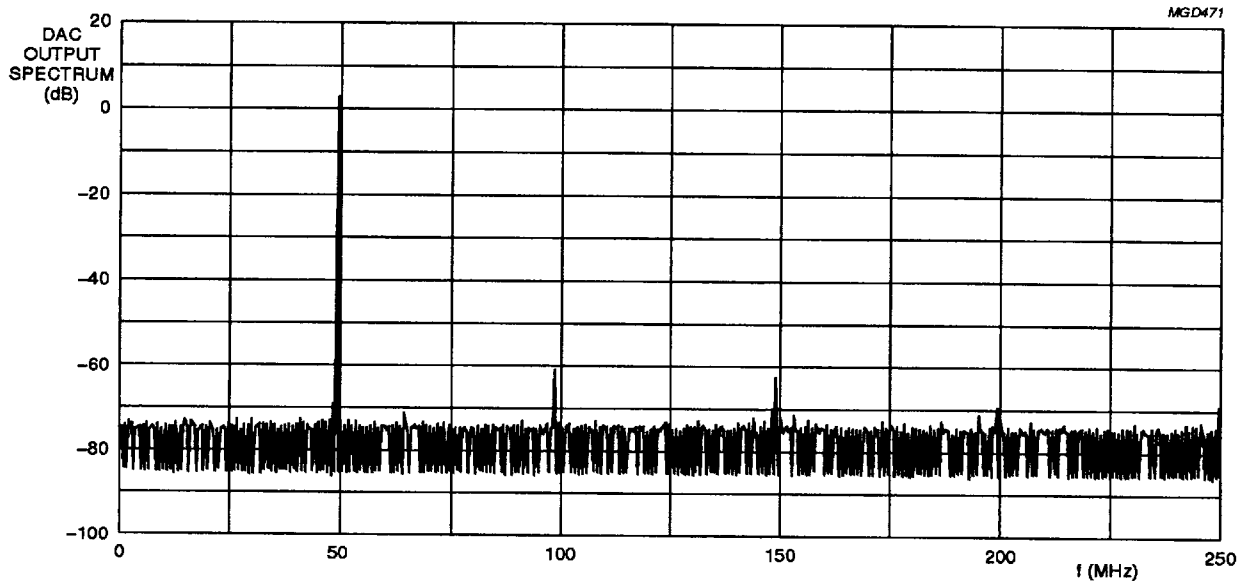


Fig.5 Typical output spectrum; f_{clk} = 500 MHz; f_{OUT} = 50 MHz.

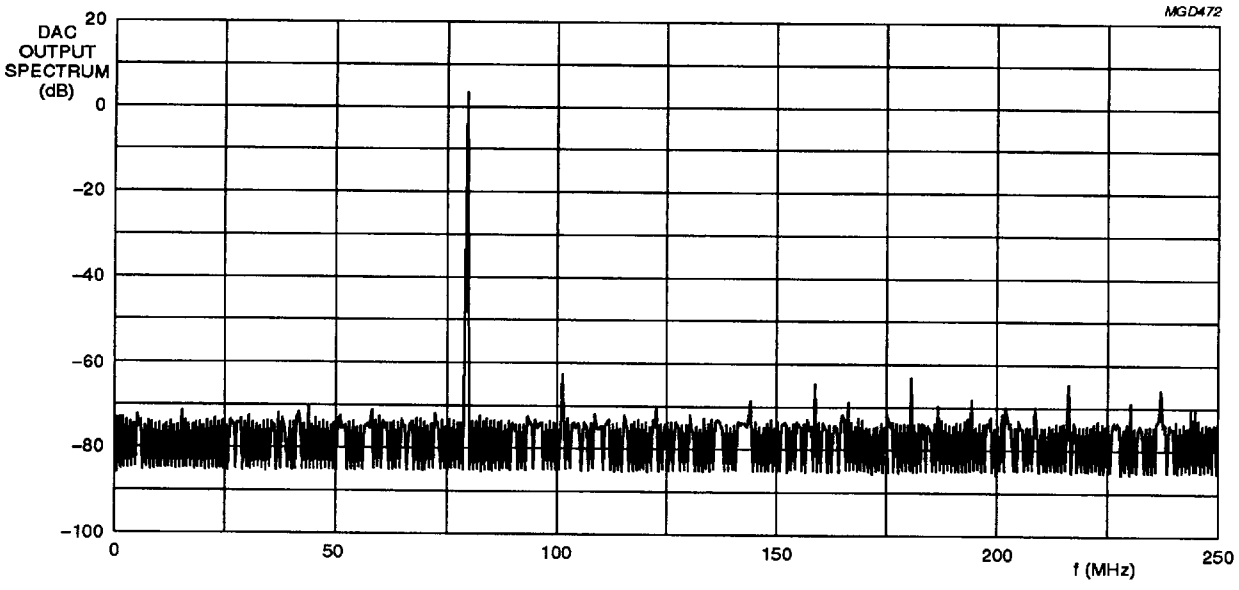


Fig.6 Typical output spectrum; f_{clk} = 500 MHz; f_{OUT} = 80 MHz.

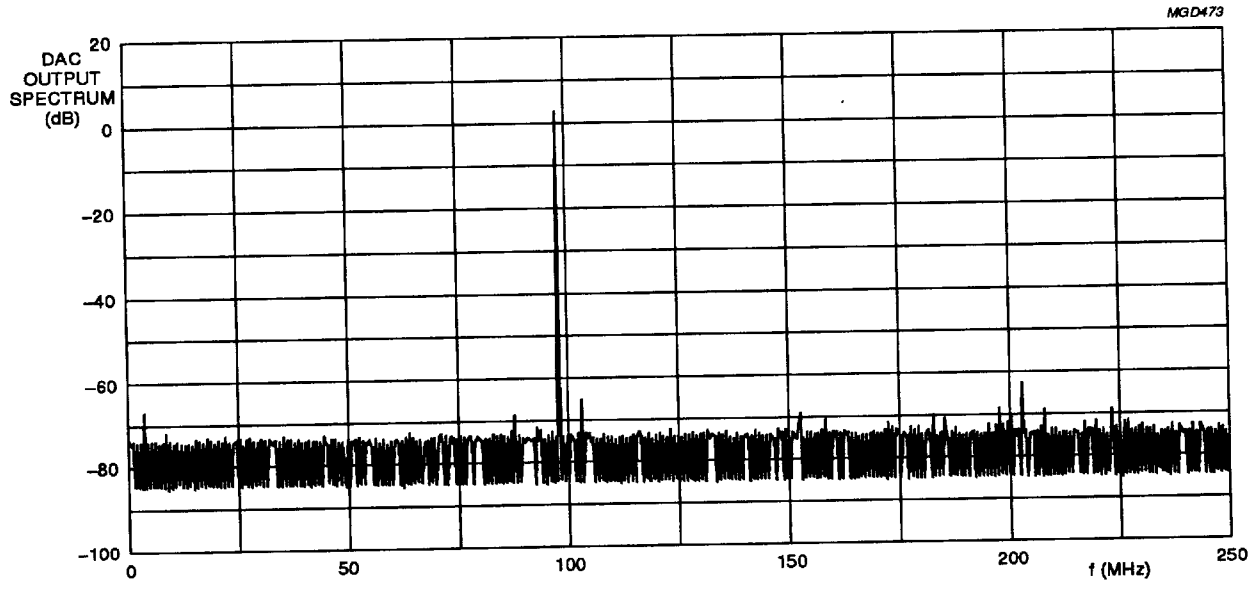
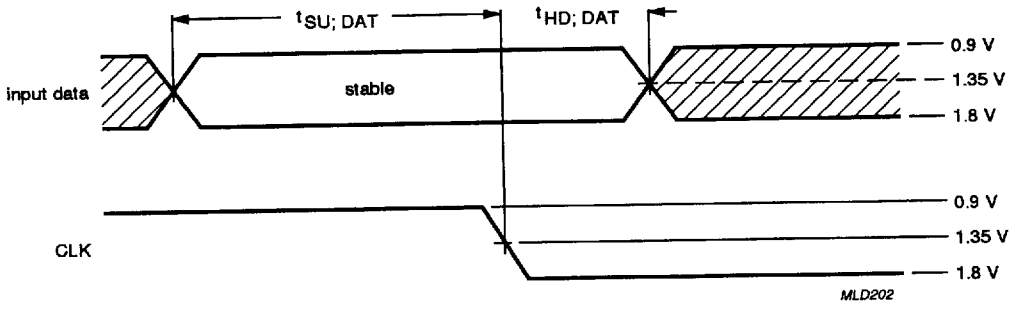


Fig.7 Typical output spectrum; f_{clk} = 500 MHz; f_{OUT} = 100 MHz.



The shaded areas indicate when the input data may change and be correctly registered. Data input update must be completed within tbf ns after the falling edge of the clock ($t_{SU;DAT}$ is negative; tbf ns). Data must be held at least tbf ns after the falling edge ($t_{HD,DAT}$ = tbf ns).

Fig.8 Data set-up and hold times.

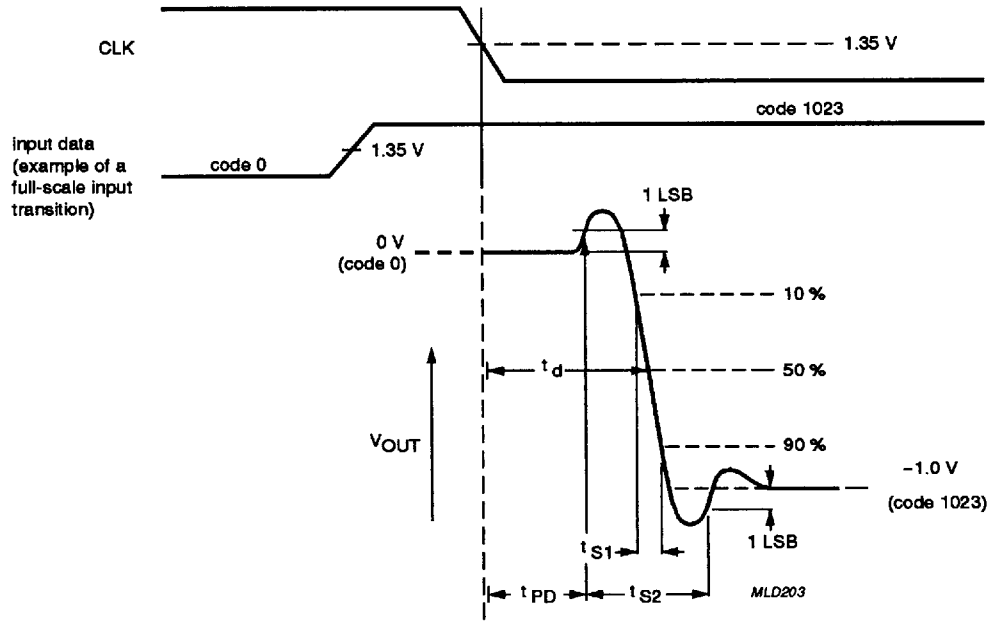
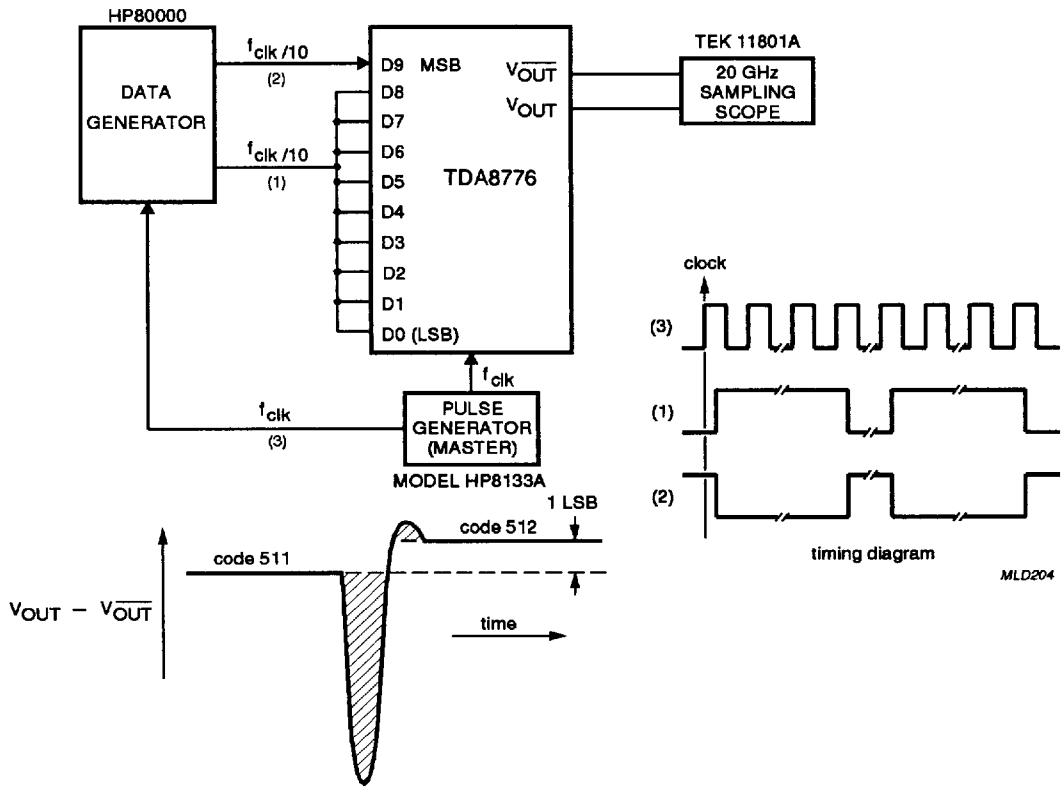


Fig.9 Switching characteristics.



The value of the glitch energy is the sum of the shaded areas measured in pV.s.

Fig.10 Glitch energy measurement.

INTERNAL PIN CONFIGURATIONS

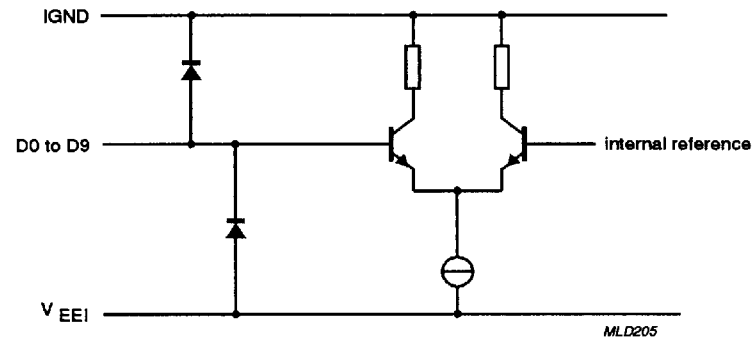


Fig.11 D9 to D0.

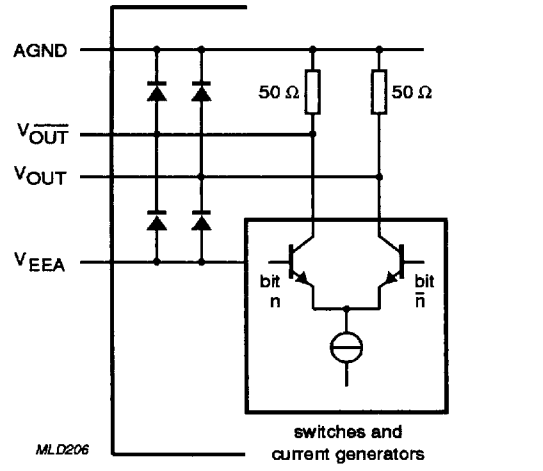


Fig.12 Analog outputs.

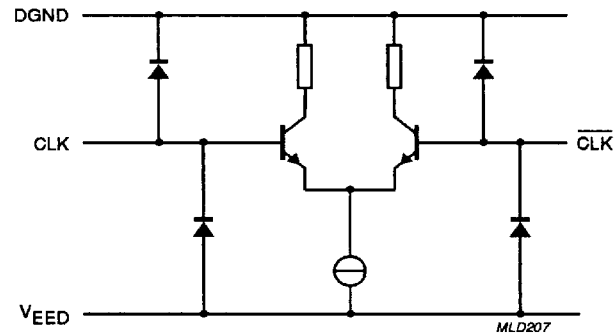
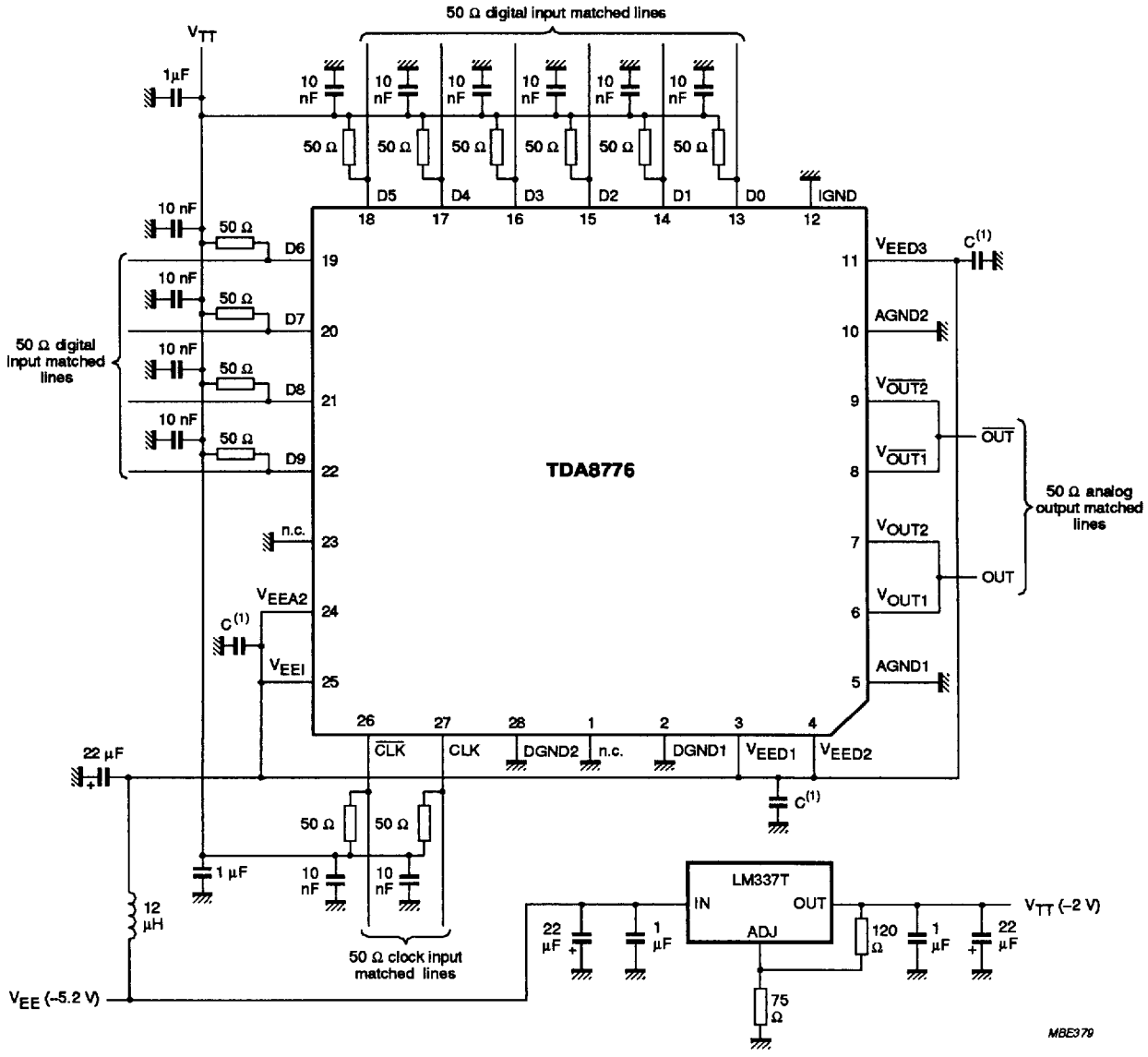


Fig.13 CLK and $\overline{CLK}$.

APPLICATION INFORMATION

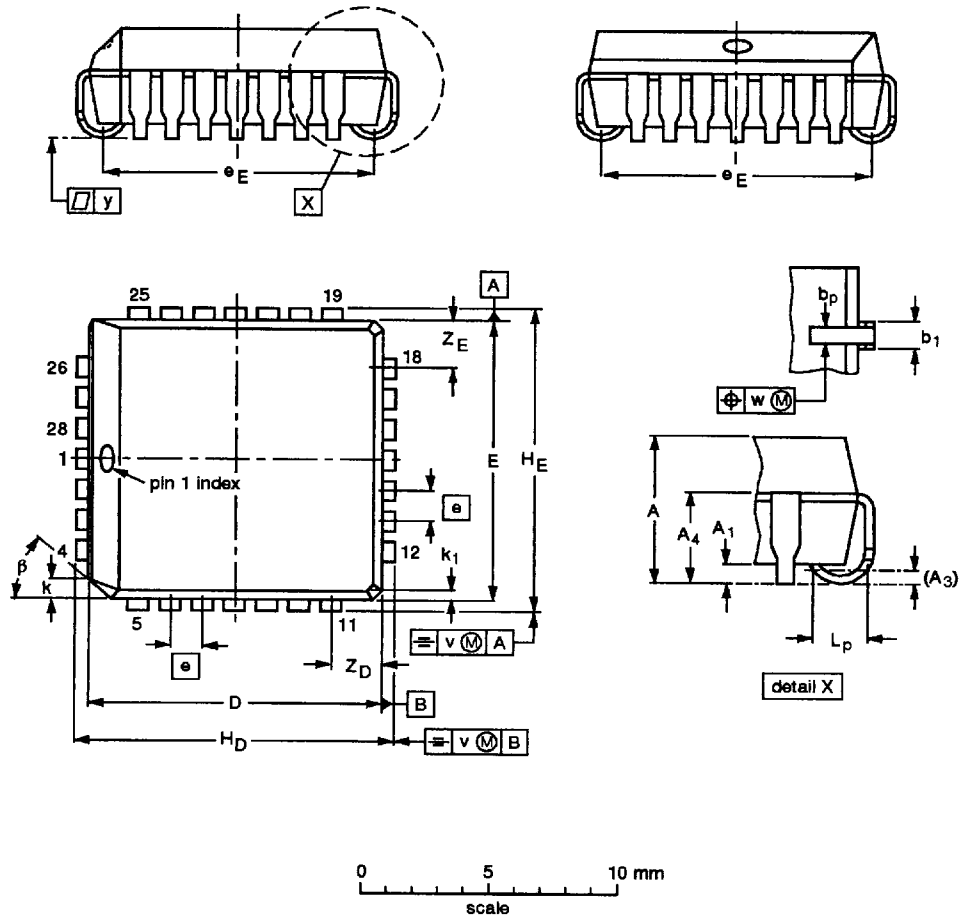


(1) C = 1 µF in parallel with 10 nF in parallel with 1 nF; all three mounted close to the supply pin of the DAC with 1 nF the nearest.

Fig.14 Application diagram.

PACKAGE OUTLINE

PLCC28: plastic leaded chip carrier; 28 leads **SOT261-2**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	$D^{(1)}$	$E^{(1)}$	e	e_D	e_E	H_D	H_E	k	k_1 max.	L_p	v	w	y	$Z_D^{(1)}$ max.	$Z_E^{(1)}$ max.	β
mm	4.57 4.19	0.51	0.25	3.05	0.53 0.33	0.81 0.66	11.58 11.43	11.58 11.43	1.27	10.92 9.91	10.92 9.91	12.57 12.32	12.57 12.32	1.22 1.07	0.51	1.44 1.02	0.18	0.18	0.10	2.16	2.16	45°
inches	0.180 0.165	0.020	0.01	0.12	0.021 0.013	0.032 0.026	0.456 0.450	0.456 0.450	0.05	0.430 0.390	0.430 0.390	0.495 0.485	0.495 0.485	0.048 0.042	0.020	0.057 0.040	0.007	0.007	0.004	0.085	0.085	

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT261-2						~~92-11-17~~ 95-02-25

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all PLCC packages.

The choice of heating method may be influenced by larger PLCC packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information, refer to the Drypack chapter in our *"Quality Reference Handbook"* (order code 9397 750 00192).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering techniques can be used for all PLCC packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.