SRAM MODULE

16K x 32 SRAM

FEATURES

- High speed: 10*, 15, 20, 25 and 35ns
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ functions
- Low profile
- All inputs and outputs are TTL compatible
- Industry standard pinout
- Upgradable with 64K x 32, 128K x 32 and 256K x 32 modules

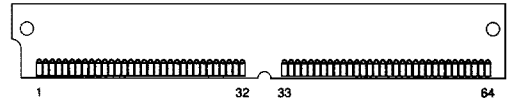
OPTIONS — MARKING

- Timing
  - 10ns access — -10*
  - 15ns access — -15
  - 20ns access — -20
  - 25ns access — -25
  - 35ns access — -35
- Packages
  - 64-pin SIMM — M
  - 64-pin ZIP — Z
- 2V data retention — L
- Part Number Example: MT8S1632M-10 L

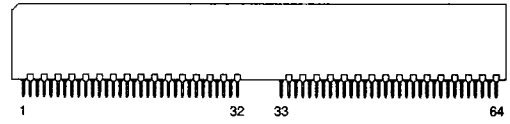
*Preliminary

PIN ASSIGNMENT (Top View)

64-Pin SIMM
(SG-1)



64-Pin ZIP
(SH-2)



PIN #	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
1	Vss	17	A2	33	$\overline{CE4}$	49	A4
2	PD0	18	A9	34	$\overline{CE3}$	50	A11
3	PD1	19	DQ13	35	NC	51	A5
4	DQ1	20	DQ5	36	NC	52	A12
5	DQ9	21	DQ14	37	$\overline{OE}$	53	Vcc
6	DQ2	22	DQ6	38	Vss	54	A13
7	DQ10	23	DQ15	39	DQ25	55	A6
8	DQ3	24	DQ7	40	DQ17	56	DQ21
9	DQ11	25	DQ16	41	DQ26	57	DQ29
10	DQ4	26	DQ8	42	DQ18	58	DQ22
11	DQ12	27	Vss	43	DQ27	59	DQ30
12	Vcc	28	$\overline{WE}$	44	DQ19	60	DQ23
13	A0	29	NC	45	DQ28	61	DQ31
14	A7	30	NC	46	DQ20	62	DQ24
15	A1	31	$\overline{CE2}$	47	A3	63	DQ32
16	A8	32	$\overline{CE1}$	48	A10	64	Vss

GENERAL DESCRIPTION

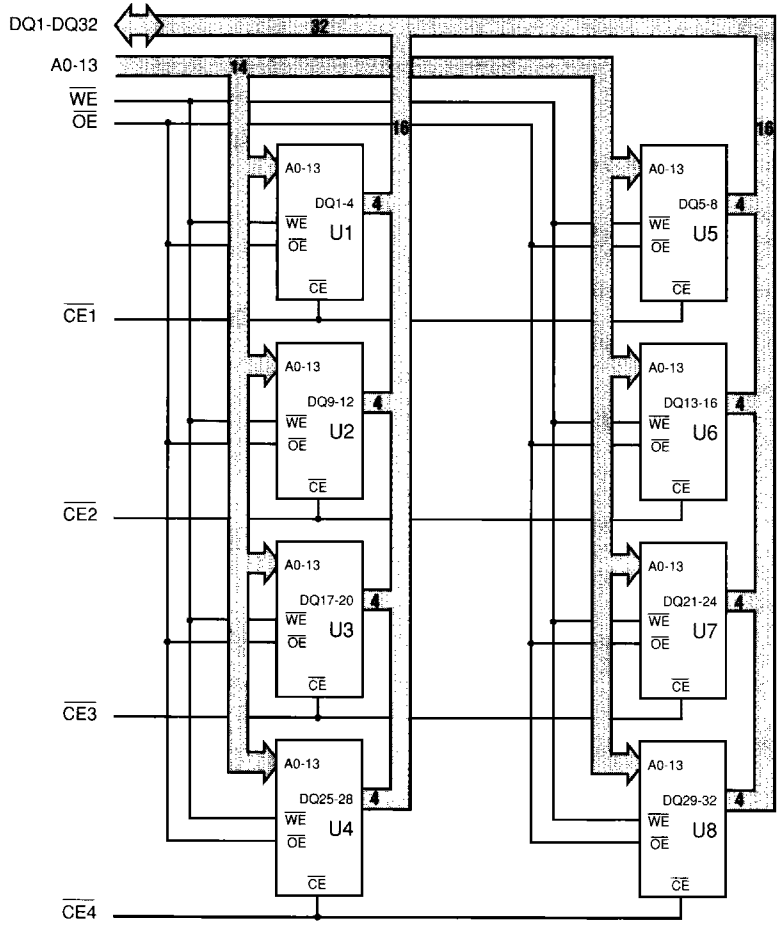
The MT8S1632 is a high-speed SRAM memory module containing 16,384 words organized in a x32-bit configuration. The module consists of eight 16K x 4 fast static RAMs mounted on a 64-pin, double-sided, FR4-printed circuit board.

Data is written into to the SRAM memory when write enable ($\overline{WE}$) and chip enable ($\overline{CE}$) inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ and output enable ($\overline{OE}$) are LOW. $\overline{CE}$ can set the output in High-Z for additional flexibility in system design, and memory expansion is accomplished by use of the $\overline{OE}$ and $\overline{CE}$ functions.

PD0 and PD1 identify the module's density, allowing interchangeable use of alternate-density, industry standard modules. Four chip enable inputs, ($\overline{CE1}$, $\overline{CE2}$, $\overline{CE3}$ and $\overline{CE4}$), are used to enable the module's 4 bytes independently.

The Micron SRAM family uses a high-speed, low-power CMOS design in a four-transistor memory cell featuring double-layer metal, double-layer polysilicon technology. All module components may be powered from a single +5V supply and all inputs and outputs are fully TTL compatible. The "L" option offers reduced-voltage operation for systems with low standby power requirements.

FUNCTIONAL BLOCK DIAGRAM



PRESENCE DETECT
PD0 = Vss
PD1 = No Connect

U1-U8 = MT5C6405DJ

TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
READ	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Storage Temperature ..... -55°C to +125°C
Power Dissipation 8W
Short Circuit Output Current 50mA
Voltage on any pin relative to V_{SS} ..... -1V to V_{CC} +1V

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; V_{CC} = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC}+1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-40	40	µA	
Output Leakage Current	Output(s) Disabled $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	4.5	5.5	V	1

				MAX						
DESCRIPTION	CONDITIONS	SYMBOL	TYP	-10*	-15	-20	-25	-35	UNITS	NOTES
Operating Current: TTL Input Levels	$\overline{CE} \le V_{IL}$; V_{CC} = MAX f = MAX = 1/ ^tRC Outputs Open	I_{CC}	520	1,280	960	880	800	720	mA	3, 13
Standby Current: TTL Input Levels	$\overline{CE} \ge V_{IH}$; V_{CC} = MAX f = MAX = 1/ ^tRC Outputs Open	I_{SB1}	160	440	320	280	240	200	mA	13
Power Supply Current: Standby	$\overline{CE} \ge V_{CC}$ -0.2V; V_{CC} = MAX $V_{IN} \le V_{SS}$ +0.2V or $V_{IN} \ge V_{CC}$ -0.2V; f = 0	I_{SB2}	3.2	24	24	24	40	24	mA	13

*Preliminary

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A13, $\overline{WE}$, $\overline{CE}$, $\overline{OE}$	T_A = 25°C; f = 1 MHz	C_I	70	pF	4
Input/Output Capacitance: DQ1-DQ32	V_{CC} = 5V	$C_{I/O}$	10	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION		-10*		-15		-20		-25		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle													
READ cycle time	tRC	10		15		20		25		35		ns	
Address access time	tAA		10		15		20		25		35	ns	
Chip Enable access time	tACE		8		12		15		20		30	ns	
Output hold from address change	tOH	3		3		3		3		3		ns	
Chip Enable to output in Low-Z	tLZCE†	2		3 2		5 2		5 2		5 2		ns	7, 14
Chip Enable to output in High-Z	tHZCE		5		7		8		8		8	ns	6, 7
Chip disable to power-up time	tPU	0		0		0		0		0		ns	
Chip Enable to power-down time	tPD		10		15		20		25		35	ns	
Output Enable access time	tAOE		4		6		7		8		15	ns	
Output disable to output in Low-Z	tLZOE	0		0		0		0		0		ns	
Output Enable to output in High-Z	tHZOE		4		6		7		8		8	ns	6
WRITE Cycle													
WRITE cycle time	tWC	10		15		20		25		35		ns	
Chip Enable to end of write	tCW	8		12		15		20		25		ns	
Address valid to end of write	tAW	8		12		15		20		25		ns	
Address setup time	tAS	0		0		0		0		0		ns	
Address hold from end of write	tAH	0		0		0		0		0		ns	
WRITE pulse width	tWP1	7		10		12		15		20		ns	
WRITE pulse width	tWP2	9		14		18		20		25		ns	
Data setup time	tDS	6		8		9		10		12		ns	
Data hold time	tDH	0		0		0		0		0		ns	
Write disable to output in Low-Z	tLZWE	2		2		2		2		2		ns	7
Write Enable to output in High-Z	tHZWE		5		6		8		8		8	ns	6, 7

*Preliminary

†The difference between the shaded and unshaded parameters is explained in note 14 on the following page.

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

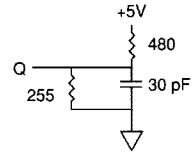


Fig. 1 OUTPUT LOAD EQUIVALENT

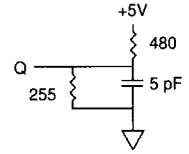


Fig. 2 OUTPUT LOAD EQUIVALENT

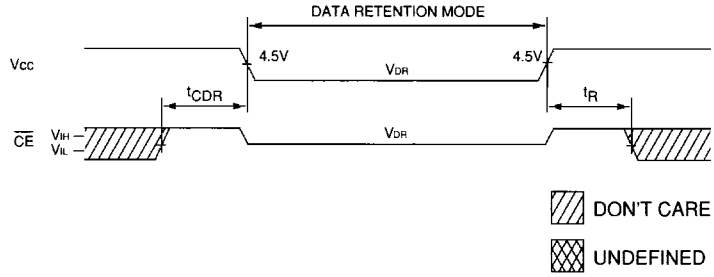
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < ^{t}RC/2.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZOE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE, and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^{t}RC=Read Cycle Time
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Typical values are measured at 5V, 25°C and 20ns cycle time.
14. New designs should use the ^{t}LZCE parameters shown unshaded. The shaded ^{t}LZCE parameters represent screened parts, which are available upon request until January 1, 1994.

DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

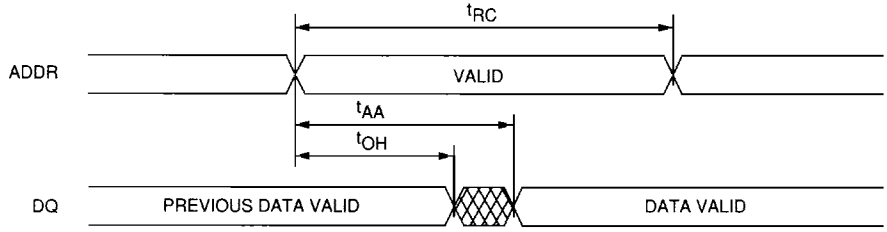
DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			VDR	2			V	
Data Retention Current	$\overline{CE}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	ICCDR		760	2,000	µA	
		Vcc = 3V			1,000	3,200	µA	
Chip Deselect to Data Retention Time			^{t}CDR	0			ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4,11

LOW Vcc DATA-RETENTION WAVEFORM

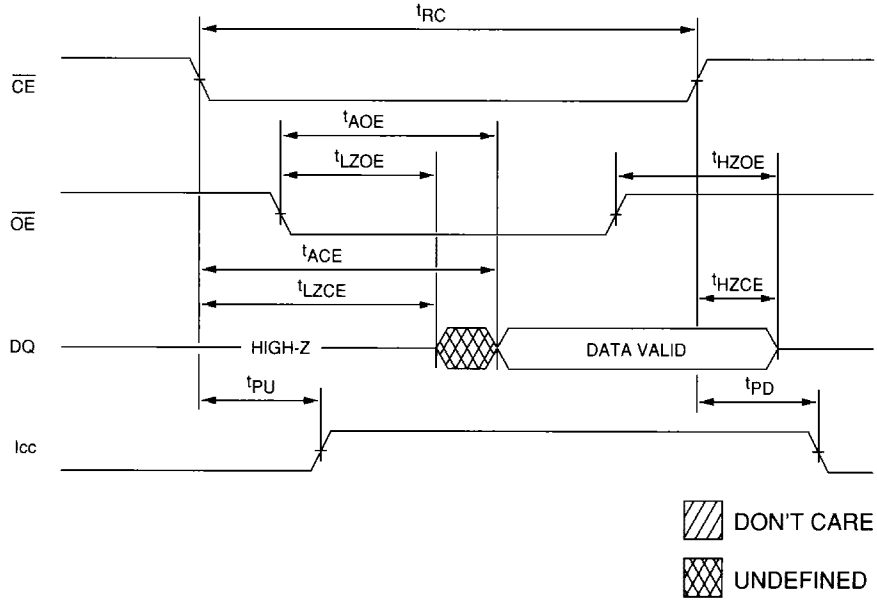


SRAM MODULE

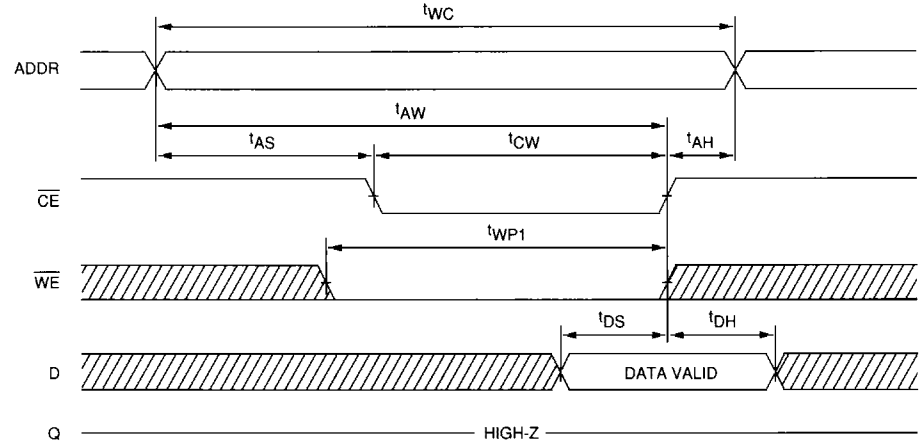
READ CYCLE NO. 1 [8, 9]



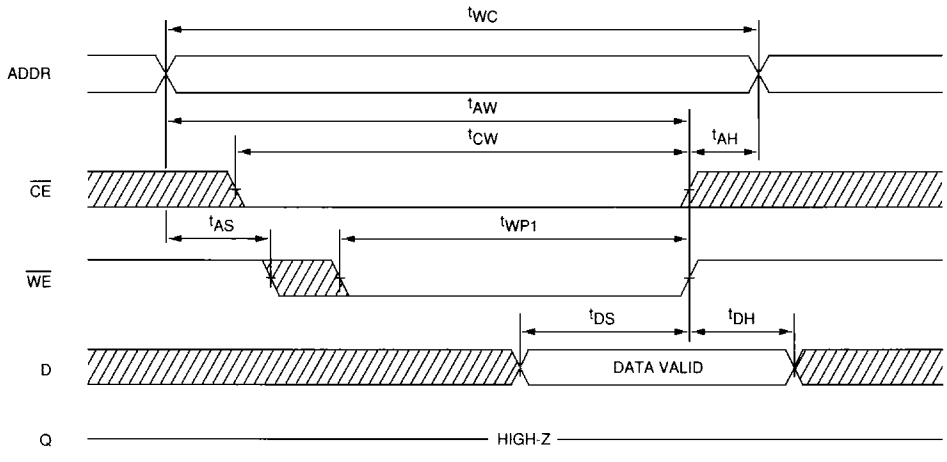
READ CYCLE NO. 2 [7, 8, 10]



WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)



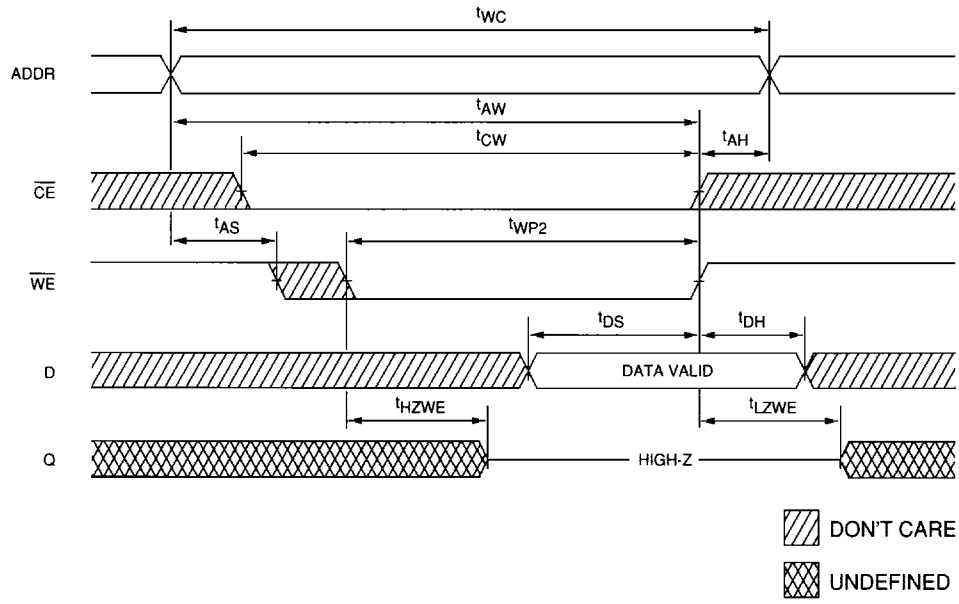
WRITE CYCLE NO. 2 [7, 12]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is inactive (HIGH).

SRAM MODULE

WRITE CYCLE NO. 3 [7, 12]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is active (LOW).