www.DataSheet4U.com

M74LS259P

8-BIT ADDRESSABLE LATCH

DESCRIPTION

The M74LS259P is a semiconductor integrated circuit containing 8 latch circuits and a demultiplexer which designates the latches with a 3-bit binary code.

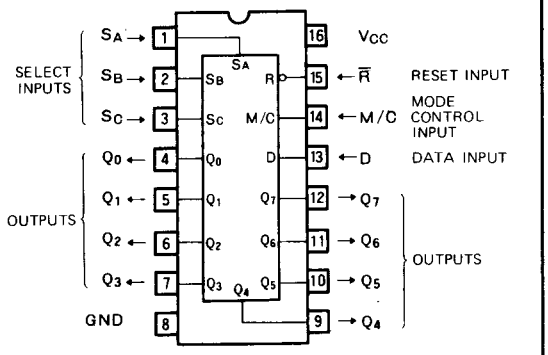
FEATURES

- Easy bit expansion
- Usable as 3-bit binary/octal decoder/demultiplexer
- Direct reset input provided
- Wide operating temperature range (T_a = −20 ~ +75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

FUNCTIONAL DESCRIPTION

This device is composed of a 3-bit binary/octal demultiplexer and 8 latch circuits. The following operational modes can be selected by combining the mode control input M/C with the reset input $\overline{R}$

(1) 3-bit binary/octal decoder/demultiplexer	M/C: Low; $\overline{R}$: Low
(2) Addressable latch	M/C: Low; $\overline{R}$: High
(3) Data input inhibit	M/C: High $\overline{R}$: High
(4) Reset	M/C: High; $\overline{R}$: Low

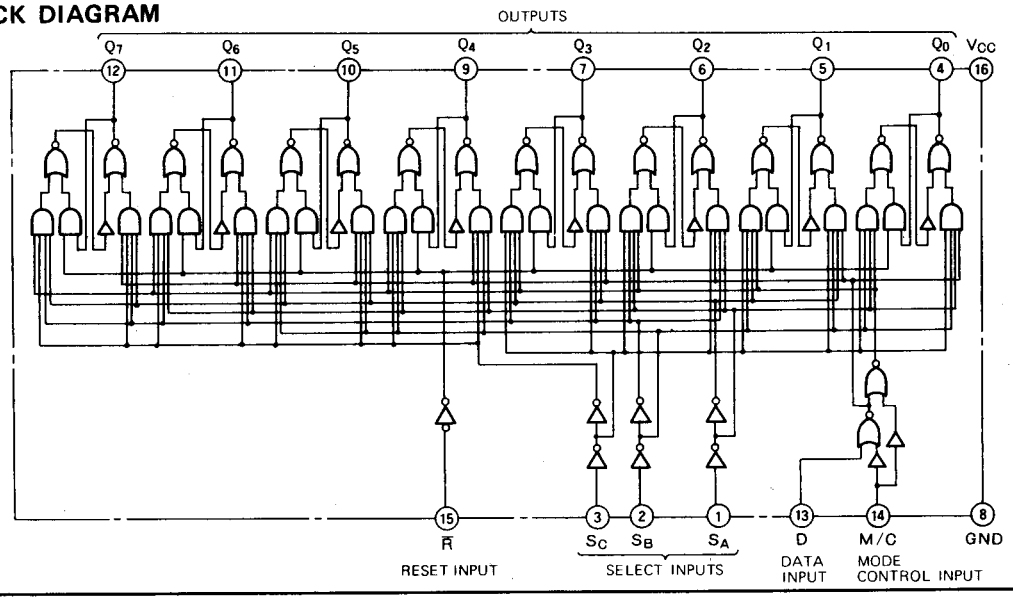
When this device is used as a 3-bit binary/octal decoder/demultiplexer and the select inputs S_A ~ S_C are designated by a 3-bit binary number, the same signal as the data input D appears in one of the outputs Q_0 ~ Q_7 corresponding to that number and all the other outputs are set low. There is no latch operation in this mode.

When used as an addressable latch and inptus S_A ~ S_C are designated as above, the corresponding latch is selected and the same signal as D appears in the output. When M/C changes from low to high (data inhibit mode), the information from the data input D immediately before the change is latched. When M/C is low, the signal appearing in Q is also changed if the signal D is changed.

In the data input inhibit mode Q_0 ~ Q_7 do not change

www.DataSheet4U.com

BLOCK DIAGRAM



www.DataSheet4U.com

www.DataSheet4U.com

even if D is changed and the status before M/C is set high is held.

With direct resetting, all the outputs are reset low irrespective of the status of D and $S_A \sim S_C$.

FUNCTION TABLE (Note 1)

Operational mode	$\overline{R}$	M/C	D	S_A	S_B	S_C	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7
Reset	L	H	X	X	X	X	L	L	L	L	L	L	L	L
3-bit binary/octal decoder/demultiplexer	L	L	L	L	L	L	L	L	L	L	L	L	L	L
	L	L	H	L	L	L	H	L	L	L	L	L	L	L
	L	L	L	H	L	L	L	L	L	L	L	L	L	L
	L	L	H	H	L	L	L	H	L	L	L	L	L	L
	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
	L	L	L	H	H	H	L	L	L	L	L	L	L	L
	L	L	H	H	H	H	L	L	L	L	L	L	L	H
Data input inhibit	H	H	X	X	X	X	Q_0^0	Q_1^0	Q_2^0	Q_3^0	Q_4^0	Q_5^0	Q_6^0	Q_7^0
Addressable latch	H	L	L	L	L	L	L	Q_1^0	Q_2^0	Q_3^0	Q_4^0	Q_5^0	Q_6^0	Q_7^0
	H	L	H	L	L	L	H	Q_1^0	Q_2^0	Q_3^0	Q_4^0	Q_5^0	Q_6^0	Q_7^0
	H	L	L	H	L	L	Q_0^0	L	Q_2^0	Q_3^0	Q_4^0	Q_5^0	Q_6^0	Q_7^0
	H	L	H	H	L	L	Q_0^0	H	Q_2^0	Q_3^0	Q_4^0	Q_5^0	Q_6^0	Q_7^0
	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
	H	L	L	H	H	H	Q_0^0	Q_1^0	Q_2^0	Q_3^0	Q_4^0	Q_5^0	Q_6^0	L
	H	L	H	H	H	H	Q_0^0	Q_1^0	Q_2^0	Q_3^0	Q_4^0	Q_5^0	Q_6^0	H

www.DataSheet4U.com

Note 1 X : Irrelevant

Q^0 : Level of Q before the indicated steady-state input conditions were established.

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	High-level state	−0.5 ~ V_{CC}	V
Topr	Operating free-air ambient temperature range		−20 ~ +75	°C
Tstg	Storage temperature range		−65 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		−400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

www.DataSheet4U.com

www.DataSheet4U.com

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ *	Max	
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
V_{IC}	Input clamp voltage	$V_{CC}=4.75V$, $I_{IC}=-18mA$			1.5	V
V_{OH}	High-level output voltage	$V_{CC}=4.75V$, $V_I=0.8V$, $V_I=2V$, $I_{OH}=-400\mu A$	2.7	3.4		V
V_{OL}	Low-level output voltage	$V_{CC}=4.75V$, $V_I=0.8V$, $V_I=2V$, $I_{OL}=4mA$		0.25	0.4	V
		$V_{CC}=4.75V$, $V_I=0.8V$, $V_I=2V$, $I_{OL}=8mA$		0.35	0.5	V
I_{IH}	High-level input current	$V_{CC}=5.25V$, $V_I=2.7V$			20	μA
		$V_{CC}=5.25V$, $V_I=10V$			0.1	mA
I_{IL}	Low-level input current	$V_{CC}=5.25V$, $V_I=0.4V$			−0.4	mA
I_{OS}	Short-circuit output current (Note 2)	$V_{CC}=5.25V$, $V_O=0V$	−20		−100	mA
I_{CC}	Supply current	$V_{CC}=5.25V$ (Note 3)		22	36	mA

* : All typical values are at $V_{CC}=5V$, $Ta=25°C$

Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with all inputs at 0V.

SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $Ta=25°C$, unless otherwise noted)

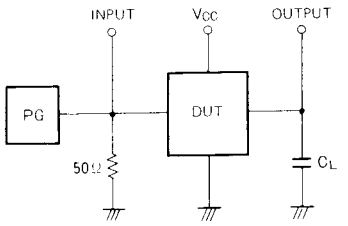
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PHL}	High-to-low-level output propagation time, from input $\overline{R}$ to outputs $Q_0 \sim Q_7$	$C_L=15pF$		9	27	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input D to outputs $Q_0 \sim Q_7$			15	32	ns
t_{PHL}				12	21	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from inputs S_A, S_B, S_C to outputs $Q_0 \sim Q_7$			15	38	ns
t_{PHL}				12	29	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time from input M/C to outputs $Q_0 \sim Q_7$			14	35	ns
t_{PHL}				13	24	ns

www.DataSheet4U.com

TIMING REQUIREMENTS ($V_{CC}=5V$, $Ta=25°C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{su(DH)}$	Setup time D high to M/C		15	10		ns
$t_{h(DH)}$	Hold time D high to M/C		5	−5		ns
$t_{su(DL)}$	Setup time D low to M/C		15	8		ns
$t_{h(DL)}$	Hold time D low to M/C		5	−7		ns
$t_{su(S)}$	Setup time S_A, S_B to M/C		15	7		ns
$t_{h(S)}$	Hold time S_A, S_B, to M/C		5	−5		ns
$t_{w(M/C)}$	M/C input pulse width		15	8		ns
$t_{w(\overline{R})}$	$\overline{R}$ input pulse width		15	7		ns

Note 4: Measurement circuit



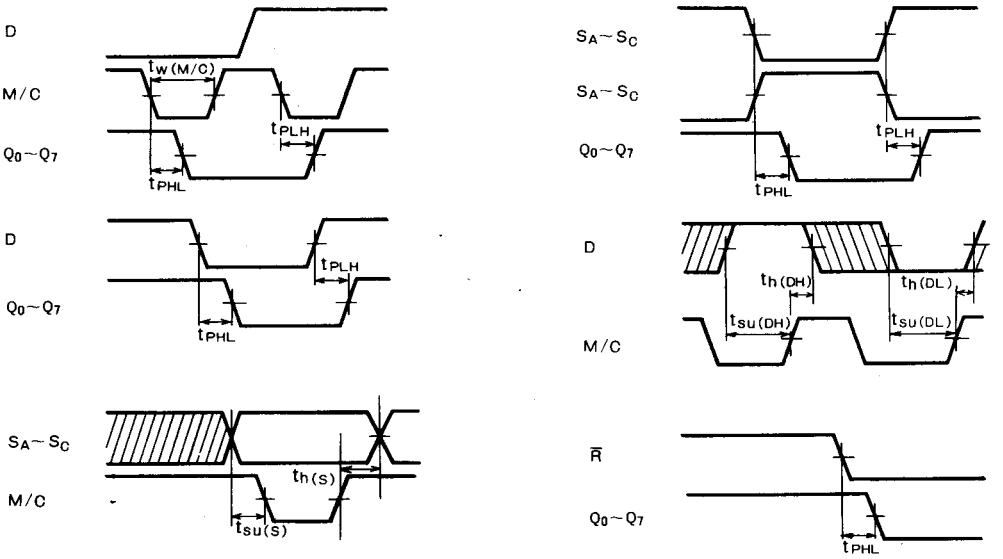
(1) The pulse generator (PG) has the following characteristics:
PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns,
$V_P = 3V_{P-P}$, $Z_O = 50\Omega$.

(2) C_L includes probe and jig capacitance.

www.DataSheet4U.com

www.DataSheet4U.com

TIMING DIAGRAM (Reference level = 1.3V)

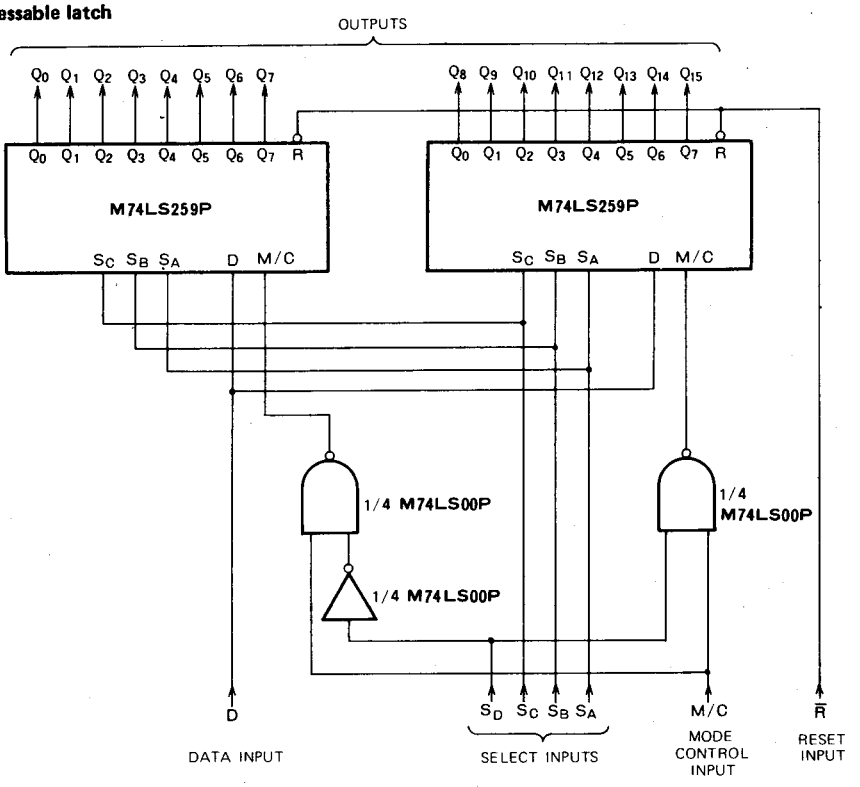


Note 5: The shaded areas indicate when the input is permitted to change for predictable output performance.

www.DataSheet4U.com

APPLICATION EXAMPLE

16-bit addressable latch

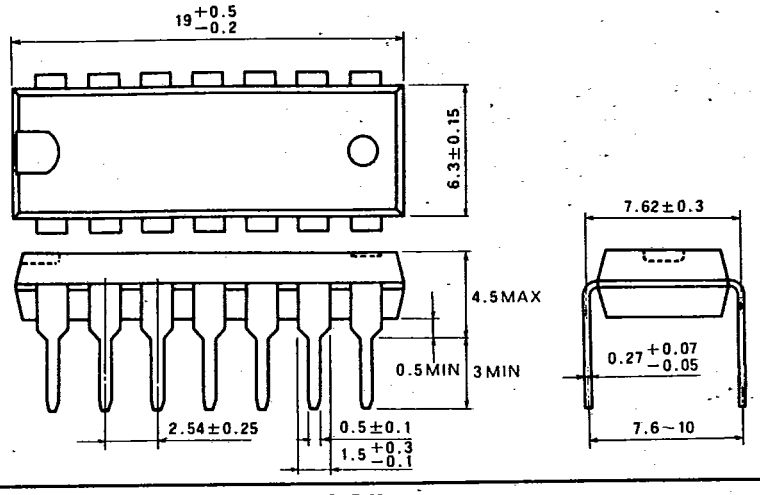


www.DataSheet4U.com

www.DataSheet4U.com

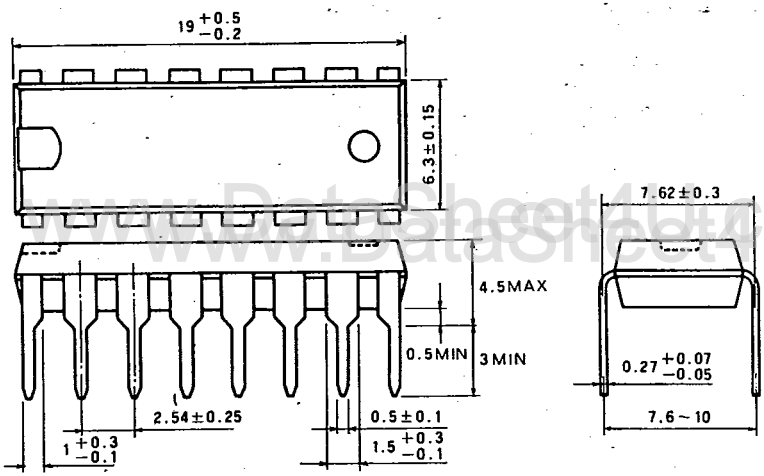
TYPE 14P4 14-PIN MOLDED PLASTIC DIL

Dimension in mm



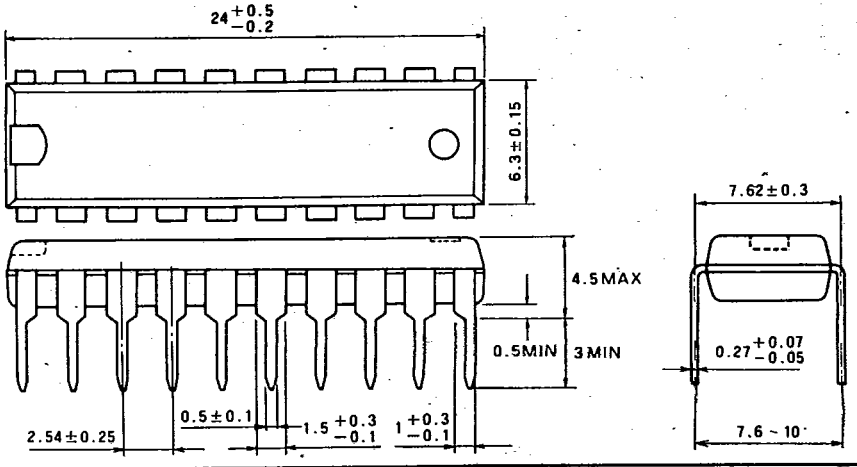
TYPE 16P4 16-PIN MOLDED PLASTIC DIL

Dimension in mm



TYPE 20P4 20-PIN MOLDED PLASTIC DIL

Dimension in mm



www.DataSheet4U.com