

CMOS SRAM

64Kx8 bit Low Power and Low Voltage CMOS Static RAM

FEATURES

- Process Technology : 0.6 μ m CMOS
- Organization : 64Kx8
- Power Supply Voltage
KM68V512A family : 3.3V $\pm$ 0.3V
KM68U512A family : 3.0V $\pm$ 0.3V
- Low Data Retention Voltage : 2V(Min)
- Three state output and TTL Compatible
- Package Type : 32-SOP-525, 32-TSOP1-0820F,
32-TSOP1-0813 4F

GENERAL DESCRIPTION

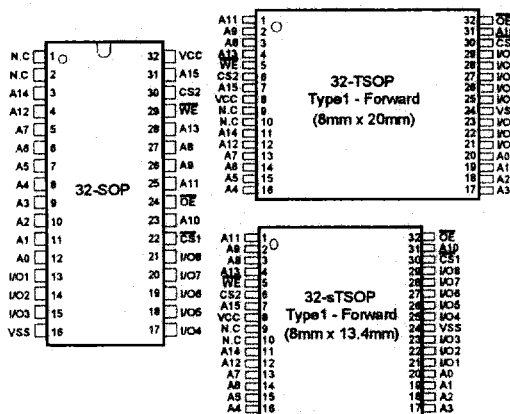
The KM68V512A and KM68U512A families are fabricated by SAMSUNG's advanced CMOS process technology. The families support various operating temperature ranges and have various package types for user flexibility of system design. The family also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed(ns)	Power Dissipation		PKG Type
				Standby (I _{ab1} , Max)	Operating (I _{cc2} , Max)	
KM68V512AL-L	Commercial(0~70°C)	3.0 ~ 3.6V	70 ¹⁾ /85/100	10μA	40mA	32-SOP 32-TSOP(I) F 32-sTSOP(I) F
KM68U512AL-L		2.7 ~ 3.3V	85 ¹⁾ /100	10μA		
KM68V512ALE-L	Extended(-25~85°C)	3.0 ~ 3.6V	70 ¹⁾ /85/100	20μA		
KM68U512ALE-L		2.7 ~ 3.3V	85 ¹⁾ /100	15μA		
KM68V512ALI-L	Industrial (-40~85°C)	3.0 ~ 3.6V	70 ¹⁾ /85/100	20μA		
KM68U512ALI-L		2.7 ~ 3.3V	85 ¹⁾ /100	15μA		

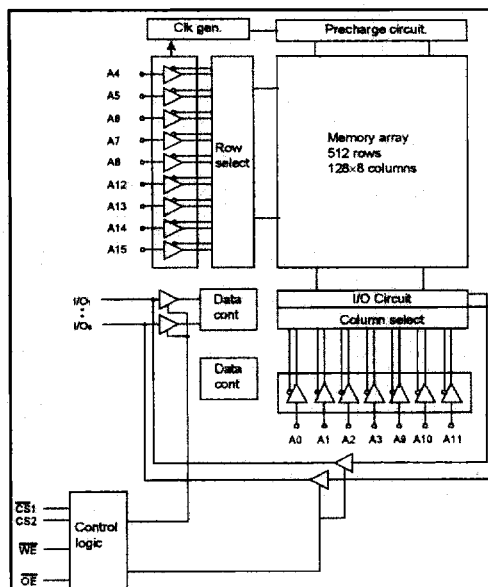
1. The parameter is measured with 30pF test load.

PIN DESCRIPTION



Name	Function
A0-A15	Address Inputs
WE	Write Enable Input
CS1, CS2	Chip Select Inputs
OE	Output Enable Input
I/O1-I/O8	Data Inputs/Outputs
Vcc	Power
Vss	Ground
N.C	No Connection

FUNCTIONAL BLOCK DIAGRAM



SAMSUNG ELECTRONICS CO., LTD. reserves the right to change products and specifications without notice.

PRODUCT LIST

Commercial Temp Product (0-70°C)		Extended Temp Products (-25-85°C)		Industrial Temp Products (-40-85°C)	
Part Name	Function	Part Name	Function	Part Name	Function
KM68V512ALG-7L	32-SOP, 70ns, 3.3V, LL	KM68V512ALGE-7L	32-SOP, 70ns, 3.3V, LL	KM68V512ALGI-7L	32-SOP, 70ns, 3.3V, LL
KM68V512ALG-8L	32-SOP, 85ns, 3.3V, LL	KM68V512ALGE-8L	32-SOP, 85ns, 3.3V, LL	KM68V512ALGI-8L	32-SOP, 85ns, 3.3V, LL
KM68V512ALG-10L	32-SOP, 100ns, 3.3V, LL	KM68V512ALGE-10L	32-SOP, 100ns, 3.3V, LL	KM68V512ALGI-10L	32-SOP, 100ns, 3.3V, LL
KM68V512ALT-7L	32-TSOP F, 70ns, 3.3V, LL	KM68V512ALTE-7L	32-TSOP F, 70ns, 3.3V, LL	KM68V512ALTI-7L	32-TSOP F, 70ns, 3.3V, LL
KM68V512ALT-8L	32-TSOP F, 85ns, 3.3V, LL	KM68V512ALTE-8L	32-TSOP F, 85ns, 3.3V, LL	KM68V512ALTI-8L	32-TSOP F, 85ns, 3.3V, LL
KM68V512ALT-10L	32-TSOP F, 100ns, 3.3V, LL	KM68V512ALTE-10L	32-TSOP F, 100ns, 3.3V, LL	KM68V512ALTI-10L	32-TSOP F, 100ns, 3.3V, LL
KM68V512ALTG-7L	32-sTSOP F, 70ns, 3.3V, LL	KM68V512ALTGE-7L	32-sTSOP F, 70ns, 3.3V, LL	KM68V512ALTGI-7L	32-sTSOP F, 70ns, 3.3V, LL
KM68V512ALTG-8L	32-sTSOP F, 85ns, 3.3V, LL	KM68V512ALTGE-8L	32-sTSOP F, 85ns, 3.3V, LL	KM68V512ALTGI-8L	32-sTSOP F, 85ns, 3.3V, LL
KM68V512ALTG-10L	32-sTSOP F, 100ns, 3.3V, LL	KM68V512ALTGE-10L	32-sTSOP F, 100ns, 3.3V, LL	KM68V512ALTGI-10L	32-sTSOP F, 100ns, 3.3V, LL
KM68U512ALG-8L	32-SOP, 85ns, 3.0V, LL	KM68U512ALGE-8L	32-SOP, 85ns, 3.0V, LL	KM68U512ALGI-8L	32-SOP, 85ns, 3.0V, LL
KM68U512ALG-10L	32-SOP, 100ns, 3.0V, LL	KM68U512ALGE-10L	32-SOP, 100ns, 3.0V, LL	KM68U512ALGI-10L	32-SOP, 100ns, 3.0V, LL
KM68U512ALT-8L	32-TSOP F, 85ns, 3.0V, LL	KM68U512ALTE-8L	32-TSOP F, 85ns, 3.0V, LL	KM68U512ALTI-8L	32-TSOP F, 85ns, 3.0V, LL
KM68U512ALT-10L	32-TSOP F, 100ns, 3.0V, LL	KM68U512ALTE-10L	32-TSOP F, 100ns, 3.0V, LL	KM68U512ALTI-10L	32-TSOP F, 100ns, 3.0V, LL
KM68U512ALTG-8L	32-sTSOP F, 85ns, 3.0V, LL	KM68U512ALTGE-8L	32-sTSOP F, 85ns, 3.0V, LL	KM68U512ALTGI-8L	32-sTSOP F, 85ns, 3.0V, LL
KM68U512ALTG-10L	32-sTSOP F, 100ns, 3.0V, LL	KM68U512ALTGE-10L	32-sTSOP F, 100ns, 3.0V, LL	KM68U512ALTGI-10L	32-sTSOP F, 100ns, 3.0V, LL

FUNCTIONAL DESCRIPTION

CS ₁	CS ₂	OE	WE	I/O	Mode	Power
H	X ¹⁾	X ¹⁾	X ¹⁾	High-Z	Deselected	Standby
X ¹⁾	L	X ¹⁾	X ¹⁾	High-Z	Deselected	Standby
L	H	H	H	High-Z	Output Disabled	Active
L	H	L	H	Dout	Read	Active
L	H	X ¹⁾	L	Din	Write	Active

1. X means don't care(Must be low or high state.)

ABSOLUTE MAXIMUM RATINGS¹⁾

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to V _{SS}	V _{IN} , V _{OUT}	-0.5 to V _{CC} +0.5	V	-
Voltage on V _{CC} supply relative to	V _{CC}	-0.3 to 4.6	V	-
Power Dissipation	P _D	1.0	W	-
Storage temperature	T _{STG}	-65 to 150	°C	-
Operating Temperature	T _A	0 to 70	°C	KM68V512AL-L, KM68U512AL-L
		-25 to 85	°C	KM68V512ALE-L, KM68U512ALE-L
		-40 to 85	°C	KM68V512ALI-L, KM68U512ALI-L
Soldering temperature and time	T _{SOLDER}	260°C, 10sec (Lead Only)	-	-

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS¹⁾

Item	Symbol	Product	Min	Typ	Max	Unit
Supply voltage	V _{CC}	KM68V512A Family	3.0	3.3	3.6	V
		KM68U512A Family	2.7	3.0	3.3	V
Ground	V _{SS}	All Family	0	0	0	V
Input high voltage	V _{IH}	KM68V512A, KM68U512A Family	2.2	-	V _{CC} +0.3V ²⁾	V
Input low voltage	V _{IL}	KM68V512A, KM68U512A Family	-0.3 ³⁾	-	0.4	V

Note:

- Commercial Product : TA=0 to 70°C, otherwise specified
Extended Product : TA=-25 to 85°C, otherwise specified
Industrial Product : TA=-40 to 85°C, otherwise specified
- Overshoot : V_{CC}+3.0V in case of pulse width ≤ 30ns
- Undershoot : -3.0V in case of pulse width ≤ 30ns
- Overshoot and undershoot are sampled, not 100% tested

CAPACITANCE¹⁾ (f=1MHz, TA=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C _{IN}	V _{IN} =0V	-	6	pF
Input/Output capacitance	C _{IO}	V _{IO} =0V	-	8	pF

1. Capacitance is sampled, not 100% tested

DC AND OPERATING CHARACTERISTICS

Item	Symbol	Test Conditions	Min	Typ	Max	Unit
Input leakage current	I _{LI}	V _{IN} =V _{SS} to V _{CC}	-1	-	1	μA
Output leakage current	I _{LO}	$\overline{CS}_1=V_{IH}$ or $CS_2=V_{IL}$ or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$, V _{IO} =V _{SS} to V _{CC}	-1	-	1	μA
Operating power supply current	I _{CC}	I _{IO} =0mA, $\overline{CS}_1=V_{IL}$, CS ₂ =V _{IH} , V _{IN} =V _{IH} or V _{IL}	-	-	5	mA
Average operating current	I _{CC1}	Cycle time=1μs, 100% duty, I _{IO} =0mA, $\overline{CS}_1 \leq 0.2V$, CS ₂ ≥ V _{CC} -0.2V, V _{IN} ≤ 0.2V or V _{IN} ≥ V _{CC} -0.2V	-	-	5	mA
	I _{CC2}	Cycle time=Min, 100% duty, I _{IO} =0mA, $\overline{CS}_1=V_{IL}$, CS ₂ =V _{IH} , V _{IN} =V _{IL} or V _{IH}	-	-	40	mA
Output low voltage	V _{OL}	I _{OL} =2.1mA	-	-	0.4	V
Output high voltage	V _{OH}	I _{OH} =-1.0mA	2.4	-	-	V
Standby Current(TTL)	I _{SB}	$\overline{CS}_1=V_{IH}$, CS ₂ =V _{IL} , Other inputs=V _{IL} or V _{IH}	-	-	0.3	mA
Standby Current(CMOS)	I _{SB1}	KM68V512AL-L	-	-	10	μA
		KM68V512ALE-L	-	-	20	μA
		KM68V512ALI-L	-	-	-	-
		KM68U512AL-L	-	-	10	μA
		KM68U512ALE-L	-	-	15	μA

AC OPERATING CONDITIONS

TEST CONDITIONS(Test Load and Input/Output Reference)

Input pulse level : 0.4 to 2.2V

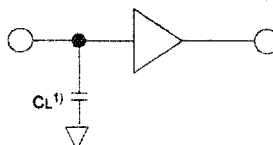
Input rising and falling time : 5ns

Input and output reference voltage : 1.5V

Output load(see right) : $C_L=100\text{pF}+1\text{TTL}$

¹⁾ $C_L=30\text{pF}+1\text{TTL}$

1. KM68V512AL-7L Family, KM68U512AL-8L Family



1. Including scope and jig capacitance

AC CHARACTERISTICS

(KM68V512B Family : $V_{CC}=3.0\sim 3.6\text{V}$, KM68U512B Family : $V_{CC}=2.7\sim 3.3\text{V}$,

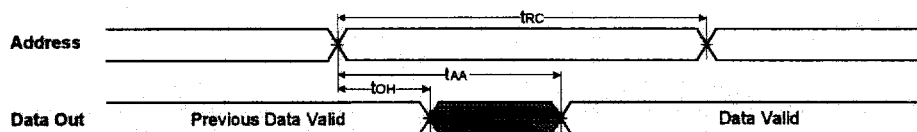
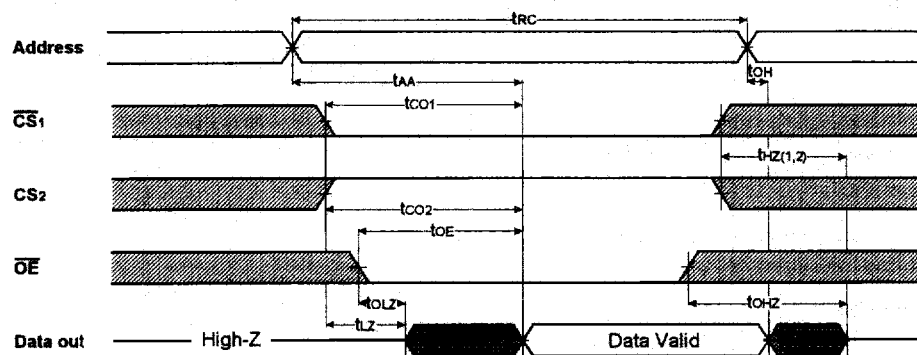
Commercial product : $T_A=0$ to 70°C , Extended product: $T_A=-25$ to 85°C , Industrial product: $T_A=-40$ to 85°C)

Parameter List		Symbol	Speed Bins						Units
			70ns		85ns		100ns		
			Min	Max	Min	Max	Min	Max	
Read	Read cycle time	t _{RC}	70	-	85	-	100	-	ns
	Address access time	t _{AA}	-	70	-	85	-	100	ns
	Chip select to output	t _{CO}	-	70	-	85	-	100	ns
	Output enable to valid output	t _{OE}	-	35	-	45	-	50	ns
	Chip select to low-Z output	t _{LZ}	10	-	10	-	10	-	ns
	Output enable to low-Z output	t _{OLZ}	5	-	5	-	5	-	ns
	Chip disable to high-Z output	t _{HZ}	0	25	0	30	0	30	ns
	Output disable to high-Z output	t _{OHZ}	0	25	0	20	0	20	ns
	Output hold from address change	t _{OH}	10	-	10	-	15	-	ns
Write	Write cycle time	t _{WC}	70	-	85	-	100	-	ns
	Chip select to end of write	t _{CW}	60	-	70	-	80	-	ns
	Address set-up time	t _{AS}	0	-	0	-	0	-	ns
	Address valid to end of write	t _{AW}	60	-	70	-	80	-	ns
	Write pulse width	t _{WP}	55	-	60	-	70	-	ns
	Write recovery time	t _{WR}	0	-	0	-	0	-	ns
	Write to output high-Z	t _{WHZ}	0	25	0	25	0	30	ns
	Data to write time overlap	t _{DW}	30	-	35	-	40	-	ns
	Data hold from write time	t _{DH}	0	-	0	-	0	-	ns
	End write to output low-Z	t _{OW}	5	-	5	-	5	-	ns

DATA RETENTION CHARACTERISTICS

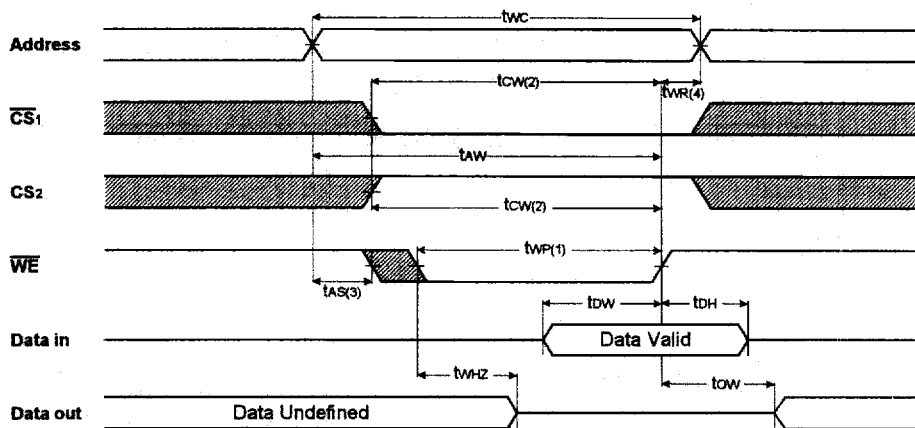
Item	Symbol	Test Condition	Min	Typ	Max	Unit
V _{CC} for data retention	V _{DR}	$\overline{CS}_1^{1)} \geq V_{CC}-0.2\text{V}$	2.0	-	3.6	V
Data retention current	I _{DR}	V _{CC} =3.0V, $\overline{CS}_1 \geq V_{CC}-0.2\text{V}$, CS ₂ $\geq V_{CC}-0.2\text{V}$ or CS ₂ $\leq 0.2\text{V}$	-	-	10	μA
			-	-	15	
			-	-	15	
			-	-	8	
			-	-	10	
Data retention set-up time	t _{SDR}	See data retention waveform	0	-	-	ms
Recovery time	t _{RDR}		5	-	-	

1. $\overline{CS}_1 \geq V_{CC}-0.2\text{V}$, CS₂ $\geq V_{CC}-0.2\text{V}$ ($\overline{CS}_1$: controlled) or CS₂ $\leq 0.2\text{V}$ (CS₂: controlled)

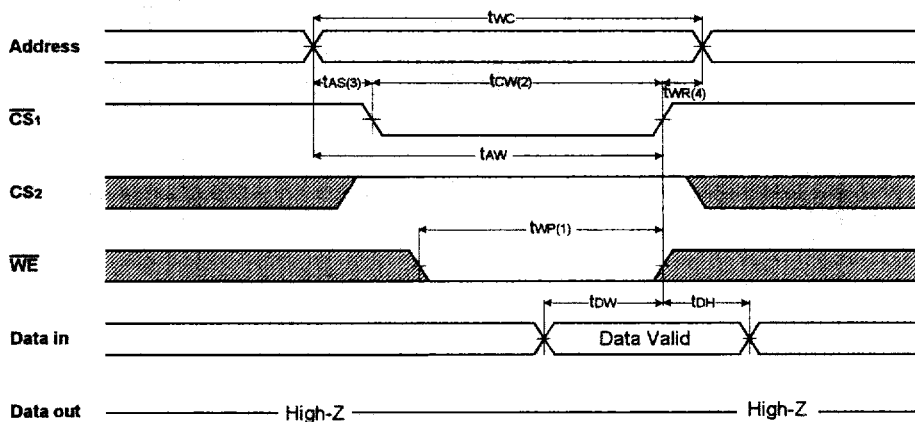
TIMMING DIAGRAMS
TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS1}=\overline{OE}=V_L$, $\overline{WE}=V_H$)

TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}=V_H$)

NOTES (READ CYCLE)

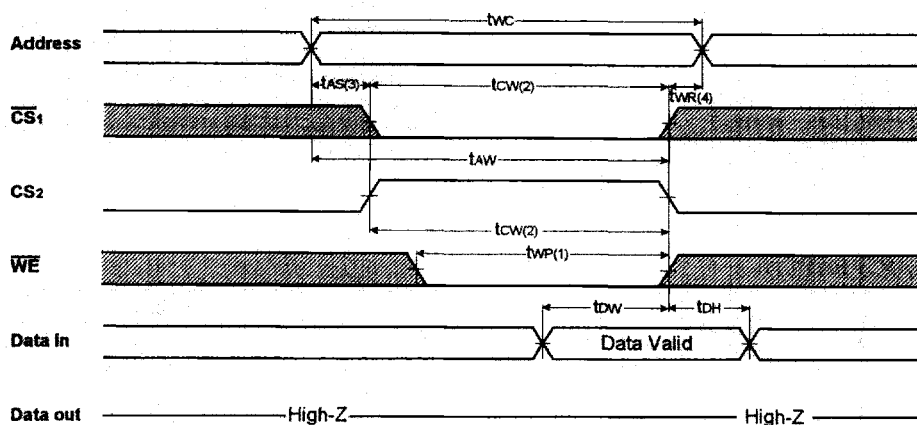
1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, $t_{HZ}(\text{Max.})$ is less than $t_{LZ}(\text{Min.})$ both for a given device and from device to device interconnection.

TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{WE}$ Controlled)

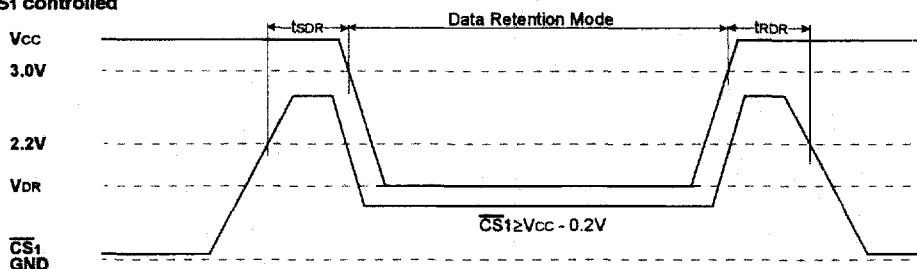


TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{CS_1}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(3) ($\overline{CS}_1$ Controlled)

NOTES (WRITE CYCLE)

1. A write occurs during the overlap of a low $\overline{CS}_1$, a high $\overline{CS}_2$ and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS}_1$ going low, $\overline{CS}_2$ going high and $\overline{WE}$ going low. A write ends at the earliest transition among $\overline{CS}_1$ going high, $\overline{CS}_2$ going low and $\overline{WE}$ going high. t_{WE} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the $\overline{CS}_1$ going low or $\overline{CS}_2$ going high to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. $t_{WR(1)}$ applied in case a write ends as $\overline{CS}_1$ or $\overline{WE}$ going high. $t_{WR(2)}$ applied in case a write ends as $\overline{CS}_2$ going low.

DATA RETENTION WAVE FORM
 $\overline{CS}_1$ controlled

 $\overline{CS}_2$ controlled
