Sound Output Circuit

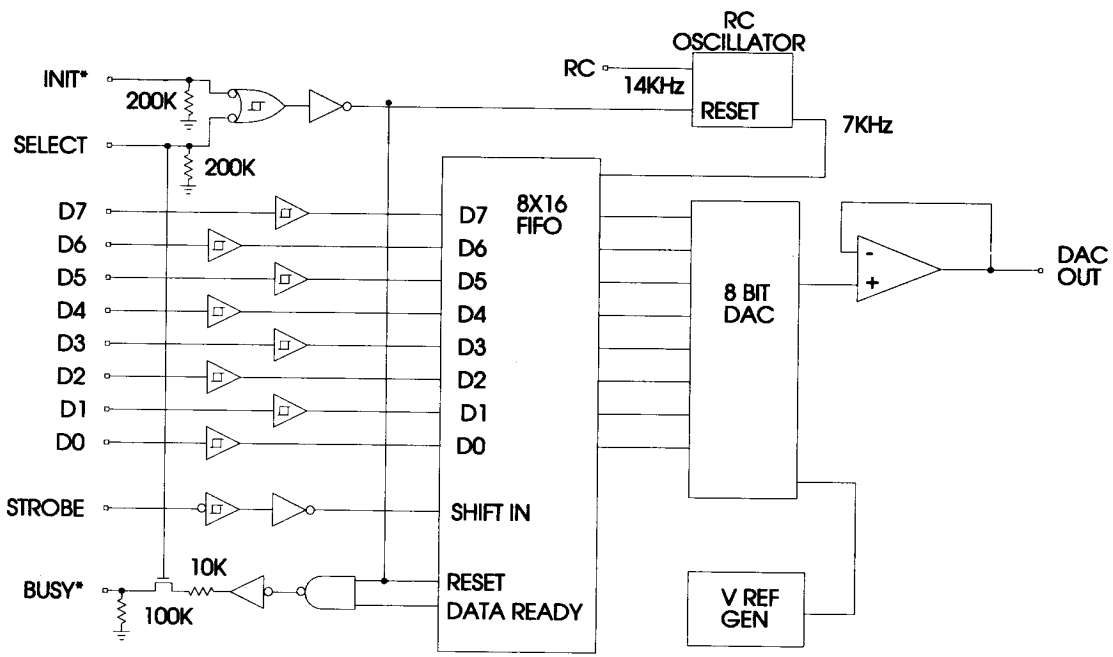
General Description

The **ICS2001** is a CMOS integrated circuit containing an 8-bit digital to analog converter fed by a 16-byte FIFO memory array. This device is intended to form the nucleus of a low-cost audio-output subsystem for personal computers, workstations, games, and talking books. The **ICS2001** is the core of the Disney Sound Source.™

Features

- 8-bit D/A converter
- 16-byte FIFO
- 5V and 9V operation
- TTL-level inputs with hysteresis
- RC clock oscillator
- Software drivers for DOS and Windows

Block Diagram

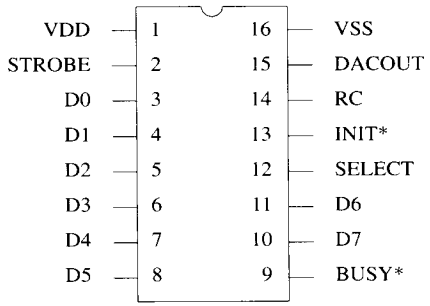


Ordering Information

ICS2001M (SO Package)
ICS2001N (DIP Package)

*Sound Source is a trademark of Walt Disney Computer Software Incorporated.

Pin Configuration



Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	VDD	Power	Positive power supply
2	STROBE	Input	Data strobe
3	D0	Input	Data input
4	D1	Input	Data input
5	D2	Input	Data input
6	D3	Input	Data input
7	D4	Input	Data input
8	D5	Input	Data input
9	BUSY*	Output	Busy (Active Low)
10	D7	Input	Data input
11	D6	Input	Data input
12	SELECT	Input	
13	INIT*	Input	Initialization (Active Low)
14	RC	Oscillator	One-pin oscillator
15	DACOUT	Output	Converter output
16	VSS	Power	Negative power supply/ground

Absolute Maximum Ratings

Storage temperature ..... -65 °C to 150 °C
Voltage on any pin with respect to ground..... -0.5V to V_{DD}+0.5V
Maximum V_{DD} 10.6V

Standard Test Conditions

Operating Temperature Range ..... 0 °C to 70 °C
Power Supply Voltage ..... 4.5 to 10.0V

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

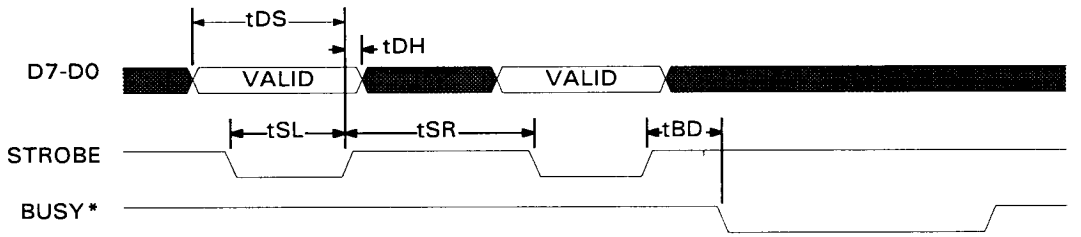
DC Characteristics

PARAMETER	SYMBOL	NOTES	MIN	TYP	MAX	UNITS
Logical 1 Input Voltage	V_{IH}		2.0		V_{DD}	V
Logical 0 Input Voltage	V_{IL}		0		0.8	V
Input Leakage Current	I_I	Any input	-1.0		1.0	uA
Input Hysteresis		Any input	20	50		mV
Pull down resistors		INIT*, SELECT	100	200	300	K ohm
Pull down resistor		BUSY*	50	100	200	K ohm
Supply Current	I_{DD}				5.0	mA
DAC output voltage	V_{DACOUT}	Data=$00 Data=$FF		V_{DD}/6 V_{DD}/2		V
DAC Differential Linearity			-1		+1	LSB
DAC Output Current	I_{DACOUT}	V_{DD}=4.5	200	500		uA
DAC Output Current	I_{DACOUT}	V_{DD}=9		1		mA
DAC Capacitive Load	C_L				20	pF
Output Current High	I_{OH}	V_{DD}=4.5V V_{OH}=2.0V	200	400		µA
Output Current Low	I_{OL}	V_{DD}=4.5V V_{OL}=.8V	200	400		µA

AC Characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator Frequency	F_{OSC}	R=160K; C=1000pF	12.6	14.0	15.4	kHz
Data Setup	T_{DS}		0			ns
Data Hold	T_{DH}		100			ns
STROBE Width Low	T_{SL}		50			ns
STROBE Recovery High	T_{SR}		50			ns
BUSY* Delay	T_{BD}	C_L=50pF			750	ns

Timing Diagram



Function Description

The overall operational status of the **ICS2001** is controlled by the INIT* and SELECT inputs. If either INIT* or SELECT is low, the chip is held in the "reset" condition: The BUSY* output is asserted, the STROBE input is ignored, and DAC OUT is forced to VDD/6 (minimum value). When INIT* *and* SELECT become high, the device enters the "run" condition, and BUSY* goes high indicating the FIFO is "ready for data."

Binary data is fed to the **ICS2001** via the D0-D7 pins and latched into the FIFO buffer by the rising edge of STROBE. Input data flow is controlled by the BUSY* output. Data in the FIFO is shifted out to the D/A converter at a rate established by the RC oscillator, typically 7 kHz. A data value of $00 will generate nominal output of VDD/6 volts, while a value of $FF will result in an output of VDD/2 volts.

The following steps represent a typical sound-playback sequence: SELECT is asserted causing BUSY* to go high indicating buffer ready for data. Data applied to pins D0-D7 are latched into the FIFO on the rising edge of STROBE. Additional bytes of data may be strobed in as long as BUSY* remains high. Thus, BUSY* is used to control the flow of data into the FIFO. SELECT is de-asserted after the last data byte has been written and sufficient time allowed for it to be reproduced.

Note that the first data byte strobed in under a "ready," *i.e.* BUSY*=1, status will ripple through to the D/A converter and its analog value appears on DAC OUT asynchronously. Subsequent bytes will be output at the data rate established by the RC clock as long as there is data in the FIFO. Therefore, it is recommended that sound samples be padded with a $00 leading byte to avoid time distortion between the first and second sample. Similar glitches may occur in the middle of sound sequences if the FIFO is allowed to empty.

Also note, that if the device is enabled (INIT* *and* SELECT=1) while the STROBE input is high, the current value of the data bus will be shifted into the FIFO. Therefore, during initialization for operation with STROBE pulsing low (statically high), valid data (usually $00) should be placed on the data inputs before the reset condition is removed.

In a typical application, the **ICS2001** shares a standard personal computer (Centronics) printer port with the system printer, and is powered by the same 9V source that supplies the external low-pass filter and speaker driver that comprise the balance of the sound subsystem. In the interest of simplicity and minimal cost, this power source is usually a battery.

In order to minimize unwanted current flow through the inputs of the **ICS2001** when the battery is disconnected or dead, all chip inputs should be connected to the printer port via series resistors with a nominal value of 10K ohms, and the power connection to the VDD pin should include a blocking diode. The BUSY* output, which normally drives an external NPN transistor, is provided with an internal 100K pull-down resistor to keep the transistor turned off when the **ICS2001** is not powered up.

The oscillator frequency is set by an external resistor and capacitor. The design center values are 160K ohms (from the RC pin to VDD) and 1000pF (from the RC pin to VSS). This results in a nominal clock frequency of 14 kHz plus or minus 5 percent. This signal is internally divided by two to yield an output sampling frequency of 7 kHz.