Features

- 32-bit RISC architecture
- Two instruction sets:
  - ARM high-performance 32-bit instruction set
  - Thumb high-code-density 16-bit instruction set
- Very low power consumption: Industry-leader in MIPS/Watt
- 4G Bytes linear address space
- Von Neumann load/store architecture:
  - Single 32-bit data bus for instructions and data
- 3-stage pipeline architecture:
  - Fetch, decode and execute stage
- 8-, 16-, and 32-bit data types
- Single cycle 32x8 hardware multiplier:
  - Multiplication is accelerated when upper bytes are all zero or one
- On-chip JTAG Debug and In Circuit Emulation

Description

The ARM7TDMI™ embedded microcontroller core is a member of the Advanced RISC Machines (ARM) family of general purpose 32-bit cores, which offer high performance and very lower power consumption. Its outstanding feature is the 16-bit Thumb subset of the most commonly used 32-bit instructions. These are expanded at run time with no less of system performance. This gives 16-bit code density (saving memory area and cost) coupled with 32-bit processor performance.

The ARM architecture is based on Reduced Instruction Set Computer (RISC) principles, and the instruction set and related decode mechanism are much simpler than those of microprogrammed Complex Instruction Set Computers. This simplicity results in a high instruction throughput and impressive real-time interrupt response from a small and cost-effective core.

Pipelining is employed so that all parts of the processing and memory systems can operate continuously. Typically, while one instruction is being executed, its successor is being decoded, and a third instruction is being fetched from memory.

The ARM memory interface has been designed to allow the performance potential to be realized without incurring high costs in the memory system. Speed-critical control signals are pipelined to allow system control functions to be implemented in standard low-power logic, and these control signals facilitate the exploitation of the fast local access modes offered by industry standard dynamic RAMs.

The ARM memory interface is also ideally suited to interfacing, either on-chip or off-chip, with Atmel's Flash memory blocks. These give the benefits of in-system programmability and security, reducing time-to-market and system cost.

This datasheet presents the electrical characteristics of the ARM7TDMI Embedded Core for the ATC35 process. See the ARM7TDMI Datasheet for the corresponding timing diagrams.

The Atmel ATC35 (AT56K) process is a proprietary 0.35 micron three-layer-metal CMOS process intended for use with a supply voltage of 3.3V $\pm$ 0.3V.

The following tables include low voltage performances (1.8V junction) to emulate 2.0V applications. The user must take into account, however, whether or not the other cells in the design can operate at these conditions.

ATC35 Electrical Characteristics

ARM7TDMI™ Embedded Core

Rev. 1249A–11/98

ATC35 AC Parameters

In the table below, SS1 emulates 3.0V worst case with voltage drop and noise immunity margins. SS2 emulates 2.0V worst case with voltage drop and noise immunity margins.

Table 1. Notes on AC Parameters

PVT	ff	typ	ss1	ss2
Process	fast	typ	slow	slow
Vjunction	3.6	3.3	2.85	1.8
Tjunction	-55	25	100	80

Note that "ns | ns/pf" in the array below means intrinsic delay(ns) or load dependant delay(ns/pf)

Table 2. ATC35 AC Parameters

		ff	typ	ss1	ss2
Symbol	**Parameter**	**ns | ns/pf**	**ns | ns/pf**	**ns | ns/pf**	**ns | ns/pf**
Tmckl	MCLK LOW time	5.40	7.24	11.32	22.78
Tmckh	MCLK HIGH time	5.40	7.24	11.32	22.78
Tws	nWAIT setup to MCLKr	0.47	0.62	1.00	1.88
Twh	nWAIT hold from MCKf	0.00	0.00	0.00	0.00
Tale	Address latch open	1.50 / 0.23	2.10 / 0.31	3.41 / 0.46	6.82 / 0.87
Taleh	Address latch hold time	1.15 / 0.17	1.65 / 0.22	2.70 / 0.34	5.20 / 0.47
Tald	Address latch time	1.43	1.89	2.91	5.32
Taddr	MCLKr to address valid	3.69 / 0.23	4.94 / 0.31	7.81 / 0.46	15.01 / 0.87
Tah	Address hold time from MCLKr	3.06 / 0.17	4.12 / 0.23	6.42 / 0.37	11.91 / 0.52
Tabe	Address bus enable time	1.47 / 0.23	1.97 / 0.31	3.07 / 0.46	5.72 / 0.87
Tabz	Address bus disable time	1.11	1.56	2.49	4.85
Taph	APE hold time from MCLKf	2.02	2.79	4.43	8.79
Taps	APE set up time to MCLKr	0.00	0.00	0.00	0.00
Tape	MCLKf to address valid	1.67 / 0.23	2.32 / 0.31	3.74 / 0.46	7.48 / 0.87
Tapeh	Address group hold time from MCLKf	1.32 / 0.17	1.89 / 0.22	3.04 / 0.34	5.79 / 0.46
Tdout	MCLKf to D[31:0] valid	3.88 / 0.22	5.33 / 0.29	8.45 / 0.40	16.23 / 0.78
Tdoh	D[31:0] out hold from MCLKf	3.10 / 0.24	4.21 / 0.32	6.60 / 0.46	12.19 / 0.82
Tdis	D[31:0] in setup time to MCLKf	0.02	0.00	0.00	0.84
Tdih	D[31:0] in hold time from MCLKf	1.31	1.48	1.99	3.40
Tdoutu	MCLKf to DOUT[31:0] valid	4.11 / 0.23	5.64 / 0.30	8.99 / 0.40	16.57 / 0.88
Tdohu	DOUT[31:0] hold time from MCLKf	2.51 / 0.17	3.48 / 0.22	5.52 / 0.34	10.23 / 0.48
Tdisu	DIN[31:0] set up time to MCLKf	0.31	0.28	0.55	2.07
Tdihu	DIN[hold time to MCLKf	1.01	1.02	1.18	1.91
Tnen	MCLKf to nENOUT valid	2.48 / 0.44	3.44 / 0.54	5.57 / 0.69	10.60 / 1.20
Tnenh	nENOUT hold time from MCLKf	1.66 / 0.36	2.37 / 0.46	3.79 / 0.65	6.83 / 0.87
Tbylh	BL[3:0] hold time from MCLKf	0.00	0.00	0.00	0.00

Table 2. ATC35 AC Parameters (Continued)

Symbol	Parameter	ff	typ	ss1	ss2
		ns | ns/pf	ns | ns/pf	ns | ns/pf	ns | ns/pf
Tbyls	BL[3:0] set up to from MCLKr	0.55	0.78	1.26	2.57
Tdbe	Data bus enable time from DBEr	3.03 / 0.24	4.26 / 0.29	6.85 / 0.40	13.26 / 0.77
Tdbz	Data bus disable time from DBEf	1.08	1.52	2.44	4.56
Tdbnen	DBE to nENOUT valid	1.34 / 0.44	1.63 / 0.61	2.34 / 0.90	4.27 / 1.75
Ttbz	Address and Data bus disable time from TBEf	1.32	1.77	2.79	5.11
Ttbe	Address and Data bus enable time from TBEr	1.56 / 0.24	2.23 / 0.28	3.56 / 0.39	6.94 / 0.77
Trwd	MCLKr to nRW valid	3.59 / 0.17	4.89 / 0.22	7.65 / 0.34	13.99 / 0.46
Trwh	nRW hold time from MCLKr	3.14 / 0.23	4.20 / 0.31	6.49 / 0.46	11.53 / 0.87
Tmsd	MCLKf to nMREQ & SEQ valid	6.00 / 0.44	7.28 / 0.46	11.99 / 0.65	26.00 / 0.87
Tmsh	nMREQ & SEQ hold time from MCLKf	2.58 / 0.37	3.68 / 0.46	5.82 / 0.66	10.59 / 0.90
Tbld	MCLKr to MAS[1:0] & LOCK	4.97 / 0.20	6.76 / 0.26	10.60 / 0.36	19.60 / 0.71
Tblh	MAS[1:0] & LOCK hold from MCLKr	3.74 / 0.17	4.99 / 0.24	7.82 / 0.37	14.22 / 0.47
Tmdd	MCLKr to nTRANS, nM[4:0], and TBIT valid	5.09 / 0.32	6.87 / 0.38	10.85 / 0.46	20.11 / 0.87
Tmdh	nTRANS & nM[4:0] hold time from MCLKr	3.65 / 0.23	5.05 / 0.28	7.94 / 0.42	14.14 / 0.69
Topcd	MCLKr to nOPC valid	3.12 / 0.23	4.18 / 0.31	6.50 / 0.46	12.17 / 0.87
Topch	nOPC hold time from MCLKr	2.93 / 0.17	3.98 / 0.22	6.22 / 0.33	11.12 / 0.46
Tcps	CPA, CPB setup to MCLKr	1.98	2.63	4.27	8.38
Tcph	CPA,CPB hold time from MCLKr	0.45	0.54	0.73	1.37
Tcpms	CPA, CPB to nMREQ, SEQ	2.37 / 0.44	3.12 / 0.61	4.83 / 0.90	9.31 / 1.74
Tcpi	MCLKf to nCPI valid	5.97 / 0.35	6.85 / 0.45	11.24 / 0.64	23.73 / 0.87
Tcpih	nCPI hold time from MCLKf	2.58 / 0.35	3.60 / 0.45	5.59 / 0.64	10.01 / 0.87
Tcts	Config setup time	0.55	0.67	1.09	2.92
Tcth	Config hold time	1.11	1.49	2.24	4.16
Tabts	ABORT setup time to MCLKf	0.00	0.00	0.00	0.00
Tabth	ABORT hold time from MCLKf	1.09	1.48	2.33	4.73
Tis	Asynchronous interrupt setup time to MCLKf for guaranteed recognition (ISYNC=0)	0.00	0.00	0.00	0.00
Tim	Asynchronous interrupt guaranteed non-recognition time (ISYNC=0)	0.58	0.90	1.47	2.66
Tsis	Synchronous nFIQ, nIRQ setup to MCLKf (ISYNC=1)	0.00	0.00	0.02	0.14
Tsih	Synchronous nFIQ, nIRQ hold from MCLKf (ISYNC=1)	0.11	0.13	0.18	0.33
Trs	Reset setup time to MCLKr for guaranteed recognition	0.00	0.00	0.00	0.00
Trm	Reset guaranteed non-recognition time	1.02	1.36	2.14	3.63
Texd	MCLKf to nEXEC valid	5.24 / 0.36	7.32 / 0.46	12.03 / 0.65	27.20 / 0.87

Table 2. ATC35 AC Parameters (Continued)

Symbol	Parameter	ff	typ	ss1	ss2
		ns | ns/pf	ns | ns/pf	ns | ns/pf	ns | ns/pf
Texh	nEXEC hold time from MCLKf	2.41 / 0.36	3.44 / 0.46	5.18 / 0.73	9.22 / 1.27
Tbrks	Set up time of BREAKPT to MCLKr	2.13	2.84	4.41	8.98
Tbrkh	Hold time of BREAKPT from MCLKr	0.55	0.67	0.92	1.73
Tbcems	BREAKPT to nCPI, nEXEC, nMREQ, SEQ delay	3.18 / 0.43	4.21 / 0.61	6.51 / 0.90	13.94 / 1.33
Tdbgd	MCLKr to DBGACK valid	5.12 / 0.44	6.55 / 0.61	10.01 / 0.90	18.10 / 1.75
Tdbgh	DGBACK hold time from MCLKr	3.41 / 0.36	4.80 / 0.46	7.68 / 0.65	14.72 / 0.87
Trqs	DBGRQ set up time to MCLKr for guaranteed recognition	0.43	0.51	0.70	1.35
Trqh	DBGRQ guaranteed non-recognition time	0.41	0.49	0.66	0.72
Tcdel	MCLK to ECLK delay	0.93 / 0.44	1.04 / 0.61	1.35 / 0.90	2.02 / 1.75
Tctdel	TCK to ECLK delay	2.91 / 0.44	3.76 / 0.61	5.67 / 0.90	10.31 / 1.75
Texts	EXTERN[1:0] set up time to MCLKf	0.00	0.00	0.00	0.00
Texth	EXTERN[1:0] hold time from MCLKf	1.16	1.58	2.46	4.35
Trg	MCLKf to RANGEOUT0, RANGEOUT1 valid	3.41 / 0.44	4.48 / 0.61	7.13 / 0.90	15.21 / 1.75
Trgh	RANGEOUT0, RANGEOUT1 hold time from MCLKf	1.64 / 0.36	2.37 / 0.46	3.80 / 0.65	7.04 / 0.87
Tdbgrq	DBGRQ to DBGRQI valid	1.08 / 0.44	1.25 / 0.61	1.70 / 0.90	2.88 / 1.75
Trstd	nRESETf to D[], DBGACK, nCPI, nENOUT, nEXEC, nMREQ, SEQ valid	2.87 / 0.42	3.93 / 0.51	6.36 / 0.65	11.98 / 1.16
Tcommd	MCLKr to COMMRX, COMMTX valid	2.29 / 0.44	2.97 / 0.61	4.46 / 0.90	8.31 / 1.75
Ttrstd	nTRSTf to every output valid	3.65 / 0.24	5.07 / 0.29	8.07 / 0.45	15.71 / 0.87
Trstl	nRESET LOW for guaranteed reset	2 minimum MCLK cycles			

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1249A–11/98/xM