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# VP5313/VP5513

## NTSC/PAL Digital Video Encoder

Supersedes DS4509 1.9 September 1997 edition

DS4509 - 2.2 October 1998

The VP5313/VP5513 converts digital Y Cr Cb data into analog PAL or NTSC composite video, and also provides simultaneous RGB outputs. These additional converters can optionally provide separate luma and chroma outputs plus a further composite video channel. All outputs are capable of driving doubly terminated 75Ω loads with standard video levels.

All D/A converters are to 9 bit accuracy, and are provided with 27MHz oversampled data. The latter simplifies the requirement for external analog anti-aliasing filters, and reduces the sinx/x distortion inherent in D/A converters. Separate digital scaling is applied to the chroma data path in order to make the most efficient use of the 9 bit dynamic range. The device accepts data inputs complying with CCIR recommendation 656. In this format 4:2:2 video is multiplexed onto an 8 bit bus using a 27MHz clock. Active video markers are embedded into the data stream and extracted by the VP5313/VP5513. Optionally the user can supply separate horizontal and vertical syncs, and colour can be genlocked to an external subcarrier if necessary.

In an alternative operating mode the VP5313/VP5513 can be configured as the source of sync for the rest of the system. In this master mode the horizontal and vertical sync pins become outputs, and any control codes in the CCIR656 bit stream are ignored.

The VP5313/VP5513 supports the insertion of teletext data through a serial interface. An internal filter shapes the data edges.

### FEATURES

- Converts Y, Cr, Cb data to analog RGB and composite or S-video and composite video
- Supports CCIR recommendations 601 and 656
- All digital video encoding
- Selectable master/slave mode for sync signals
- Switchable chrominance bandwidth
- CCIR 624 PAL SMPTE or 170M NTSC compatible outputs
- GENLOCK mode
- $I^2C$ bus serial microprocessor interface
- Only VP5313 supports Macrovision anti-taping Rev. 7.01
- Line 21 Closed Caption encoding
- Teletext insertion, fully line programmable

### APPLICATIONS

- Digital Cable TV
- Digital Satellite TV
- Multi-media
- Video games
- Digital VCRs
- Karaoke

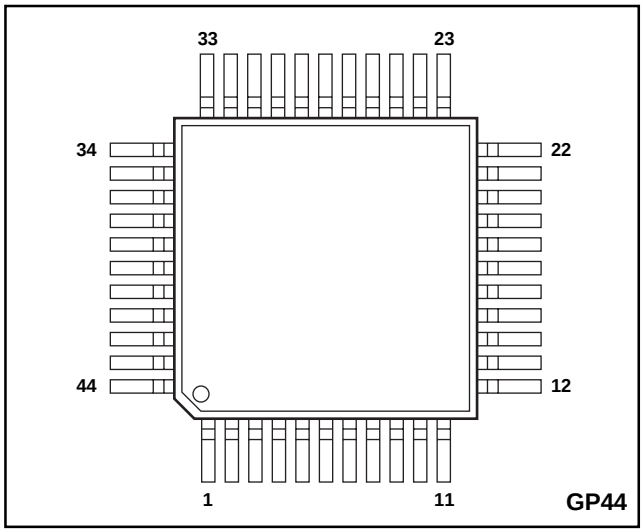



*Fig.1 Pin connections (top view)*

| PIN | FUNCTION | PIN | FUNCTION |
|---|---|---|---|
| 1 | VDD | 23 | SCL |
| 2 | PD5 | 24 | SDA |
| 3 | PD6 | 25 | DACCOMP |
| 4 | PD7 | 26 | RED/C |
| 5 | CLAMP | 27 | GREEN/Y |
| 6 | COMPSYNC | 28 | AVDD |
| 7 | PALID | 29 | AGND |
| 8 | SCSYNC | 30 | AVDD |
| 9 | REFSQ | 31 | BLUE/CVBS2 |
| 10 | GND | 32 | CVBS1 |
| 11 | VDD | 33 | VREF |
| 12 | FC2 | 34 | RREF |
| 13 | FC1 | 35 | AGND |
| 14 | FC0 | 36 | AGND |
| 15 | $\overline{\text{HSYNC}}$ | 37 | AVDD |
| 16 | $\overline{\text{VSYNC}}$ | 38 | PD0 |
| 17 | TTXREQ | 39 | PD1 |
| 18 | SA | 40 | PD2 |
| 19 | TTXDATA | 41 | PD3 |
| 20 | VDD | 42 | PD4 |
| 21 | GND | 43 | GND |
| 22 | $\overline{\text{RESET}}$ | 44 | PXCK |

### ORDERING INFORMATION

**VP5313A/CG/GP1N**
**VP5513A/CG/GP1N**

## RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| Power supply voltage | VDD, AVDD | 4.75 | 5.00 | 5.25 | V |
| Power supply current (including analog outputs)[1] | IDD | | | 230 | mA |
| Power supply current (including analog outputs)[2] | IDD | | | 190 | mA |
| Input clock frequency | PXCK | -50ppm | 27.00 | +50ppm | MHz |
| SCL clock frequency | $f_{SCL}$ | | | 500 | kHz |
| Analog video output load | | | 37.5 | | Ω |
| DAC gain resistor | | | 730 | | Ω |
| Ambient operating temperature | | 0 | | 70 | °C |

1. All four DACs driving 37R5 loads
2. All four DACs driving 75R loads

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated): As specified in Recommended Operating Conditions**

## DC CHARACTERISTICS

| Parameter | Conditions | Symbol | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| Digital Inputs TTL compatible (except SDA, SCL) | | | | | | |
| Input high voltage | | VIN | 2.0 | | | V |
| Input low voltage | | VIL | | | 0.8 | V |
| Digital Inputs SDA, SCL | | | | | | |
| Input high voltage | | VIH | 0.7VDD | | | V |
| Input low voltage | | VIL | | | 0.3VDD | V |
| Input high current | VIN = VDD | IIH | | | 10 | µA |
| Input low current | VIN = VSS | IIL | | | -10 | µA |
| Digital Outputs CMOS compatible | | | | | | |
| Output high voltage | IOH = -1mA | VOH | 3.7 | | | V |
| Output low voltage | IOL = +4mA | VOL | | | 0.4 | V |
| Digital Output SDA | | | | | | |
| Output low voltage | IOL = +6mA | VOL | | | 0.6 | V |

## DC CHARACTERISTICS DACs

| Parameter | Symbol | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| Accuracy (each DAC) | | | | | |
| Integral linearity error | INL | | | ±1.5 | LSB |
| Diffential linearity error | DNL | | | ±1 | LSB |
| DAC matching error | | | | ±5 | % |
| Monotonicity | | | guaranteed | | |
| LSB size | | | 66.83 | | µA |
| Internal reference voltage | $V_{REF}$ | 0.95 | 1.00 | 1.05 | V |
| Internal reference voltage output impedance | $Z_R$ | | 8k | | Ω |
| Reference Current ($V_{REF}/R_{REF}$) $R_{REF}$ = 730Ω | $I_{REF}$ | | 1.3899 | | mA |
| Maximum output | | | 34.15 | | mA |
| Peak Glitch Energy (see fig.3) | | | 50 | | pV-s |

## ABSOLUTE MAXIMUM RATINGS

| | | |
|---|---|---|
| Supply voltage | VDD, AVDD | -0·3 to 7·0V |
| Voltage on any non power pin | | -0·3 to VDD+0·3V |
| Ambient operating temperature | | 0 to 70°C |
| Storage temperature | | -55°C to 150°C |

Note: Stresses exceeding these listed under Absolute Maximum Ratings may induce failure. Exposure to Absolute Maximum Ratings for extended periods may reduce reliability. Functionality at or above these conditions is not implied.

## ESD COMPLIANCE

| Pins | Test | Test Levels | Notes |
|---|---|---|---|
| All pins | Human body model | 2kV on 100pF through 1k5Ω | Meets Mil-Std-883 Class 2 |
| All pins | Machine model | 200V on 200pF through 0Ω & 500nH | |

## DC CHARACTERISTICS DACs

| Parameter | Symbol | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| RGB outputs: | | | | | |
| Peak level | | | 19.98 | | mA |
| Black level | | | 1.337 | | mA |
| | | | | | |
| CVBS1, 2 Y and C outputs - NTSC (pedestal enabled) | | | | | |
| Maximum output, relative to sync bottom | | | 33.75 | | mA |
| White level relative to black level | | | 17.63 | | mA |
| Black level relative to blank level | | | 1.40 | | mA |
| Blank level relative to sync level | | | 7.61 | | mA |
| Colour burst peak - peak | | | 7.61 | | mA |
| DC offset (bottom of sync) | | | 0.40 | | mA |
| | | | | | |
| CVBS1, 2, Y and C outputs - PAL | | | | | |
| White level relative to black level | | | 18.70 | | mA |
| Black level relative to sync level | | | 8.01 | | mA |
| Colour burst peak - peak | | | 8.01 | | mA |
| DC offset (bottom of sync) | | | 0.00 | | mA |

All figures are for: RREF = 730Ω; if RL = 75Ω then RREF = 1460Ω

## VIDEO CHARACTERISTICS (NTSC, PAL COMPOSITE VIDEO)

| Parameter | Symbol | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| Luminance bandwidth | | | 5.5 | | MHz |
| Chrominance bandwidth (Extended B/w mode) | | | 1.3 | | MHz |
| Chrominance bandwidth (Reduced B/w mode) | | | 650 | | kHz |
| Burst frequency (NTSC) | | | 3.57954545 | | MHz |
| Burst frequency (PAL-B, D,G,H,I) | | | 4.43361875 | | MHz |
| Burst frequency (PAL-N Argentina) | | | 3.58205625 | | MHz |
| Burst cycles (NTSC and PAL-N) | | | 9 | | Fsc cycles |
| Burst cycles ( PAL-B, D, G, H,I) | | | 10 | | Fsc cycles |
| Burst envelope rise / fall time (NTSC ) | | | 300 | | ns |
| Burst envelope rise / fall time (PAL-B, D, G, H, I, N) | | | 300 | | ns |
| Analog video sync rise / fall time (NTSC) | | | 145 | | ns |
| Analog video sync rise / fall time (PAL-B, D, G, H,I) | | | 245 | | ns |
| Analog video blank rise / fall time (NTSC ) | | | 145 | | ns |
| Analog video blank rise / fall time (PAL-B, D, G, H,I) | | | 245 | | ns |
| Differential gain | | | | | % pk-pk |
| Differential phase | | | | 1 | ° pk-pk |
| Signal to noise ratio (unmodulated ramp) | | | | 1 | dB |
| Chroma AM signal to noise ratio (100% red field) | | | | -61 | dB |
| Chroma PM signal to noise ratio (100% red field) | | | | -56 | dB |
| Hue accuracy | | | | -58 | % |
| Colour saturation accuracy | | | | 2.5 | % |
| Residual sub carrier | | | -60 | 2.5 | dB |
| Luminance / chrominance delay | | | 5 | | ns |
| | | | | 10 | |

## PIN DESCRIPTIONS

| Pin Name | Pin No. | Description |
|---|---|---|
| PD0-7 | 2-4, 38-42 | 8 Bit Pixel Data inputs clocked by PXCK. PD0 is the least significant bit. These pins are internally pulled low. |
| PXCK | 44 | 27MHz Pixel Clock input. The VP5313/VP5513 internally divides PXCK by two to provide the pixel clock. |
| SA | 18 | Slave address select. |
| SCL | 23 | Standard $I^2C$ bus serial clock input. |
| SDA | 24 | Standard $I^2C$ bus serial data input/output. |
| FC0-2 | 12-14 | Field Counter output in master sync mode. |
| REFSQ | 9 | Reference square wave input used only during Genlock mode. |
| SCSYNC | 8 | Subcarrier sync input, (synchronises phase quadrant in 4xfsc genlock mode), see fig 6. |
| PALID | 7 | PAL IDENT input, controls swinging colour burst phase in PAL genlock mode. |
| COMPSYNC | 6 | Composite sync pulse output. This is an active low output signal. |
| CLAMP | 5 | The CLAMP output signal is synchronised to COMPSYNC output and indicates the position of the BURST pulse, (lines 10-263 and 273-525 for NTSC; lines 6-310 and 319-623 for PAL-B,D,G,I,N(Argentina)). |
| TTXREQ | 17 | Teletext Data Request output, requests next line of teletext data. |
| TTXDATA | 19 | Teletext Data input. |
| $\overline{\text{HSYNC}}$ | 15 | Horizontal Sync, output in master mode, input in slave mode |
| $\overline{\text{VSYNC}}$ | 16 | Vertical Sync, output in master mode, input in slave mode |
| $\overline{\text{RESET}}$ | 22 | Master reset. This is an asynchronous, active low, input signal and must be asserted for a minimum 200ns in order to reset the VP5313/VP5513. |
| VREF | 33 | Voltage reference output. This output is nominally 1·0V and should be decoupled with a 100nF capacitor to GND. |
| RREF | 34 | DAC full scale current control. A resistor connected between this pin and GND sets the magnitude of the video output current. An internal loop amplifier controls a reference current flowing through this resistor so that the voltage across it is equal to the Vref voltage. This reference current has a weighting equal to 20.8 LSB's. |
| DACCOMP | 25 | DAC compensation. A 100nF ceramic capacitor must be connected to AVDD. |
| CVBS1 | 32 | Composite video output. These are high impedance current source outputs. A DC path to GND must exist from each of these pins. |
| BLUE/CVBS2 | 31 | Blue or composite DAC output. Output type as CVBS1. |
| GREEN/Y | 27 | Green or luminance DAC output. Output type as CVBS1. |
| RED/C | 26 | Red or chrominance DAC output. Output type as CVBS1. |
| VDD | 1, 11, 20 | Positive supply input. All VDD pins must be connected. |
| AVDD | 37,28,30 | Analog positive supply input. All AVDD pins must be connected. |
| GND | 10,21,43 | Negative supply input. All GND pins must be connected. |
| AGND | 36,29,35 | Analog negative supply input. All AGND pins must be connected. |

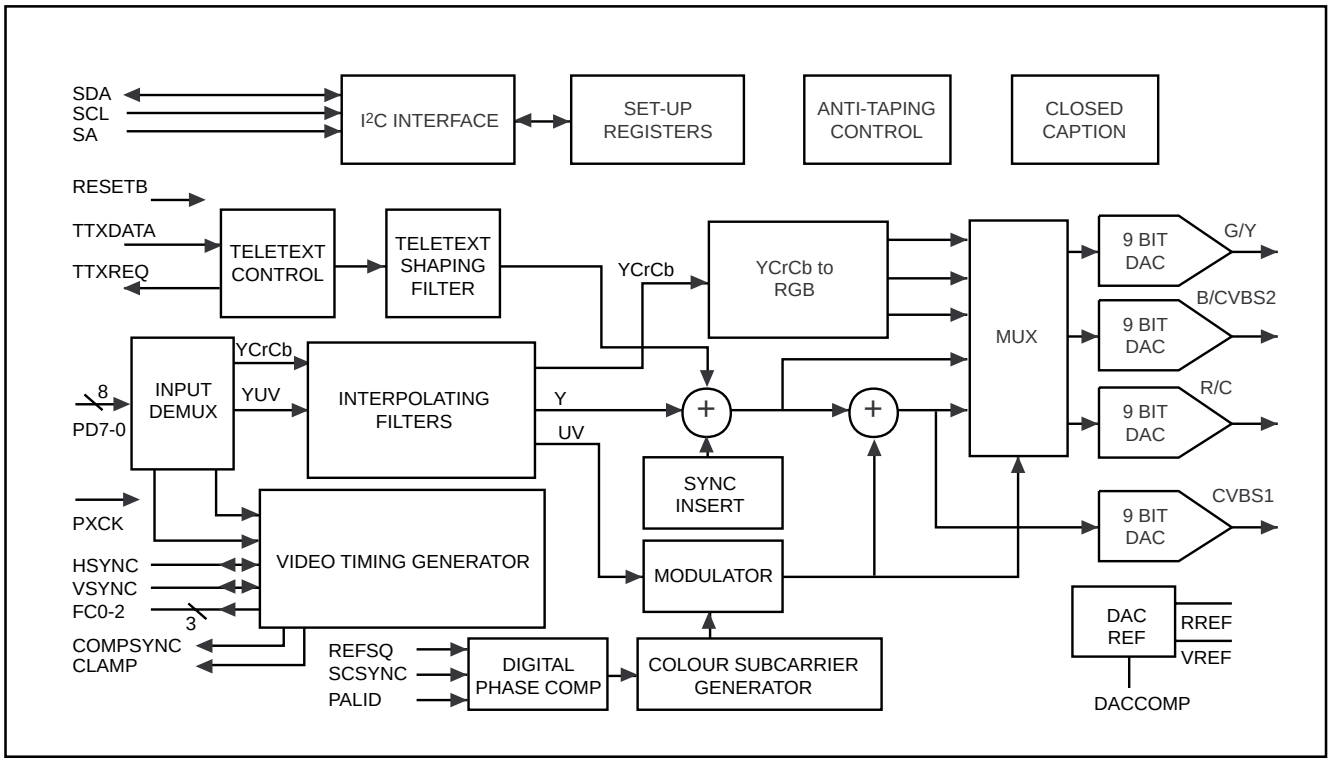
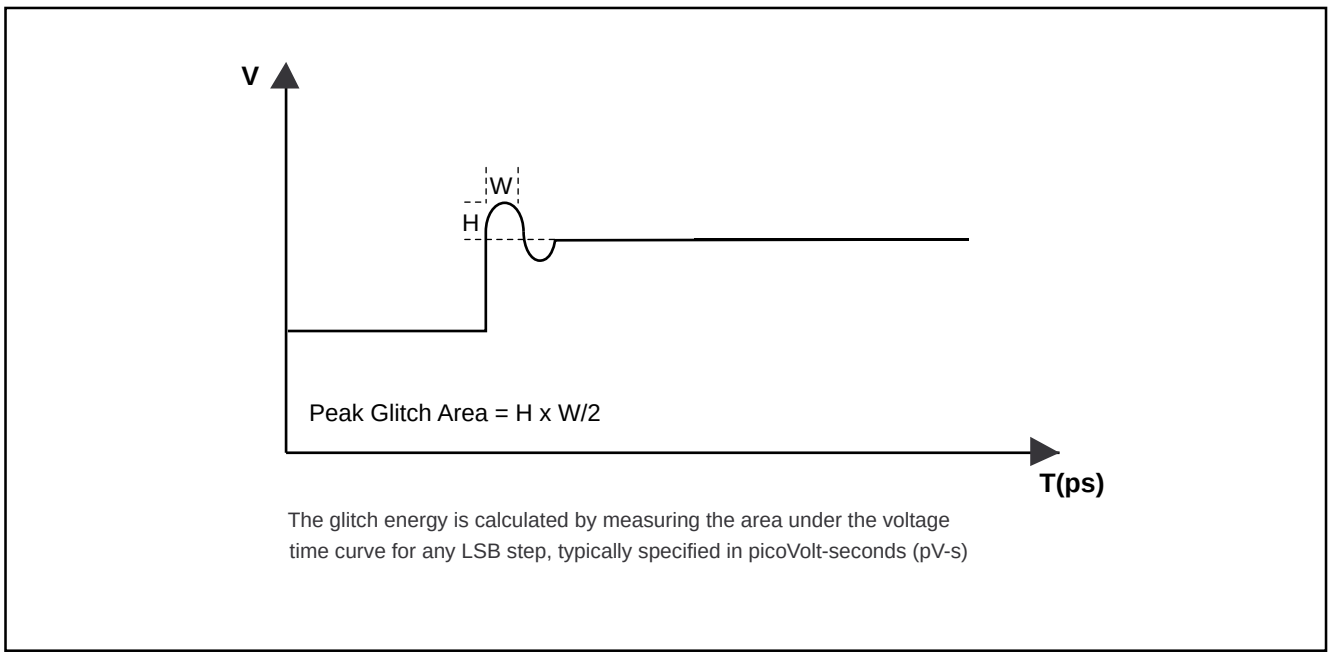



*Figure 2 Functional block diagram*




The glitch energy is calculated by measuring the area under the voltage time curve for any LSB step, typically specified in picoVolt-seconds (pV-s)

*Figure 3 Glitch Energy (see Peak Glitch Energy in table on page 2)*

## REGISTERS MAP

See Register Details for further explanations.

| ADDRESS hex | REGISTER NAME | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | R/W | DEFAULT hex |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | BAR | RA7 | RA6 | RA5 | RA4 | RA3 | RA2 | RA1 | RA0 | W | |
| 00 | PART ID2 | ID17 | ID16 | ID15 | ID14 | ID13 | ID12 | ID11 | ID10 | R | 00 |
| 01 | PART ID1 | ID0F | ID0E | ID0D | ID0C | ID0B | ID0A | ID09 | ID08 | R | 53 |
| 02 | PART ID0 | ID07 | ID06 | ID05 | ID04 | ID03 | ID02 | ID01 | ID00 | R | 13 |
| 03 | REV ID | REV7 | REV6 | REV5 | REV4 | REV3 | REV2 | REV1 | REV0 | R | 01 |
| 04 | MODE | - | - | - | DACCFG | VFS1 | VFS0 | SYNCM1 | SYNCM0 | R/W | 00 |
| 05 | GCR | FSC4SEL | GENDITH | GENLKEN | NOLOCK | PALIDEN | YCDELAY | CLMPDIS | CVBSCLMP | R/W | 00 |
| 06 | VOCR | DITHEN | CHRMCLIP | CHRBW | SYNCDIS | BURDIS | LUMDIS | CHRDIS | PEDEN | R/W | 20 |
| 07 | RSTCTL | | | | | | | | TSURST | R/W | 00 |
| 08 | SC_ADJ | SC7 | SC6 | SC5 | SC4 | SC3 | SC2 | SC1 | SC0 | R/W | 9C |
| 09 | FREQ2 | FR17 | FR16 | FR15 | FR14 | FR13 | FR12 | FR11 | FR10 | R/W | A8 |
| 0A | FREQ1 | FR0F | FR0E | FR0D | FR0C | FR0B | FR0A | FR09 | FR08 | R/W | 26 |
| 0B | FREQ0 | FR07 | FR06 | FR05 | FR04 | FR03 | FR02 | FR01 | FR00 | R/W | 2B |
| 0C | SCHPHM | - | - | - | - | - | - | - | SCH8 | R/W | 00 |
| 0D | SCHPHL | SCH7 | SCH6 | SCH5 | SCH4 | SCH3 | SCH2 | SCH1 | SCH0 | R/W | 00 |
| 0E | HSOFFL | HSOFF7 | HSOFF6 | HSOFF5 | HSOFF4 | HSOFF3 | HSOFF2 | HSOFF1 | HSOFF0 | R/W | 7E |
| 0F | HSOFFM | - | - | - | - | - | - | HSOFF9 | HSOFF8 | R/W | 00 |
| 10 | SLAVE1 | NCORSTD | VBITDIS | VSMODE | F_SWAP | SL_HS1 | SL_HS0 | HCNT9 | HCNT8 | R/W | 00 |
| 11 | SLAVE2 | HCNT7 | HCNT6 | HCNT5 | HCNT4 | HCNT3 | HCNT2 | HCNT1 | HCNT0 | R/W | 00 |
| 12 | TSTPAT | - | - | - | - | - | - | TTXPAT | RAMPEN | R/W | 00 |
| 13-1F | Not used | | | | | | | | | | |
| 20-33 | Reserved | | | | | | | | | | |
| 34-3F | Not used | | | | | | | | | | |
| 40 | TTXLO2 | - | - | - | - | - | - | - | L6 | R/W | 00 |
| 41 | TTXLO1 | L14 | L13 | L12 | L11 | L10 | L9 | L8 | L7 | R/W | 00 |
| 42 | TTXLO0 | L22 | L21 | L20 | L19 | L18 | L17 | L16 | L15 | R/W | 00 |
| 43 | TTXLE2 | - | - | - | - | - | - | L319 | L318 | R/W | 00 |
| 44 | TTXLE1 | L327 | L326 | L325 | L324 | L323 | L322 | L321 | L320 | R/W | 00 |
| 45 | TTXLE0 | L335 | L334 | L333 | L332 | L331 | L330 | L329 | L328 | R/W | 00 |
| 46 | TTXDD | TTXDD7 | TTXDD6 | TTXDD5 | TTXDD4 | TTXDD3 | TTXDD2 | TTXDD1 | TTXDD0 | R/W | 01 |
| 47 | TTXCTL | | | | | | | | TTXEN | R/W | 00 |
| 48-4F | Not used | | | | | | | | | | |
| 50 | CCREG1 | - | F1W1D6 | F1W1D5 | F1W1D4 | F1W1D3 | F1W1D2 | F1W1D1 | F1W1D3 | R/W | XX |
| 51 | CCREG2 | - | F1W2D6 | F1W2D5 | F1W2D4 | F1W2D3 | F1W2D2 | F1W2D1 | F1W2D3 | R/W | XX |
| 52 | CCREG3 | - | F2W1D6 | F2W1D5 | F2W1D4 | F2W1D3 | F2W1D2 | F2W1D1 | F2W1D3 | R/W | XX |
| 53 | CCREG4 | - | F2W2D6 | F2W2D5 | F2W2D4 | F2W2D3 | F2W2D2 | F2W2D1 | F2W2D3 | R/W | XX |
| 54 | CC_CTL | - | - | - | - | F2ST | F1ST | F2EN | F1EN | R/W | 00 |
| 55-5F | Not used | | | | | | | | | | |
| 60 | IICEXCTL | CTL7 | CTL6 | CTL5 | CTL4 | CTL3 | CTL2 | CTL1 | CTL0 | W | FF |
| 61 | IICEXW/R | W/RD7 | W/RD6 | W/RD5 | W/RD4 | W/RD3 | W/RD2 | W/RD1 | W/RD0 | R/W | - |
| 62-FD | Not used | | | | | | | | | | |
| FE-FF | Reserved | | | | | | | | | | |

*Table.1 Register map*

## REGISTER DETAILS

**BAR** **Base register**
RA7-0 Register address

**PART ID 2-0** **Part number**
ID17-00 Chip part ID number

**REV ID** **Revision number**
REV7-0 Chip revision ID number

**MODE** **Mode Control**

| DACCFG | |
|---|---|
| 0 | R,G,B & CVBS analog outputs |
| 1 | Y,C, CVBS1 & CVBS2 analog outputs |

| VFS1 | VFS0 | Video Standard |
|---|---|---|
| 0 | 0 | PAL-B,D,G,H,I,N(Arg.) |
| 0 | 1 | NTSC |
| 1 | 0 | Reserved |
| 1 | 1 | Reserved |

| SYNCM1 | SYNCM0 | Sync mode |
|---|---|---|
| 0 | 0 | Slave, Rec. 656 |
| 0 | 1 | Slave H & V I/P |
| 1 | 0 | Master H & V O/P |
| 1 | 1 | Reserved |

**GCR** **Global Control**

| FSC4SEL | Input subcarrier frequency select |
|---|---|
| 0 | REFSQ I/P = Fsubcarrier<br>SCSYNC I/P ignored |
| 1 | REFSQ I/P = 4 x Fsubcarrier<br>When SCSYNC I/P is asserted the<br>REFSQ I/P divide by 4 is reset |

| GENDITH | Genlock dither addition control |
|---|---|
| 0 | No dither added |
| 1 | Dither added |

| GENLKEN | Genlock enable control |
|---|---|
| 0 | Internal subcarrier generation |
| 1 | When high, enable Genlock to REFSQ |

| NOLOCK | Genlock status bit (read only) |
|---|---|
| 0 | Genlocked |
| 1 | Cannot lock to REFSQ.<br>This bit is cleared by reading and set<br>again if lock cannot be attained. |

| PALIDEN | PAL Ident select |
|---|---|
| 0 | Normal operation, internal PAL switch<br>is used. |
| 1 | Enables PALID input, a phase control<br>an for PALID signal, (0 = +135°, 1 = -135°) |

| YCDELAY | Add delay to luma channel |
|---|---|
| 0 | Luma to Chroma delay, 0ns |
| 1 | Luma to Chroma delay, 37ns |

| CLAMPDIS | CLAMP O/P select |
|---|---|
| 0 | CLAMP O/P enabled |
| 1 | CLAMP O/P disabled |

| CVBSCLAMP | Composite clamp enable |
|---|---|
| 0 | CVBS Clamp disabled |
| 1 | Clamps CVBS output, to prevent out of<br>range DAC codes. |

**VOCR** **Video Output Control**

| DITHEREN | Luma dither enable |
|---|---|
| 0 | Normal operation |
| 1 | Luma dither enabled |

| CHRMCLIP | Chroma clipping select |
|---|---|
| 0 | No chroma clipping |
| 1 | Enable clipping of chroma data when<br>luma is clipped |

| CHRBW | Chroma bandwidth select |
|---|---|
| 0 | ±650kHz |
| 1 | ±1·3MHz |

| SYNCDIS | Sync disable (in CVBS signal) |
|---|---|
| 0 | Normal operation |
| 1 | Sync disabled<br>(COMPSYNC O/P is not affected) |

| BURDIS | Chroma burst disable |
|---|---|
| 0 | Normal operation |
| 1 | Chroma burst disabled |

| LUMDIS | Luma input disable - force black level |
|---|---|
| 0 | Normal operation |
| 1 | Luma disabled |

| CHRDIS | Chroma input disable - force monochrome |
|---|---|
| 0 | Normal operation |
| 1 | Chroma disabled |

| PEDEN | Pedestal (set-up) select<br>Valid for NTSC |
|---|---|
| 0 | Pedestal disabled |
| 1 | 7·5 IRE pedestal on lines<br>23-262 and 286-525 |

**RSTCTL** **Reset Data Control**

| TSURST | Soft reset control |
|---|---|
| 0 | Normal operation |
| 1 | Chip soft reset |

**SC_ADJ** **Sub Carrier Adjust**
SC7-0 Sub carrier frequency seed value.

**FREQ2-0** **Sub carrier frequency**
FR17-00 24 bit Sub carrier frequency programmed via $I^2C$ bus. FREQ3 is the MSB.

**SCHPHM-L** **Sub carrier phase offset**
SCH8-0 9 bit Sub carrier phase relative to the 50% point of the leading edge of the horizontal part of composite sync. SCHPHM bit 0 is the MSB.

**HSOFFL-M** **Horizontal Sync Output Offset**
HSOFF9-0 This is a 10 bit number which allows the user to offset the start of digital data input with reference to the pulse HS.

**SLAVE1-2** **H & V Slave Mode Control**

| NCORSTD | NCO line reset disable |
|---|---|
| | NCO is always reset at end of 4(8) field sequence in NTSC(PAL) regardless of the value of this control bit |
| 0 | NCO is reset every line in NTSC mode |
| 1 | NCO line reset is disabled |

| VBITDIS | Ignore REC656 V-bit select |
|---|---|
| 0 | REC656 V-bit will be decoded and the line blanked accordingly |
| 1 | REC656 V-bit will be ignored |

| VSMODE | Select type of Vsync input |
|---|---|
| 0 | Standard Vsync I/P |
| 1 | Field even/odd Vsync I/P |

| F_SWAP | Invert field detect decision |
|---|---|
| 0 | Standard relationship applies |
| 1 | Inverted relationship applies |

| SL_HS(1:0) | Internal Hsync delay control |
|---|---|
| 00 | No internal delay |
| 01 | 1 x 27MHz cycle delay |
| 10 | 2 x 27MHz cycle delay |
| 11 | 3 x 27MHz cycle delay |

**TSLAVE2** HCNT(9:0) - Internal H counter is reset to this value on falling edge of Hsync input.

**TSTPAT** **Test Pattern Register**

| TTX_PAT | Teletext test pattern enable |
|---|---|
| 0 | Normal operation |
| 1 | Teletext test pattern enabled |

| RAMPEN | Modulated test ramp enable |
|---|---|
| 0 | Normal operation |
| 1 | Modulated test ramp enabled |

**TTXLO2-0** **Teletext Odd Line Enable**
L6-22 1 = Teletext Enabled on that line number

**TTXLE2-0** **Teletext Even Line Enable**
L318-335 1 = Teletext Enabled on that line number

**TTXDD7-0** **Teletext Request Pulse Position**

**TTXCTL** **Teletext Control**

| TTXEN | Teletext enable |
|---|---|
| 0 | Teletext disabled |
| 1 | Teletext enabled |

**CCREG1** **Closed Caption register 1**
F1W1D6-0 Field one (line 21), first data byte

**CCREG2** **Closed Caption register 2**
F1W2D6-0 Field one (line 21), second data byte

**CCREG3** **Closed Caption register 3**
F2W2D6-0 Field two (line 284), first data byte

**CCREG4** **Closed Caption register 4**
F2W2D6-0 Field two (line 284), second data byte

**CCCTL** **Closed Caption control register**

| F1ST | Field one (line 21) status bit |
|---|---|
| 0 | New data has been loaded to CCREG1-2 |
| 1 | Data has been encoded |

| F2ST | Field one (line 284) status bit |
|---|---|
| 0 | New data has been loaded to CCREG3-4 |
| 1 | Data has been encoded |

| F1EN | Closed Caption field one (line 21) |
|---|---|
| 0 | Disabled |
| 1 | Enabled |

| F2EN | Closed Caption field one (line 284) |
|---|---|
| 0 | Disabled |
| 1 | Enabled |

**IICEXCTL** **I²C Extension Control**
CTL7-0 Each bit controls port direction
0 = output 1 = input

**IICEXR/W** **I²C Extension Control**
RD7-0 I²C bus read and write data from I²C extension port

## I²C BUS CONTROL INTERFACE

### I²C bus address

| A6 | A5 | A4 | A3 | A2 | A1 | A0 | R/ $\overline{W}$ |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 1 | 0 | SA | X |

The serial microprocessor interface is via the bi-directional port consisting of a data (SDA) and a clock (SCL) line. It is compatible to the Philips I²C bus standard (Jan. 1992 publication number 9398 393 40011). The interface is a slave transmitter - receiver with a sub-address capability. All communication is controlled by the microprocessor. The SCL line is input only. The most significant bit (MSB) is sent first. Data must be stable during SCL high periods.

A bus free state is indicated by both SDA and SCL lines being high. START of transmission is indicated by SDA being pulled low while SCL is high. The end of transmission, referred to as a STOP, is indicated by SDA going from low to high while SCL is high. The STOP state can be omitted if a repeated START is sent after the acknowledge bit. The reading device acknowledges each byte by pulling the SDA line low on the ninth clock pulse, after which the SDA line is released to allow the transmitting device access to the bus.

The device address can be partially programmed by the setting of the pin SA. This allows the device to respond to one of two addresses, providing for system flexibility. The I²C bus address is seven bits long with the last bit indicating read/$\overline{\text{write}}$ for subsequent bytes.

The first data byte sent after the device address, is the sub-address - BAR (base address register). The next byte will be written to the register addressed by BAR and subsequent bytes to the succeeding registers. The BAR maintains its data after a STOP signal.

### NTSC/PAL Video Standards

Both NTSC (4-field, 525 lines) and PAL (8-field, 625 lines) video standards are supported by the VP5313/VP5513. All raster synchronisation, colour sub-carrier and burst characteristics are adapted to the standard selected. The VP5313/VP5513 generates outputs which follow the requirements of SMPTE 170M and CCIR 624 for PAL signals.

The device supports the following standards:
PAL B, D, G, H, I, N (Argentina) (default state) and NTSC.

### Video Blanking

The VP5313/VP5513 automatically performs standard composite video blanking. Lines 1-9, 264-272 inclusive, as well as the last half of line 263 are blanked in NTSC mode. In PAL mode, lines 1-5, 311-318, 624-625 inclusive, as well as the last half of line 623 are blanked.

The V bit within REC656 defines the video blanking when in TRS slave mode. By setting VBITDIS in the SLAVE1 register this blanking can be overidden. When in MASTER mode the V bit is ignored; hence, if any lines are required to be blank, they must have no video signal input on them.

### Interpolator

The luminance and chrominance data is separately passed through interpolating filters to produce output sampling rates double that of the incoming pixel rate. This reduces the sinx/x distortion that is inherent in the digital to analog converters (DACs), and also simplifies the analog reconstruction filter requirements.

### Digital to Analog Converters

The VP5313/VP5513 contains four 9 bit digital to analog converters which produce the analog video signals. The DACs use a current steering architecture in which bit currents are routed to one of two outputs; thus the DAC has true and complimentary outputs, however, only the true outputs are available on the pins. The use of identical current sources and current steering their outputs means that monoticity is guaranteed. An on-chip voltage reference of 1·00V (typ.) provides the necessary biasing; if required, this can be overridden by an external reference.

The full-scale output currents of the DACs is set by an external 730Ω resistor between the RREF and AGND pins. An on-chip loop amplifier stabilises the full-scale output current against temperature and power supply variations.
By digitally summing the luma and chroma outputs a composite output is generated. The analog outputs of the VP5313/VP5513 are capable of directly driving doubly terminated 75Ω co-axial cable. If it is required only to drive a single 75Ω load then the DACGAIN resistor is simply doubled.

### Luminance, Chrominance and Composite Video Outputs

The Luminance video output drives a 37.5Ω load at 1·0V, sync tip to peak white. It contains only the luminance content of the image plus the composite sync pulses. In the NTSC mode, a set-up level offset is added during the active video portion of the raster.

The Chrominance video output drives a 37.5Ω load at levels proportional in amplitude to the luma output (40 IRE pk-pk burst). Burst is injected with the appropriate timing relative to the luma signal.

Output sinx/x compensation filters are required on all video outputs, as shown in the typical application diagram, see fig. 11 & 12.

### RGB Video Outputs

The RGB video outputs drive a 37.5Ω load at 0.7V blank to peak.

Output sinx/x compensation filters are required on all video outputs, as shown in the typical application diagram, see fig. 11 & 12.

### Video Timing - Slave sync mode

The VP5313/VP5513 has an internal timing generator which produces video timing signals appropriate to the mode of operation. TRS slave mode means that the video encoder synchronises itself to the TRS (Timing Reference Signal) codes that are embedded into the Rec. 656 data pattern. In the

default (power up) the TRS slave mode is selected. All internal timing signals are derived from the input clock, (PXCK) this must be derived from a crystal controlled oscillator. Input pixel data is latched on the rising edge of the PXCK clock.
The video timing generator produces the internal blanking and burst gate pulses, together with the composite sync output signal.

H&V slave mode is enabled by setting the SYNCM1-0 bits in the MODE register to 01. In this mode the position of the video syncs is derived from the HS and VS inputs. These HS and VS pins are automatically configured as inputs.

**Video Timing - Master sync mode**

When SYNCM1-0 of the MODE register are 10, the VP5313/VP5513 operates in a MASTER sync mode, all REC656 timing reference codes are ignored with VS, HS and FC0-2 outputs providing synchronisation signals to an external (MPEG) device. The PXCK signal is, however, still used to generate all internal clocks. In master mode the direction setting of bits 4 - 0 of the IICEXCTL register are ignored.

VS is the start of the field sync datum in the middle of the equalisation pulses. HS is the line sync which is used by the preceding MPEG2 decoder to define when to output digital video data to the VP5313/VP5513. The position of the falling edge of HS relative to the first data Cb0, can be programmed in HSOFFM-L registers, see figure 5.

**Genlock using REFSQ input**

The VP5313/VP5513 can be Genlocked to another video source by setting GENLKEN high (in GCR register) and feeding a phase coherent sub carrier frequency signal into REFSQ. Under normal circumstances, REFSQ will be the same frequency as the sub carrier; however if FSC4SEL is set high (in GCR register), a 4 x sub carrier frequency signal may be input to REFSQ. In this case, the Genlock circuit can be reset to the required phase of REFSQ, by supplying a pulse to SCSYNC. The frequency of SCSYNC can be at the sub carrier frequency, once per line or once per field could be adequate, depending on the application. When GENLKEN is set high, the direction setting of bit 5 of the IICEXCTL register is ignored.

**PALID input**

When using PAL and Genlock mode; the VP5313/VP5513 requires a PAL phase identification signal, to define the correct phase on every line. This is supplied to PALID input, High = -135° and low = +135°. The signal is asynchronous, and should by changed before the sub carrier burst signal. PALID input is enabled by setting PALIDEN high (in GCR register). When PALIDEN is set high, the direction setting of bit 7 of the IICEXCTL register is ignored.

**Line 21 coding**

Two bytes of data are coded on the line 21 of each field, see figure 8. In the NTSC Closed Caption service, the default state is to code on line 21 of field one only. An additional service can also be provided using line 21 (284) of the second field. The data is coded as NRZ with odd parity, after a clock run-in and framing code. The clock run-in frequency = 0.5034965MHz which is related to the nominal line period, D = H / 32.

$$D = 63.55555556 / 32\mu s$$

Two data bytes per field are loaded via $I^2C$ bus registers CCREG1-4. Each field can be independently enabled by programming the enable bits in the control register (CC_CTL). The data is cleared to zero in the Closed Caption shift registers after it has been encoded by the VP5313/VP5513. Two status bit are provided (in CC_CTL), which are set high when data is written to the registers and set low when the data has been encoded on the Luma signal. The data is cleared to zero in the Closed Caption shift registers after it has been encoded by the VP5313/VP5513. The next data bytes must be written to the registers when the status bit goes high, otherwise the Closed Caption data output will contain Null characters. If a transmission slot is missed (ie. no data received) the encoder will send Null characters. Null characters are invisible to a closed caption reciever. The MSB (bit 7) is the parity bit and is automatically added by the encoder.

**Teletext**

The Teletext function within the VP5313/VP5513 co-ordinates the insertion of teletext serial data into the luminance data stream and subsequently the composite video data stream.

The serial data is filtered prior to insertion to minimise the high frequency components and to reduce the jitter inherent in the digital data stream.

The lines in which teletext data are inserted are individually programmable for both even and odd fields. The insertion of teletext data will only be enabled if the format of the composite video is configured to be PAL-B,G,H,I,N and the teletext enable bit TTXEN is asserted.

For test purposes, the teletext function incorporates control logic to generate a serial clock cracker pattern in place of the normal teletext data. This test pattern is enabled when the TTX_PAT bit is asserted. There is no row coding used so it will not display on a TV.

The VP5313/VP5513 teletext interface comprises of a teletext request output, TTX_REQ, and a serial data input, TTX_DATA.

To ensure that the composite video timing requirements are satisfied, the serial data must be received at a specific point in time during lines containing teletext data. The teletext request output, TTX_REQ, will be asserted to indicate when data must be applied to TTX_DATA, which must be generated synchronous to the rising edges of PXCK. The TTX_REQ may be advanced in multiples of PXCK, to compensate for the latency within the source device, by writing to the TTXDD register.

The serial teletext data which is applied to the TTX_DATA input must obey the sequence defined below.

The teletext bit rate is defined to be 6.9375 MHz, which equates to 444 times the PAL line frequency (15.625 kHz). It is clear that for a 27 MHz system clock, a constant bit period cannot be achieved.

The horizontal line duration for PAL equates to 1728 CLK27M cycles and within each line there are 444 data bit periods. The duration of 37 data bits (the smallest number possible for an integer number of CLK27M cycles) therefore equates to 144 CLK27M cycles.

To ensure that the average bit rate is 6.9375 MHz, 33 in every 37 data bits will have a duration of 4 CLK27M cycles and 4 in every 37 data bits will have a duration of 3 CLK27M cycles. Of the first 37 data bits in each line, bits 10, 19, 28 and 37 will have a duration of 3 CLK27M cycles. The sequence will be repeated for all subsequent 37 bit groups.

**Master Reset**

The VP5313/VP5513 must be initialised with $\overline{\text{RESET}}$. This is an asynchronous, active low signal and must be active for a minimum of 200ns in order to reset the VP5313/VP5513. The device resets to line 64, start of horizontal sync (i.e. line blanking active). There is no on-chip power on reset circuitry.

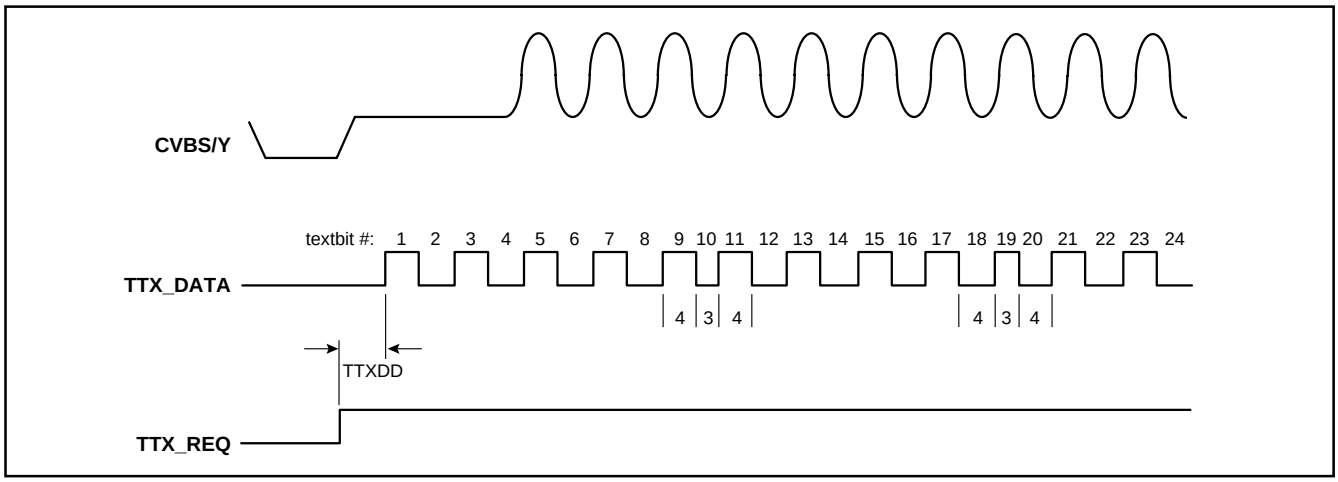



*Figure 4 Teletext timing diagram*

**NCO Adjustment**

| Standard | Lines/ field | Field freq. HZ | Number of pixels/line at 27MHz | Horizontal freq. kHz. $f_H$ | Subcarrier freq. kHz. $f_{SC}$ | $f_{SC}/f_H$ | SC_ADJ register hex | FREQ2-0 registers hex |
|---|---|---|---|---|---|---|---|---|
| NTSC | 525 | 59.94 | 1716 | 15.734266 | 3.57954545 | (455/2) | xx | 87 C1 F1 |
| PAL-B, G, H, I (d) | 625 | 50 | 1728 | 15.625000 | 4.43361875 | (1135/4+1/625) | 9C | A8 26 2B |
| PAL-N (Argentina) | 625 | 50 | 1728 | 15.625000 | 3.58205625 | (917/4+1/625) | 57 | 87 DA 51 |

*Table.2 Line, field and subcarrier standards and register settings*

(d) = default
xx = don't care.

The calculation of the FREQ register value is according to the following formula:-

$$FREQ = 2^{26} \times f_{SC}/PXCK \text{ hex, where PXCK} = 27.00\text{MHz}$$

NTSC value is rounded UP from the decimal number. PAL-B, D, G, H, I and N (Argentina) are rounded DOWN. The SC_ADJ value is derived from the adjustment needed to be added after 8 fields to ensure accuracy of the Subcarrier frequency. Note the SC_ADJ value of 9C required for PAL-B, D, G, H, I.

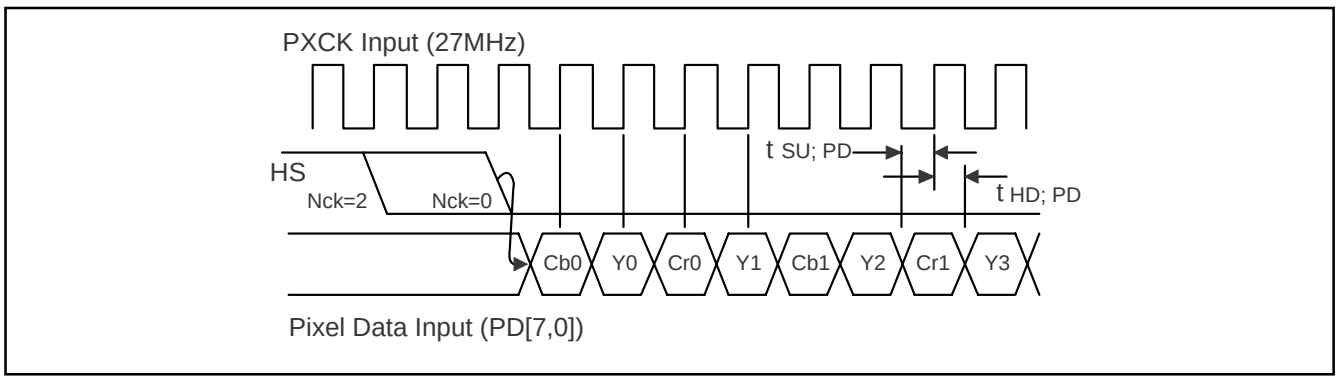



*Figure 5 REC 656 interface with HS output timing*

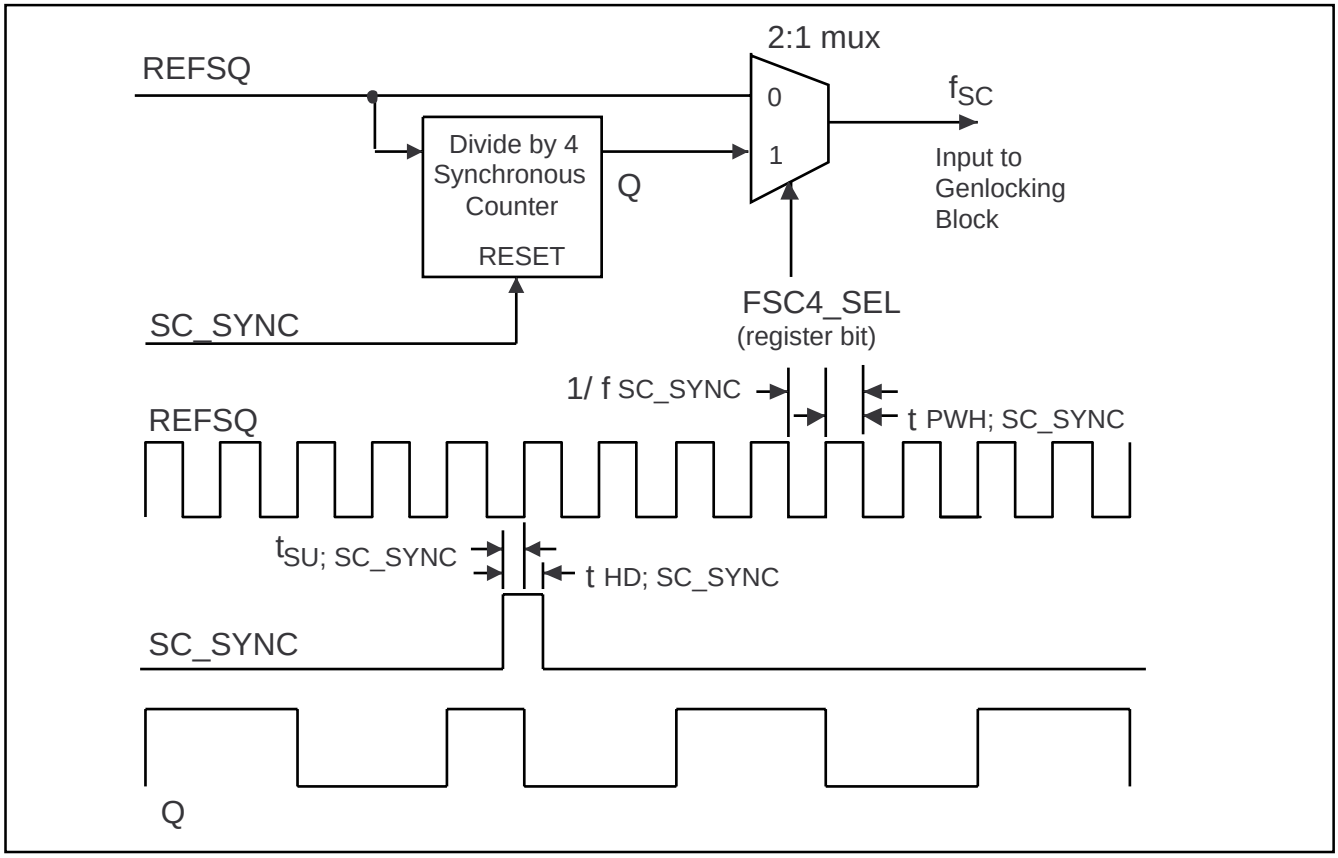



*Figure 6 REFSQ and SC_SYNC input timing*

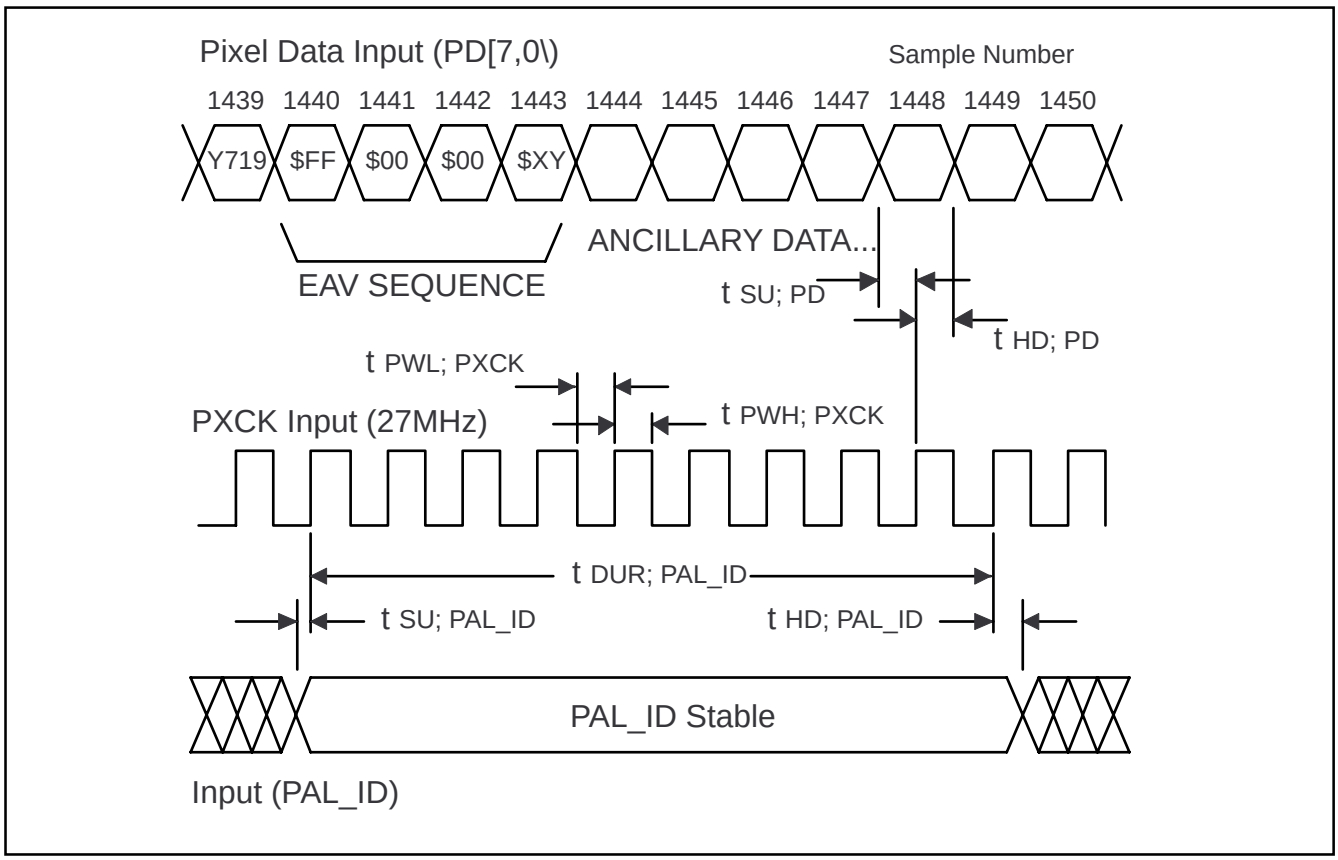



*Figure 7 PAL_ID input timing*

## TIMING INFORMATION

| Parameters | Conditions | Symbol | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| Master clock frequency (PXCK input) | | $f_{PXCK}$ | | 27.0 | | MHz |
| PXCK pulse width, HIGH | | $t_{PWH;\ PXCK}$ | 10 | | | ns |
| PXCK pulse width, LOW | | $t_{PWL;\ PXCK}$ | 14.5 | | | ns |
| PXCK rise time | 10% to 90% points | $t_{RP}$ | | | TBD | ns |
| PXCK fall time | 90% to 10% points | $t_{FP}$ | | | TBD | ns |
| PD7-0 set up time | | $t_{SU;PD}$ | 10 | | | ns |
| PD7-0 hold time | | $t_{HD;PD}$ | 5 | | | ns |
| SCSYNC set up time | | $t_{SU;SC\_SYNC}$ | 10 | | | ns |
| SCSYNC hold time | | $t_{HD;SC\_SYNC}$ | 0 | | | ns |
| PALID set up time | | $t_{SU;PAL\_ID}$ | 10 | | | ns |
| PALID hold time | | $t_{HD;PAL\_ID}$ | 0 | | | ns |
| PALID duration | | $t_{DUR;PAL\_ID}$ | 9 | | | PXCK periods |
| Output delay | PXCK to COMPSYNC<br>PXCK to CLAMP | $t_{DOS}$ | | | 25 | ns |

Note: Timing reference points are at the 50% level. Digital $C_{LOAD}$ <40pF.

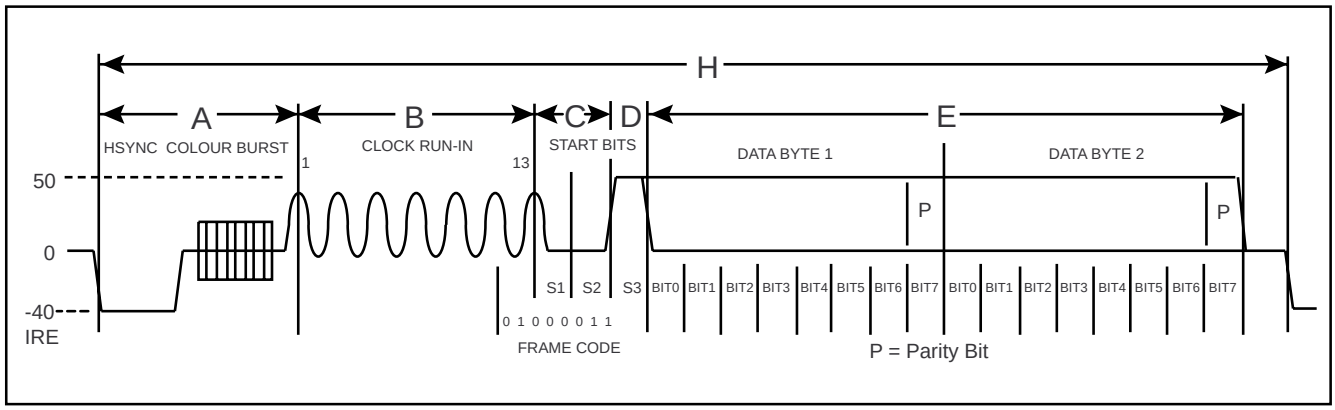



*Figure 8 Closed Capation format*

| Interval | Description | Encoder minimum | Encoder nominal | Encoder maximum |
|---|---|---|---|---|
| A | H-sync to clock run-in | 10.250µs | 10.500µs | 10.750µs |
| B | Clock run-in [2, 3] | | 6.5D (12.910µs) | |
| C | Clock run-in to third start bit [3] | | 2.0D (3.972µs) | |
| D | Data bit [1, 3] | | 1.0D (1.986µs) | |
| E | Data characters [4] | | 16.0D (31.778µs) | |
| H | Horizontal line [1] | | 32.0D (63.556) | |
| | Rise / fall time of data bit transitions [5] | | 0.240µs | 0.288µs |
| | Data bit high (logic level one) [6]<br>Clock run-in maximum | 48 IRE | 50 IRE | 52 IRE |
| | Data bit low (logic level zero) [6]<br>Clock run-in minimum | 0 IRE | 0 IRE | 2 IRE |
| | Data bit differential (high - low)<br>Clock run-in differential (max. - min) | 48 IRE | 50 IRE | 52 IRE |

*Table. 5 Closed Caption data timing. (source EIA R - 4.3 Sept 16 1992)*

Notes

1. The Horizontal line frequency $f_H$ is nominally 15734.26Hz ±0.05Hz. Interval D shall be adjusted to $D = 1/(f_H \times 32)$ for the instantaneous $f_H$ at line 21.
2. The clock run-in signal consists of 7.0 cycles of a 0.5034965MHz (1/D) sine wave when measured from the leading to trailing 0 IRE points. The sine wave is to be symmetrical about the 25 IRE level.
3. The negative going midpoints (half amplitude) of the clock run-in shall be coherent with the midpoints (half amplitude) of the Start and Data bit transitions.
4. Two characters, each consisting of 7 data bits and 1 odd parity bit.
5. 2 T Bar, measured between the 10% and 90% amplitude points.
6. The clock run-in maximum level shall not differ from the data bit high level by more than ±1 IRE. The clock run-in minimum level shall not differ from the data bit low level by more than ±1 IRE.

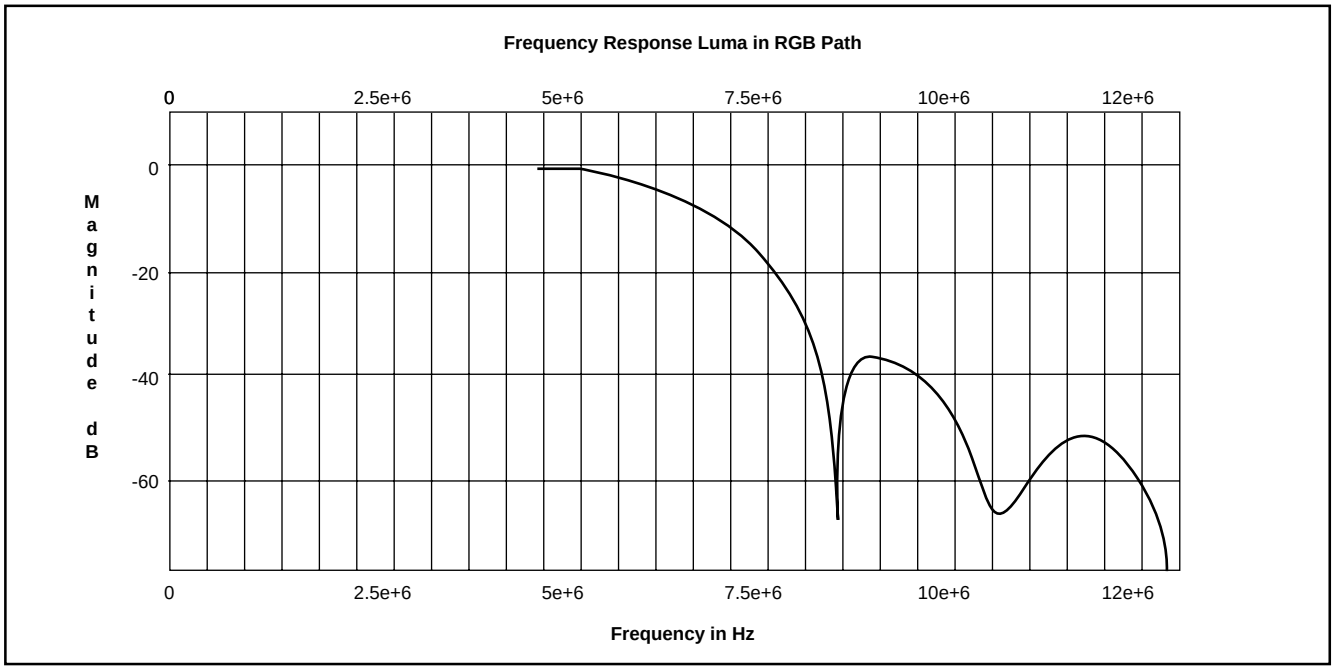



*Figure 9 Luma filter for RGB datapath*

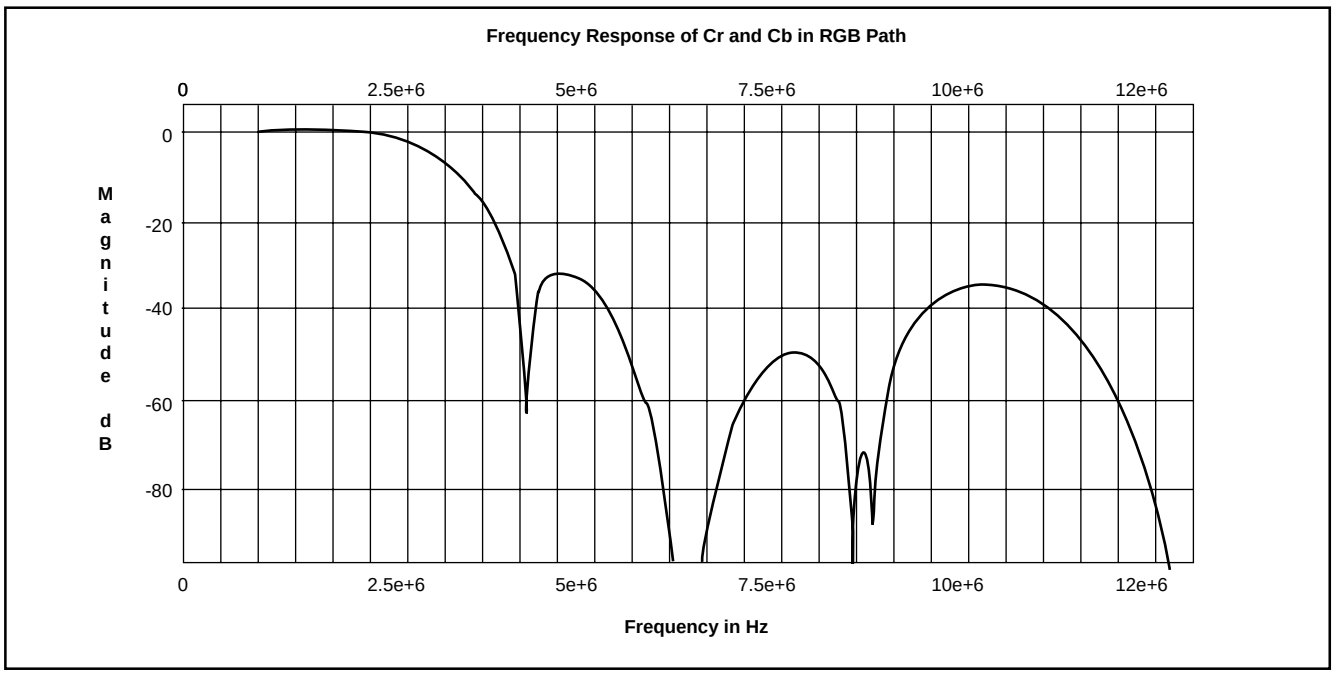



*Figure 10 Chroma filter for RGB datapath*

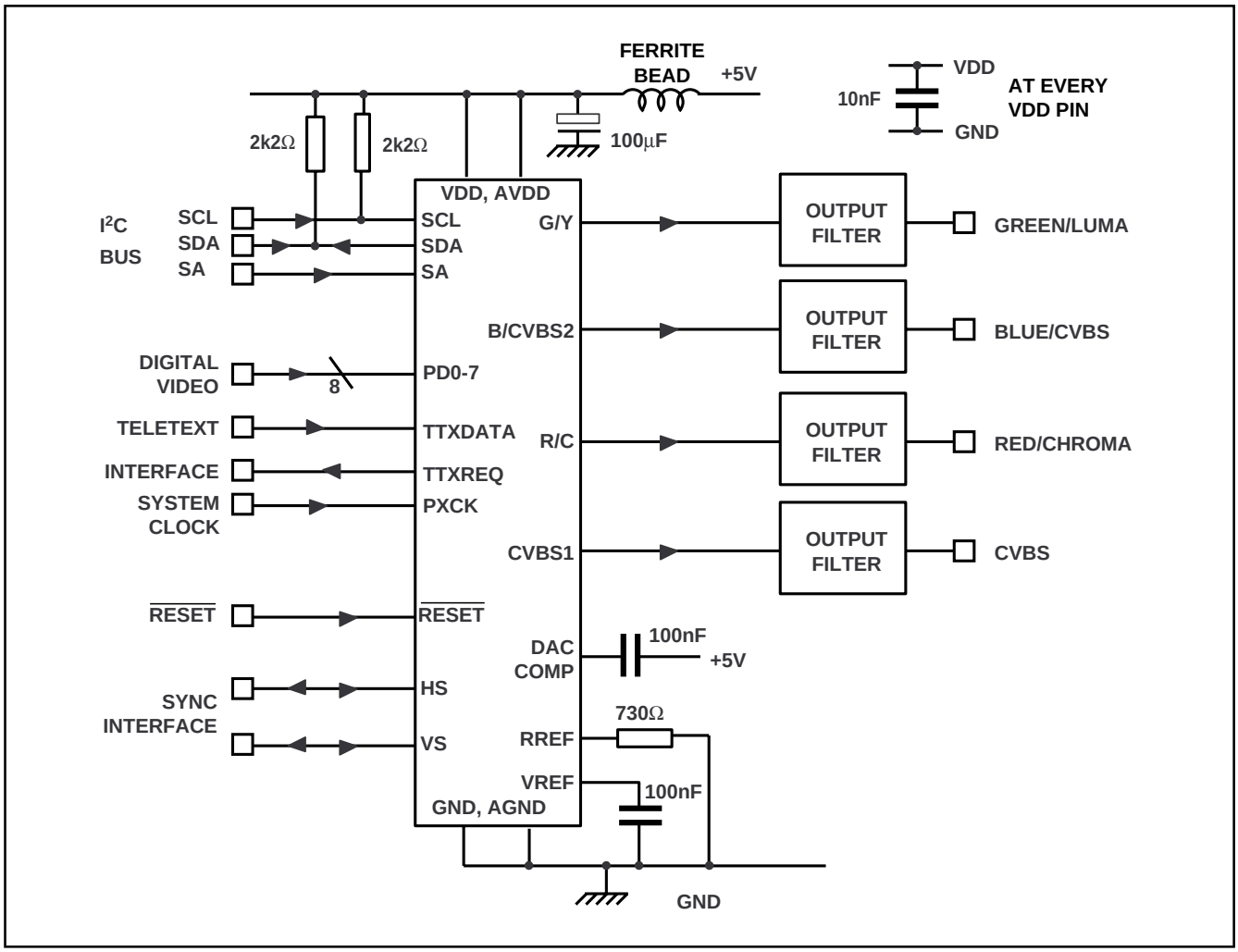



*Figure 11 Typical application diagram. (Output filter - see Fig.12) to drive 37.5ohms*

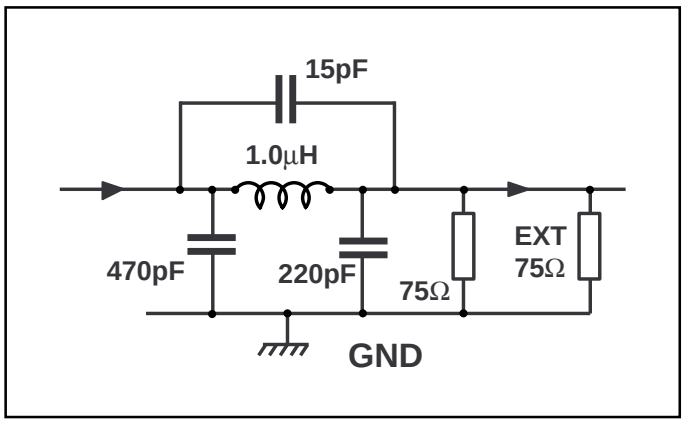



*Figure 12 Output reconstruction filter*

**Note:**
The VP5313 is only available to customers with a valid and existing authorisation to purchase issued by MACROVISION CORPORATION.

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