TC74HC563AP/AF
TC74HC573AP/AF/AFW

OCTAL D-TYPE LATCH WITH 3-STATE OUTPUT

TC74HC563AP/AF INVERTING
TC74HC573AP/AF/AFW NON-INVERTING

The TC74HC563A and TC74HC573A are high speed CMOS OCTAL LATCH with 3-STATE OUTPUT fabricated with silicon gate C^2MOS technology.

They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

These 8-bit D-type latches are controlled by a latch enable input (LE) and a output enable input($\overline{OE}$).

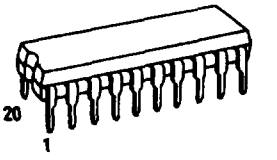
When the $\overline{OE}$ input is high, the eight outputs are in a high impedance state.

The TC74HC563A has inverting outputs, and TC74HC573A has non-inverting outputs.

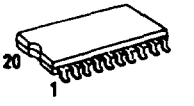
All inputs are equipped with protection circuits against static dischage or transient excess voltage.

FEATURES:

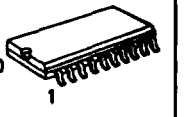
- High Speed ····· t_{pd} =13ns(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC} (Min.)
- Output Drive Capability ····· 15 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=6mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC} (opr.)=2V~6V
- Pin and Function Compatible with 74LS563/573



P(DIP20-P-300A)



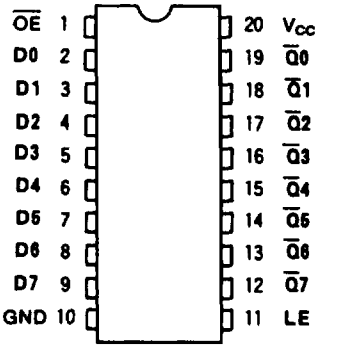
F(SOP20-P-300)



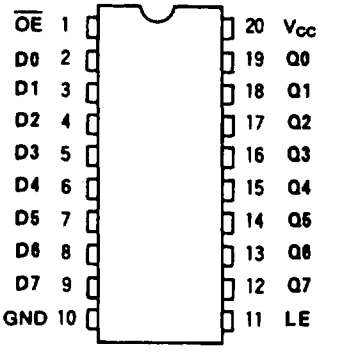
FW(SOL20-P-300)

PIN ASSIGNMENT

TC74HC563A



TC74HC573A

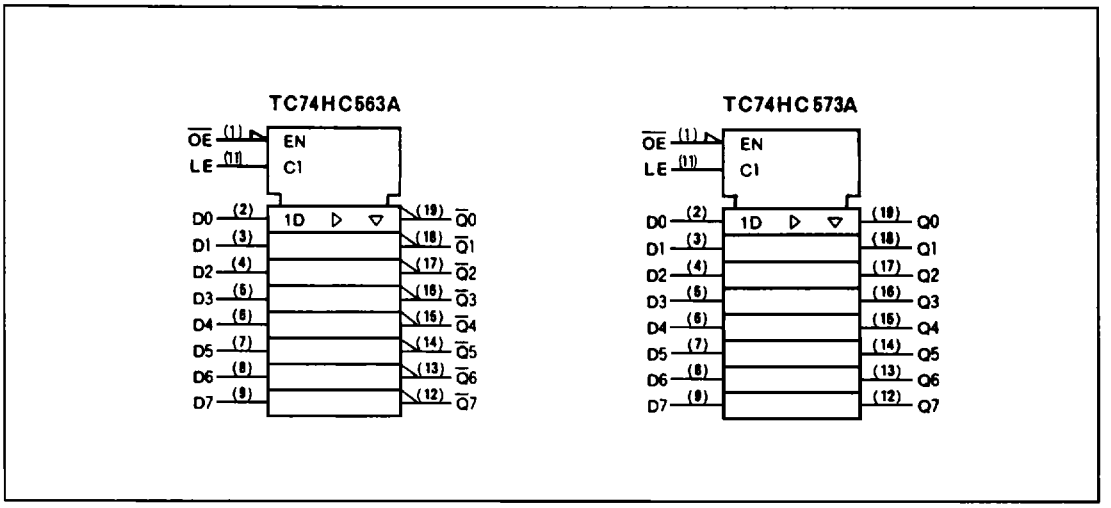


TRUTH TABLE

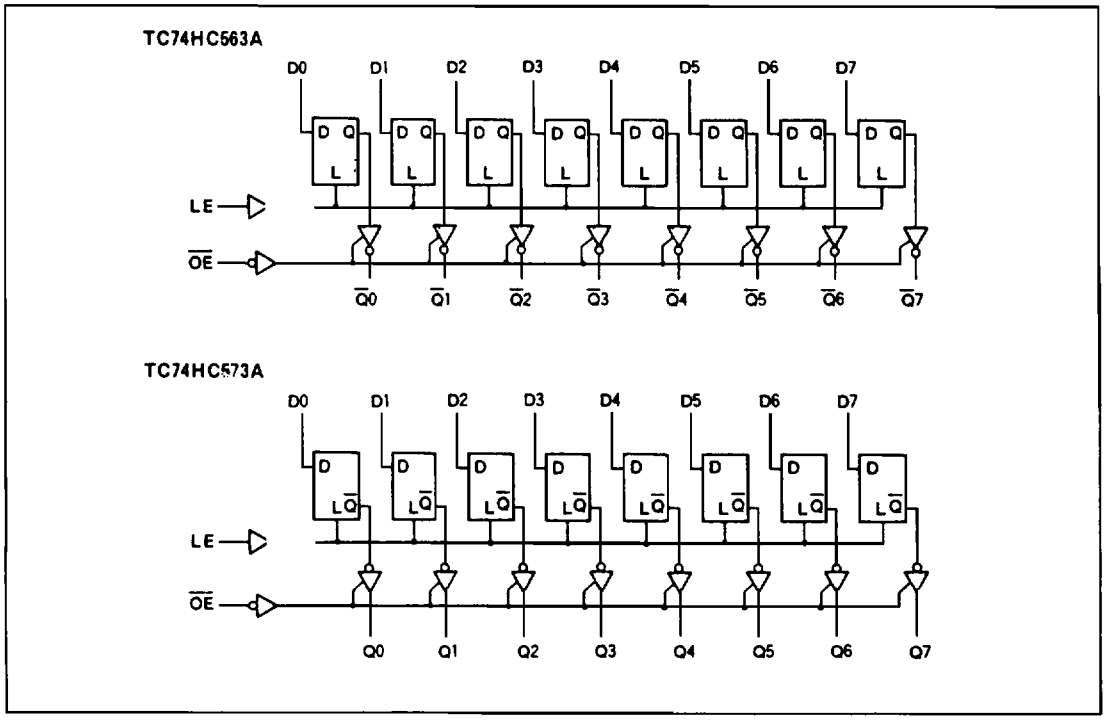
INPUTS			OUTPUTS	
$\overline{OE}$	LE	D	Q(HC573A)	$\overline{Q}$(HC563A)
H	X	X	Z	Z
L	L	X	Q_n	$\overline{Q_n}$
L	H	L	L	H
L	H	H	H	L

X : Don't Care
Z : High Impedance
$Q_n(\overline{Q_n})$: Q($\overline{Q}$) outputs are latched at the time when the LE input is taken to a low logic level.

IEC LOGIC SYMBOL



SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±75	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−6 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−7.8mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =6 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =7.8mA	6.0	−	0.18	0.26	−	0.33	
3−State Output Off−State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		6.0	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

TIMING REQUIREMENTS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40 ~85℃ LIMIT	UNIT
Minimum Pulse Width (LE)	$t_{W(H)}$		2.0	−	75	95	ns
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set−up Time (Data)	t_s		2.0	−	50	65	
			4.5	−	10	13	
			6.0	−	9	11	
Minimum Hold Time (Data)	t_h		2.0	−	5	5	
			4.5	−	5	5	
			6.0	−	5	5	

AC ELECTRICAL CHARACTERISTICS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	CL	V_{CC}	Ta=25℃ MIN.	TYP.	MAX.	Ta=−40 ~85℃ MIN.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		50	2.0	−	20	60	−	75	ns
				4.5	−	6	12	−	15	
				6.0	−	5	10	−	13	
Propagation Delay Time (LE−Q, $\overline{Q}$)	t_{pLH}		50	2.0	−	50	115	−	145	
				4.5	−	15	23	−	29	
				6.0	−	13	20	−	25	
	t_{pHL}		150	2.0	−	60	155	−	195	
				4.5	−	20	31	−	39	
				6.0	−	17	26	−	33	
Propagation Delay Time (D−Q, $\overline{Q}$)	t_{pLH}		50	2.0	−	42	110	−	140	
				4.5	−	14	22	−	28	
				6.0	−	12	19	−	24	
	t_{pHL}		150	2.0	−	57	150	−	190	
				4.5	−	19	30	−	38	
				6.0	−	16	26	−	32	
Output Enable time	t_{pZL}	$R_L=1\,k\Omega$	50	2.0	−	55	140	−	175	
				4.5	−	17	28	−	35	
				6.0	−	14	24	−	30	
	t_{pZH}		150	2.0	−	66	180	−	225	
				4.5	−	22	36	−	45	
				6.0	−	19	31	−	38	
Output Disable time	t_{pLZ} t_{pHZ}	$R_L=1\,k\Omega$	50	2.0	−	40	125	−	155	
				4.5	−	17	25	−	31	
				6.0	−	15	21	−	26	
Input Capacitance	C_{IN}				−	5	10	−	10	pF
Output Capacitance	C_{OUT}				−	10	−	−	−	
Power Dissipation Capacitance	C_{PD}(1)	TC74HC563A			−	49	−	−	−	
		TC74HC573A			−	51	−	−	−	

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{(per Latch)}$$

And the total C_{PD} when n pcs. of Latch operate can be gained by the following equation:

$C_{PD}(total)=33+16 \cdot n$ (TC74HC563A)
$C_{PD}(total)=33+18 \cdot n$ (TC74HC573A)