

FEATURES

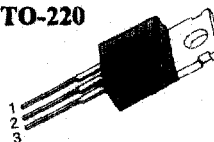
- Avalanche Rugged Technology
- Rugged Gate Oxide Technology
- Lower Input Capacitance
- Improved Gate Charge
- Extended Safe Operating Area
- 175°C Operating Temperature
- Lower Leakage Current : 10 μ A (Max.) @ $V_{DS} = 100V$
- Lower $R_{DS(ON)}$: 0.032 Ω (Typ.)

$$BV_{DSS} = 100 V$$

$$R_{DS(on)} = 0.04 \Omega$$

$$I_D = 40 A$$

TO-220



1.Gate 2. Drain 3. Source

Absolute Maximum Ratings

Symbol	Characteristic	Value	Units
V_{DSS}	Drain-to-Source Voltage	100	V
I_D	Continuous Drain Current ($T_C=25^\circ\text{C}$)	40	A
	Continuous Drain Current ($T_C=100^\circ\text{C}$)	28.3	
I_{DM}	Drain Current-Pulsed ①	160	A
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulsed Avalanche Energy ②	640	mJ
I_{AR}	Avalanche Current ①	40	A
E_{AR}	Repetitive Avalanche Energy ①	16.7	mJ
dv/dt	Peak Diode Recovery dv/dt ③	6.5	V/ns
P_D	Total Power Dissipation ($T_C=25^\circ\text{C}$)	167	W
	Linear Derating Factor	1.11	W/°C
T_J, T_{STG}	Operating Junction and Storage Temperature Range	- 55 to +175	°C
T_L	Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5-seconds	300	

Thermal Resistance

Symbol	Characteristic	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.9	°C/W
$R_{\theta CS}$	Case-to-Sink	0.5	—	
$R_{\theta JA}$	Junction-to-Ambient	—	62.5	

Electrical Characteristics ($T_C=25^\circ\text{C}$ unless otherwise specified)

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
BV_{DSS}	Drain-Source Breakdown Voltage	100	—	—	V	$V_{GS}=0V, I_D=250\mu A$
$\Delta BV/\Delta T_J$	Breakdown Voltage Temp. Coeff.	—	0.11	—	V/°C	$I_D=250\mu A$ See Fig 7
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS}=5V, I_D=250\mu A$
I_{GSS}	Gate-Source Leakage, Forward	—	—	100	nA	$V_{GS}=20V$
	Gate-Source Leakage, Reverse	—	—	-100	nA	$V_{GS}=-20V$
I_{DSS}	Drain-to-Source Leakage Current	—	—	10	μA	$V_{DS}=100V$
		—	—	100		$V_{DS}=80V, T_C=150^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-State Resistance	—	—	0.04	Ω	$V_{GS}=10V, I_D=20A$ ④
g_{fs}	Forward Transconductance	—	27.44	—	S	$V_{DS}=40V, I_D=20A$ ④
C_{iss}	Input Capacitance	—	1750	2270	pF	$V_{GS}=0V, V_{DS}=25V, f=1\text{MHz}$ See Fig 5
C_{oss}	Output Capacitance	—	420	485		
C_{rss}	Reverse Transfer Capacitance	—	185	215		
$t_{d(on)}$	Turn-On Delay Time	—	17	50	ns	$V_{DD}=50V, I_D=40A,$ $R_G=6.2\Omega$ See Fig 13 ④ ⑤
t_r	Rise Time	—	20	50		
$t_{d(off)}$	Turn-Off Delay Time	—	80	160		
t_f	Fall Time	—	45	100		
Q_g	Total Gate Charge	—	75	97	nC	$V_{DS}=80V, V_{GS}=10V,$ $I_D=40A$ See Fig 6 & Fig 12 ④ ⑤
Q_{gs}	Gate-Source Charge	—	13.2	—		
Q_{gd}	Gate-Drain("Miller") Charge	—	34.8	—		

Source-Drain Diode Ratings and Characteristics

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
I_S	Continuous Source Current	—	—	40	A	Integral reverse pn-diode in the MOSFET
I_{SM}	Pulsed-Source Current ①	—	—	160		
V_{SD}	Diode Forward Voltage ④	—	—	1.6	V	$T_J=25^\circ\text{C}, I_S=40A, V_{GS}=0V$
t_{rr}	Reverse Recovery Time	—	135	—	ns	$T_J=25^\circ\text{C}, I_F=40A$
Q_{rr}	Reverse Recovery Charge	—	0.65	—	μC	$di/dt=100A/\mu s$ ④

Notes :

- ① Repetitive Rating : Pulse Width Limited by Maximum Junction Temperature
- ② $L=0.6mH, I_{AS}=40A, V_{DD}=25V, R_G=27\Omega$, Starting $T_J=25^\circ\text{C}$
- ③ $I_{SD} \leq 40A, di/dt \leq 470A/\mu s, V_{DD} \leq BV_{DSS}$, Starting $T_J=25^\circ\text{C}$
- ④ Pulse Test : Pulse Width = $250\mu s$, Duty Cycle $\leq 2\%$
- ⑤ Essentially Independent of Operating Temperature

Fig 1. Output Characteristics

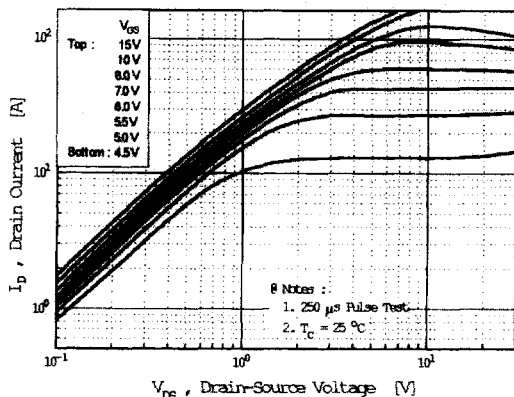


Fig 2. Transfer Characteristics

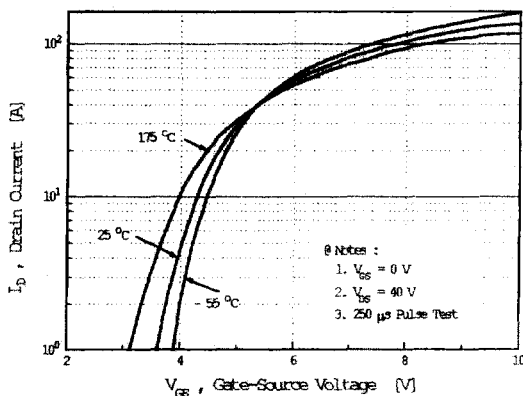


Fig 3. On-Resistance vs. Drain Current

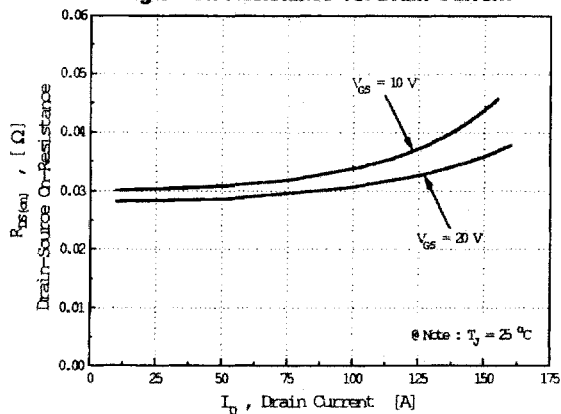


Fig 4. Source-Drain Diode Forward Voltage

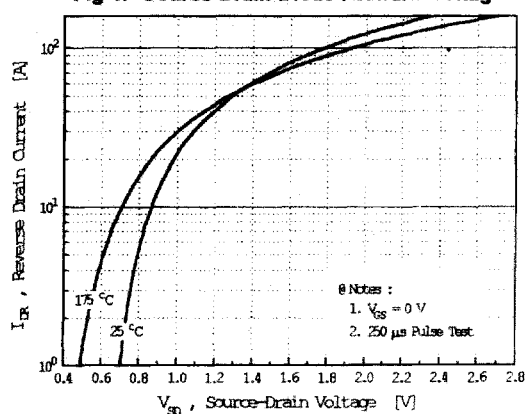


Fig 5. Capacitance vs. Drain-Source Voltage

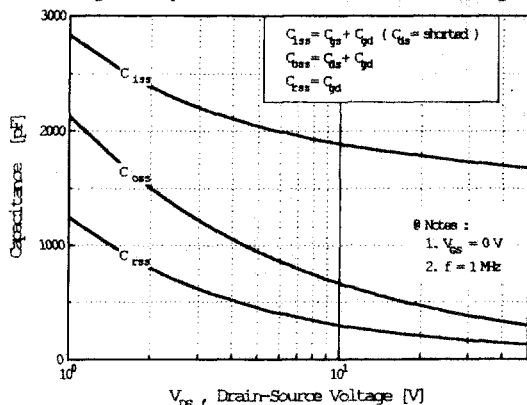


Fig 6. Gate Charge vs. Gate-Source Voltage

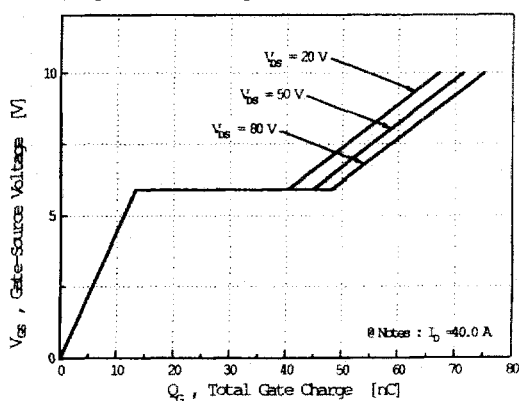


Fig 7. Breakdown Voltage vs. Temperature

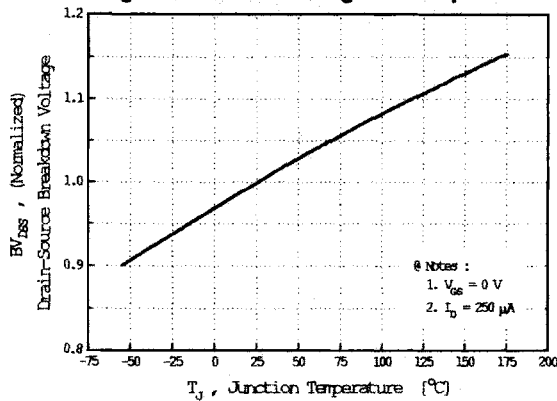


Fig 8. On-Resistance vs. Temperature

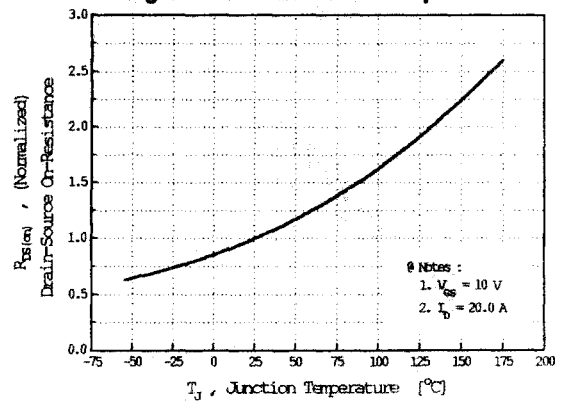


Fig 9. Max. Safe Operating Area

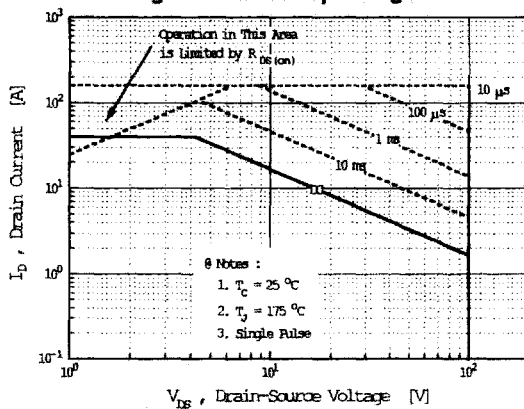


Fig 10. Max. Drain Current vs. Case Temperature

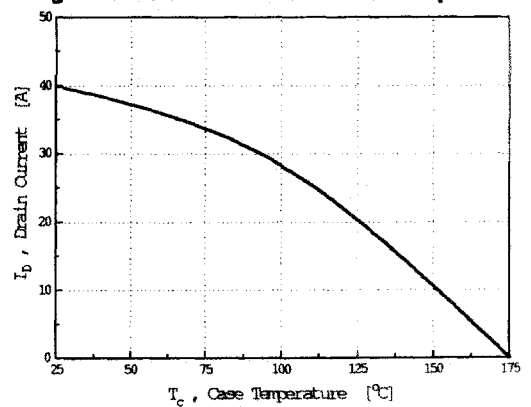


Fig 11. Thermal Response

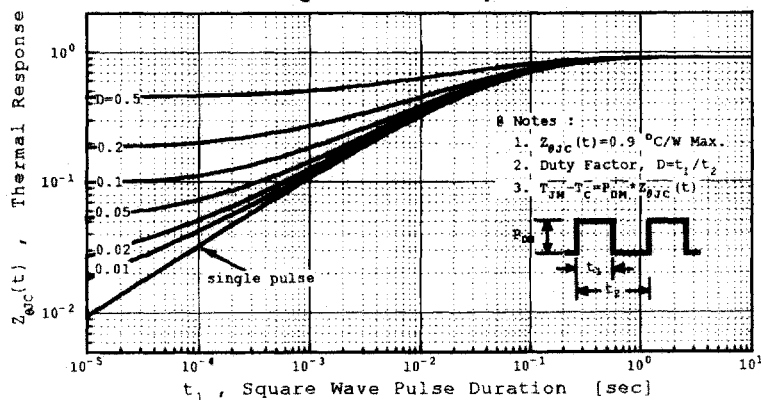


Fig 12. Gate Charge Test Circuit & Waveform

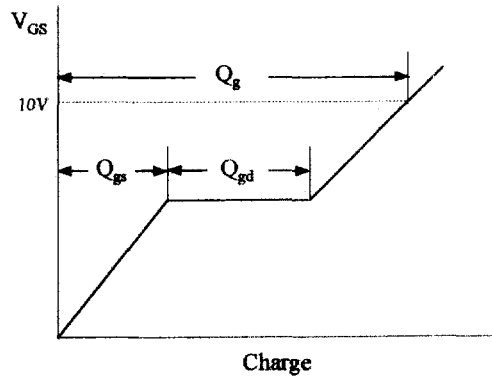
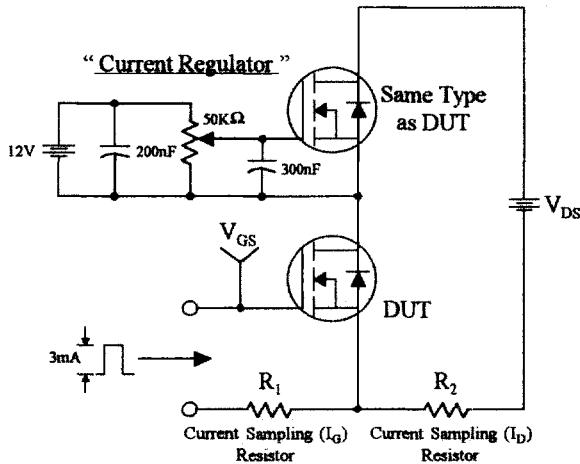


Fig 13. Resistive Switching Test Circuit & Waveforms

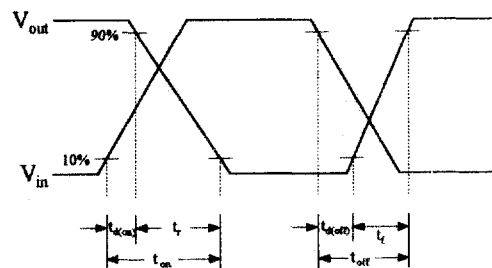
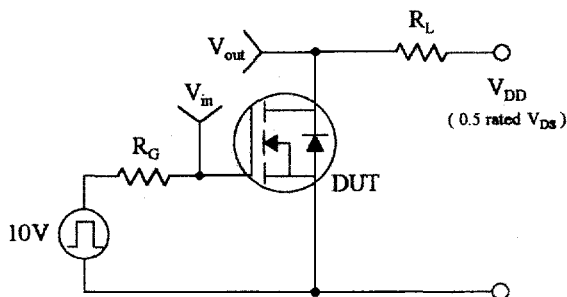


Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms

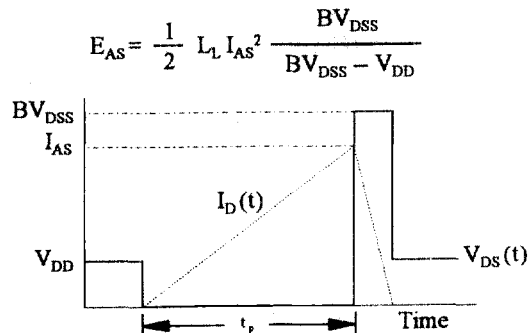
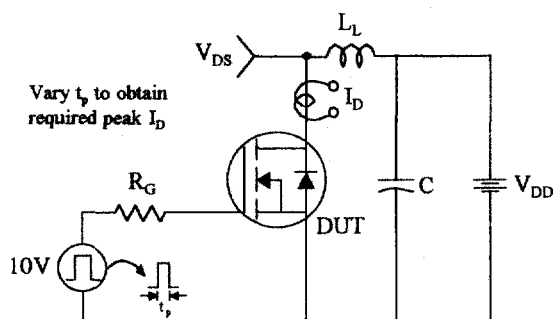


Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

