

HM50464 Series

65536-word x 4-bit Dynamic Random Access Memory

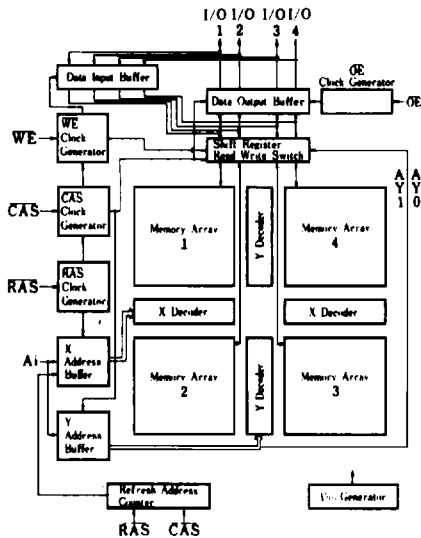
■ FEATURES

- Page mode capability
- Single 5V ($\pm 10\%$)
- On chip substrate bias generator
- Low power: 350 mW active, 20 mW standby
- High speed: Access Time 120ns/150ns/200ns
- Output data controlled by CAS or OE
- TTL compatible
- 256 refresh cycles 4 ms
- 3 variations of refresh RAS only refresh
CAS before RAS refresh
Hidden refresh

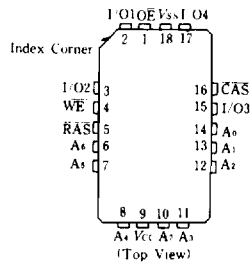
■ ORDERING INFORMATION

Type No.	Access Time	Package
HM50464P-12	120ns	300 mil 18 pin Plastic DIP
HM50464P-15	150ns	
HM50464P-20	200ns	
HM50464CP-12	120ns	18 pin PLCC
HM50464CP-15	150ns	
HM50464CP-20	200ns	

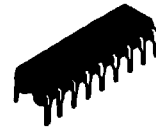
■ BLOCK DIAGRAM



● HM50464CP Series



HM50464P Series



(DP-18B)

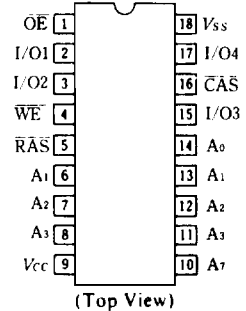
HM50464CP Series



(CP-18)

■ PIN ARRANGEMENT

● HM50464P Series



A ₀ - A ₇	Address Inputs
CAS	Column Address Strobe
I/O1 - I/O4	Data In/Data Out
OE	Output Enable
RAS	Row Address Strobe
WE	Read/Write Input
V _{CC}	Power (+5V)
V _{SS}	Ground
A ₈ - A ₁₅ (Row)	Refresh Address Inputs



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■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	V_T	-1 to +7	V
Supply Voltage relative to V_{SS}	V_{CC}	-1 to +7	V
Operating Temperature (Ambient)	T_{opr}	0 to +70	°C
Storage Temperature (Ambient)	T_{stg}	-55 to +125	°C
Power Dissipation	P_T	1.0	W
Short Circuit Output Current	I_{out}	50	mA

■ RECOMMENDED DC OPERATING CONDITION ($T_a = 0$ to +70°C)

Parameter	Symbol	min.	typ.	max.	unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.4	—	6.5	V
Input Low Voltage	V_{IL}	-1.0	—	0.8	V

Note) All voltage referenced to V_{SS} .

■ DC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, $T_a = 0$ to +70°C)

Parameter	Symbol	HM50464-12		HM50464-15		HM50464-20		Unit	Note
		min.	max.	min.	max.	min.	max.		
Operating Current ($I_{RC} = \text{min.}$)	I_{CC1}	—	83	—	70	—	55	mA	1
Standby Current ($RAS = V_{IH}$, Dout = Disable)	I_{CC2}	—	4.5	—	4.5	—	4.5	mA	
Refresh Current (RAS only refresh, $I_{RC} = \text{min.}$)	I_{CC3}	—	62	—	53	—	42	mA	
Standby Current ($RAS = V_{IH}$, Dout = Enable)	I_{CC5}	—	10	—	10	—	10	mA	1
Refresh Current (CAS before RAS refresh, $I_{RC} = \text{min.}$)	I_{CC6}	—	69	—	58	—	45	mA	1
Operating Current (Page mode, $I_{PC} = \text{min.}$)	I_{CC7}	—	57	—	48	—	37	mA	1
Input Leakage Current ($0 < V_{in} < 7V$)	I_{LI}	-10	10	-10	10	-10	10	μA	
Output Leakage Current ($0 < V_{out} < 7V$, Dout = Disable)	I_{LO}	-10	10	-10	10	-10	10	μA	
Output High Voltage ($I_{out} = -5 \text{ mA}$)	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output Low Voltage ($I_{out} = 4.2 \text{ mA}$)	V_{OL}	0	0.4	0	0.4	0	0.4	V	

Note) 1. I_{CC} depends on output loading condition when the device is selected, I_{CC} max. is specified at the output open condition.

■ CAPACITANCE ($V_{CC} = 5V \pm 10\%$, $T_a = 25^\circ C$)

Parameter	Symbol	typ.	max.	Unit	Note
Input Capacitance	Address	C_{I1}	5	pF	1
	RAS , CAS , WE , OE	C_{I2}	10	pF	1
Output Capacitance	Data In/Data Out	$C_{I/O}$	10	pF	1, 2

Notes) 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.

2. $CAS = V_{IH}$ to disable Dout.

■ ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

($V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, $T_a = 0$ to +70°C)

Parameter	Symbol	HM50464-12		HM50464-15		HM50464-20		Unit	Note
		min.	max.	min.	max.	min.	max.		
Access Time from RAS	t_{RAC}	—	120	—	150	—	200	ns	2, 3
Access Time from CAS	t_{CAC}	—	60	—	75	—	100	ns	3, 4
Output Buffer Turn-off Delay referenced to CAS	t_{OFF1}	—	30	—	40	—	50	ns	5
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	6
Random Read or Write Cycle Time	t_{RC}	220	—	260	—	330	—	ns	
RAS Precharge Time	t_{RP}	90	—	100	—	120	—	ns	
RAS Pulse Width	t_{RAS}	120	10000	150	10000	200	10000	ns	
CAS Pulse Width	t_{CAS}	60	10000	75	10000	100	10000	ns	
RAS to CAS Delay Time	t_{RCD}	25	60	25	75	30	100	ns	7
RAS Hold Time	t_{RSH}	60	—	75	—	100	—	ns	
CAS Hold Time	t_{CSH}	120	—	150	—	200	—	ns	
CAS to RAS Precharge Time	t_{CRP}	10	—	10	—	10	—	ns	
Row Address Set-up Time	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	15	—	15	—	20	—	ns	

(to be continued)



Parameter	Symbol	HM50464-12		HM50464-15		HM50464-20		Unit	Note
		min.	max.	min.	max.	min.	max.		
Column Address Set-up Time	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	20	—	25	—	30	—	ns	
Column Address Hold Time referenced to $\overline{RAS}$	t_{AR}	80	—	100	—	130	—	ns	
Write Command Set-up Time	t_{WCS}	0	—	0	—	0	—	ns	8
Write Command Hold Time	t_{WCH}	40	—	45	—	55	—	ns	
Write Command Hold Time referenced to $\overline{RAS}$	t_{WCR}	100	—	120	—	155	—	ns	
Write Command Pulse Width	t_{WP}	40	—	45	—	55	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{RWL}	40	—	45	—	55	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	40	—	45	—	55	—	ns	
Data-in Set-up Time	t_{DS}	0	—	0	—	0	—	ns	9
Data-in Hold Time	t_{DH}	40	—	45	—	55	—	ns	9
Data-in Hold Time referenced to $\overline{RAS}$	t_{DHR}	100	—	120	—	155	—	ns	
Read Command Set-up Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time referenced to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	ns	
Read Command Hold Time referenced to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	ns	
Refresh Period	t_{REF}	—	4	—	4	—	4	ms	
Read-Write Cycle Time	t_{RWC}	305	—	360	—	450	—	ns	
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	100	—	125	—	160	—	ns	8
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	160	—	200	—	260	—	ns	8
$\overline{CAS}$ Precharge Time	t_{CPN}	50	—	60	—	80	—	ns	
$\overline{CAS}$ Set-up Time ($\overline{CAS}$ before $\overline{RAS}$ refresh)	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ refresh)	t_{CHR}	120	—	150	—	200	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	0	—	0	—	0	—	ns	
Access Time from $\overline{OE}$	t_{OAC}	—	30	—	35	—	45	ns	
Output Buffer Turn-off Delay referenced to $\overline{OE}$	t_{OFF2}	—	30	—	40	—	50	ns	
$\overline{OE}$ to Data-in Delay Time	t_{ODD}	30	—	40	—	50	—	ns	
$\overline{OE}$ Hold Time referenced to $\overline{WE}$	t_{OEH}	25	—	30	—	40	—	ns	
Page Mode Cycle Time	t_{PC}	120	—	145	—	190	—	ns	
$\overline{CAS}$ Precharge Time (for Page-mode Cycle Only)	t_{CP}	50	—	60	—	80	—	ns	
$\overline{CAS}$ Read-modify-write Cycle Time (Page-mode)	t_{PCM}	205	—	245	—	310	—	ns	

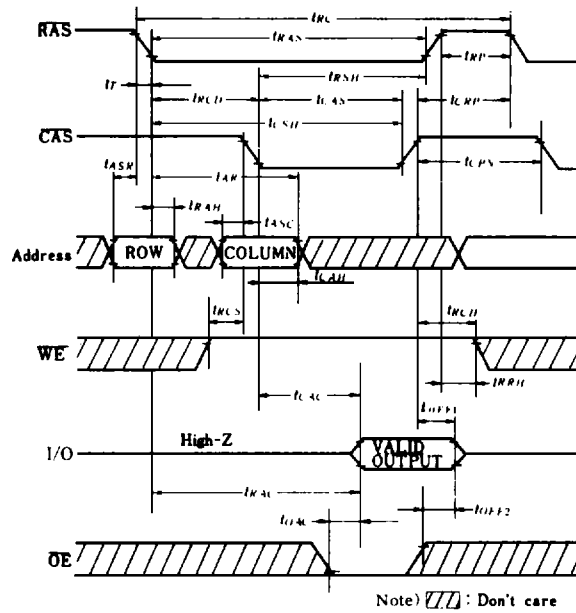
Notes)

1. AC measurements assume $t_T = 5\text{ns}$.
2. Assume that $t_{RCD} \leq t_{RCD}(\text{max})$. If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
4. Assumes that $t_{RCD} \geq t_{RCD}(\text{max})$.
5. $t_{OFF}(\text{max})$ is defined as the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} .
7. Operation with the $t_{RCD}(\text{max})$ limit insures that $t_{RAC}(\text{max})$ can be met; $t_{RCD}(\text{max})$ is specified as a reference point only, if t_{RCD} is greater than the specified $t_{RCD}(\text{max})$ limit, then access time is controlled exclusively by t_{CAC} .
8. t_{WCS} , t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}(\text{min})$, the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}(\text{min})$ and $t_{RWD} \geq t_{RWD}(\text{min})$, the cycle is a read/write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
9. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
10. An initial pause of 100 μs is required after power-up followed by a minimum of 8 initialization of cycles.
11. Minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh is required before using internal refresh counter.
12. In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffers prior to applying data to the device.

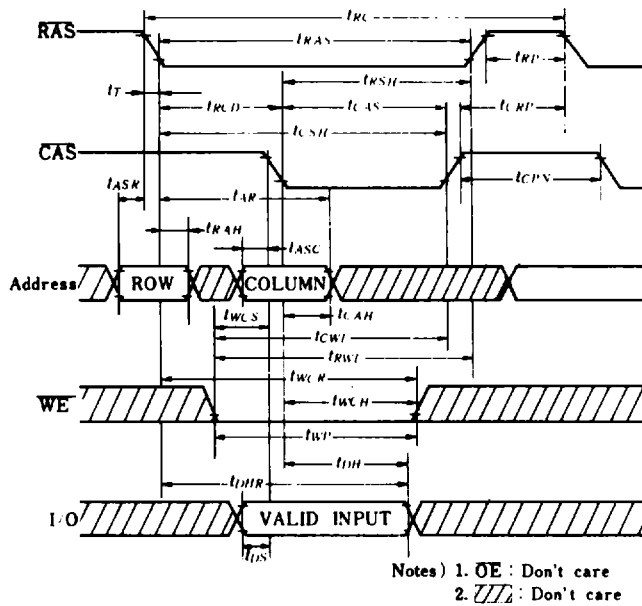


■ TIMING WAVEFORMS

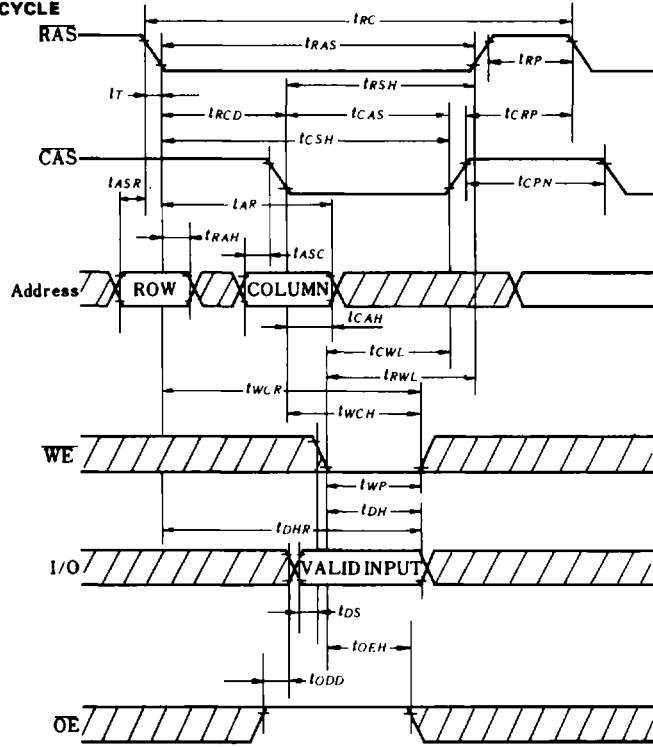
● READ CYCLE



● EARLY WRITE CYCLE

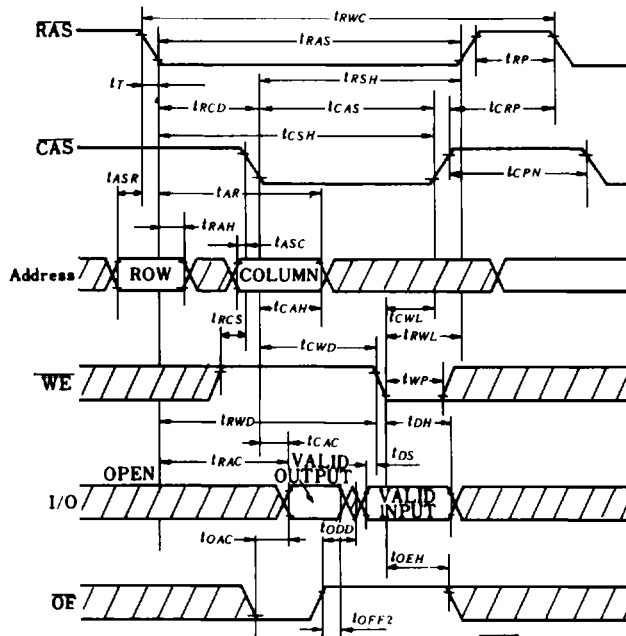


• DELAYED WRITE CYCLE



Note) : Don't care

• READ MODIFY WRITE CYCLE

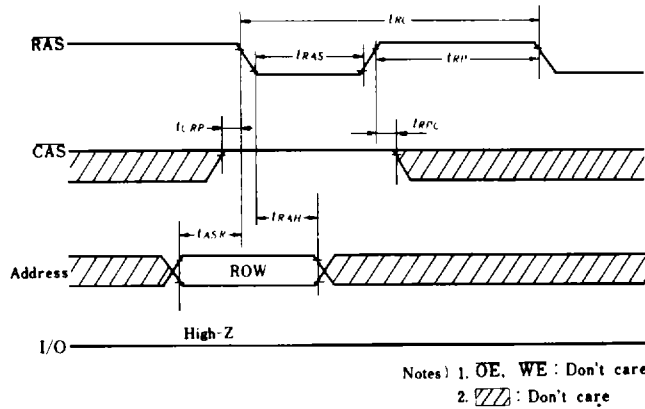


Note) : Don't care

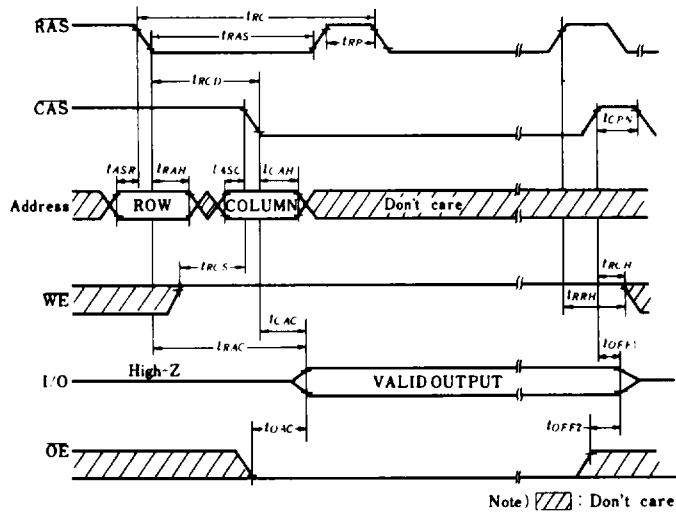


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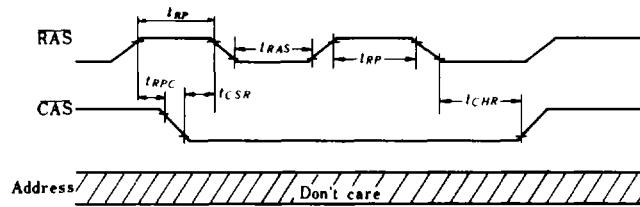
• **RAS ONLY REFRESH CYCLE**



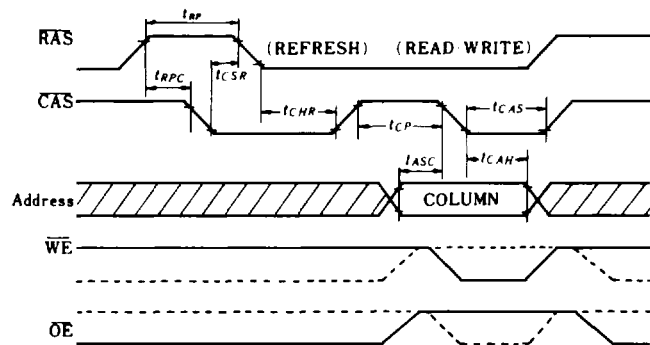
• **HIDDEN REFRESH CYCLE**



• CAS BEFORE RAS REFRESH CYCLE

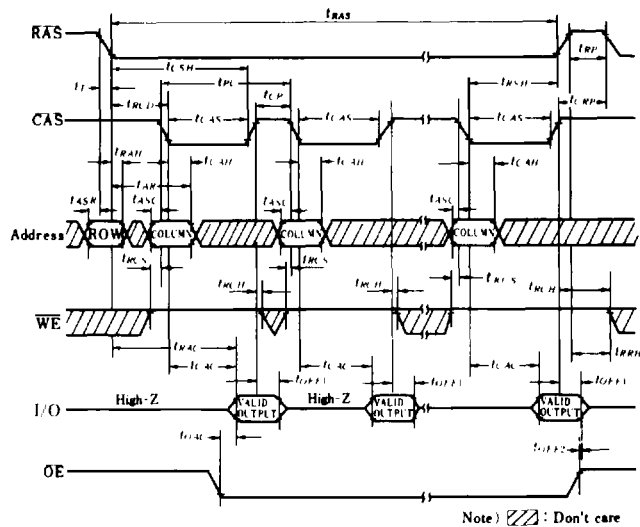


• COUNTER TEST



Notes) 1. Dotted-line Means Read Cycle. 2. : Don't care

• PAGE MODE READ CYCLE



Note) : Don't care



