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| Doc. Version | 0.3 |
| Total Page | 29 |
| Date | 2006/11/15 |

Product Specification

6.5" COLOR TFT-LCD MODULE

MODEL NAME: A065VL01 V2

< □ > Preliminary Specification

< > Final Specification

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1. Summary

A065VL01 V2 is a LTPS (Low Temperature Poly-Silicon) type TFT (Thin Film Transistor) LCD (Liquid crystal Display) with touch panel. This model is composed of TFT-LCD, drive IC, FPC (flexible printed circuit), backlight unit and touch panel.

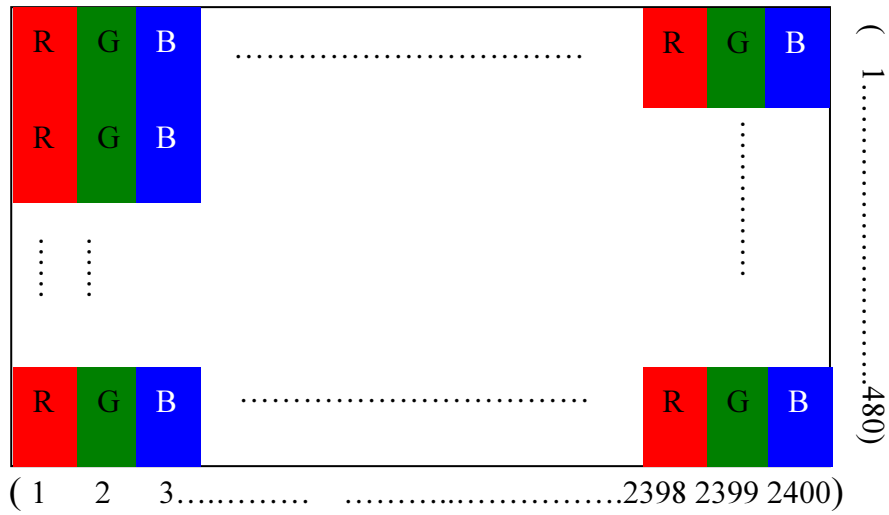
2. Features

- 6.5" display size in 16:9 aspect ratio
- 800RGBx480(WVGA) resolution for wide view format
- 250nits high brightness with high power LED backlight
- 250:1 high contrast
- Wide viewing angle technology
- Power supply: 3.3V for LCD panel and 13.2V for LED
- Parallel RGB I/F of 6-bit color depth
- Green design

3. Physical Specifications

| NO. | Item | Specification | Remark |
|-----|-------------------------|-----------------------------|--------|
| 1 | Display resolution(dot) | 800 (W)×RGBx480 (H) | |
| 2 | Active area(mm) | 143.4(W)×79.2(H) | |
| 3 | Screen size(inch) | 6.5"(Diagonal) | |
| 4 | Display Mode | Normally White | |
| 5 | Pixel pitch(mm) | 0.0597(W)×RGB×0.165 (H) | |
| 6 | Color configuration | R. G. B. stripe | Note 1 |
| 7 | Color Depth | 262K Colors | Note 2 |
| 8 | Overall dimension(mm) | 157.2(W)×89.2(H)×6.4(D) | Note 3 |
| 9 | Weight(g) | 145±5% | |
| 10 | Surface treatment | AG(8% haze) & with SWV film | |
| 11 | Backlight unit | High power LEDs | |

Note 1: Below figure shows the dot stripe arrangement.



Note 2: The 262K color display depends on 6-bit data signal input.

Note 3: Not including the backlight cable and screw height. Refer to next page for further information.

4. Electrical Specifications

a. Pin Assignment

Connector type: FH16-80S-0.3SH(05) or compatible

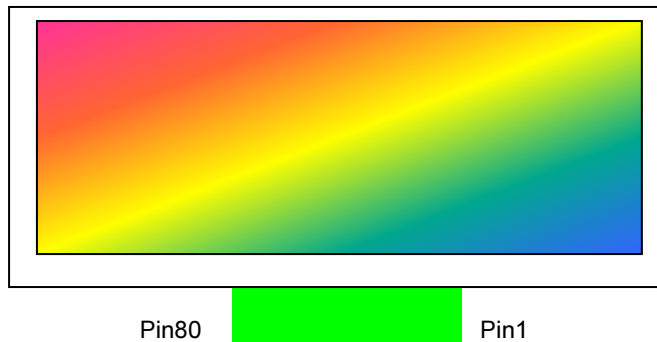
| Pin no | Symbol | I/O | Description | Remark |
|--------|--------|-----|--|--------|
| 1 | VGH | P | Power for LCD | |
| 2 | DIO2 | I/O | Start pulse signal | |
| 3 | AVDD | P | Analog power for source driver | |
| 4 | CHNSL1 | I | Control signal, please set to '1' | |
| 5 | CHNSL0 | I | Control signal, please set to '1' | |
| 6 | VCC | P | Digital power for source driver | |
| 7 | POL | I | Output data polarity control signal | |
| 8 | REV | I | Data inversion control signal output for source driver | |
| 9 | LINV | I | Polarity control signal | |
| 10 | MUX2 | I | Source driver control signal | |
| 11 | MUX1 | I | Source driver control signal | |
| 12 | MUX0 | I | Source driver control signal | |
| 13 | GAMA | I | Source driver control signal ,please set to '1' | |
| 14 | LD2 | I | Source driver control signal | |
| 15 | LD1 | I | Source driver control signal | |
| 16 | OP1 | I | Output buffer driving capacity control signal | |
| 17 | OP0 | I | Output buffer driving capacity control signal | |
| 18 | MODE | I | Control signal , please set to '1' | |
| 19 | GND | P | Digital ground | |
| 20 | B5 | I | Blue data | |
| 21 | B4 | I | Blue data | |
| 22 | B3 | I | Blue data | |
| 23 | B2 | I | Blue data | |
| 24 | B1 | I | Blue data | |
| 25 | B0 | I | Blue data | |
| 26 | GND | P | Digital ground | |
| 27 | AGND | P | Analog ground | |
| 28 | V14 | P | Gamma reference voltage | |
| 29 | V13 | P | Gamma reference voltage | |
| 30 | V12 | P | Gamma reference voltage | |

| | | | | |
|----|--------|---|--|--|
| 31 | V11 | P | Gamma reference voltage | |
| 32 | V10 | P | Gamma reference voltage | |
| 33 | V9 | P | Gamma reference voltage | |
| 34 | V8 | P | Gamma reference voltage | |
| 35 | V7 | P | Gamma reference voltage | |
| 36 | V6 | P | Gamma reference voltage | |
| 37 | V5 | P | Gamma reference voltage | |
| 38 | V4 | P | Gamma reference voltage | |
| 39 | V3 | P | Gamma reference voltage | |
| 40 | V2 | P | Gamma reference voltage | |
| 41 | V1 | P | Gamma reference voltage | |
| 42 | AVDD | P | Analog power for source driver | |
| 43 | GND | P | Digital ground | |
| 44 | G5 | I | Green data | |
| 45 | G4 | I | Green data | |
| 46 | G3 | I | Green data | |
| 47 | G2 | I | Green data | |
| 48 | G1 | I | Green data | |
| 49 | G0 | I | Green data | |
| 50 | GND | P | Digital ground | |
| 51 | R5 | I | Red data | |
| 52 | R4 | I | Red data | |
| 53 | R3 | I | Red data | |
| 54 | R2 | I | Red data | |
| 55 | R1 | I | Red data | |
| 56 | R0 | I | Red data | |
| 57 | GND | P | Digital ground | |
| 58 | PRSEL1 | I | Source driver control signal , please set to '0' | |
| 59 | PRSEL0 | I | Source driver control signal , please set to '1' | |
| 60 | SHL | I | Source driver horizontal shift direction control | |
| 61 | CLK | I | Output data clock for source driver | |
| 62 | EDGSL | I | Source driver control signal | |
| 63 | RSTB | I | Reset pin, low active | |
| 64 | VCC | P | Digital power for source driver | |
| 65 | AGND | P | Analog ground | |

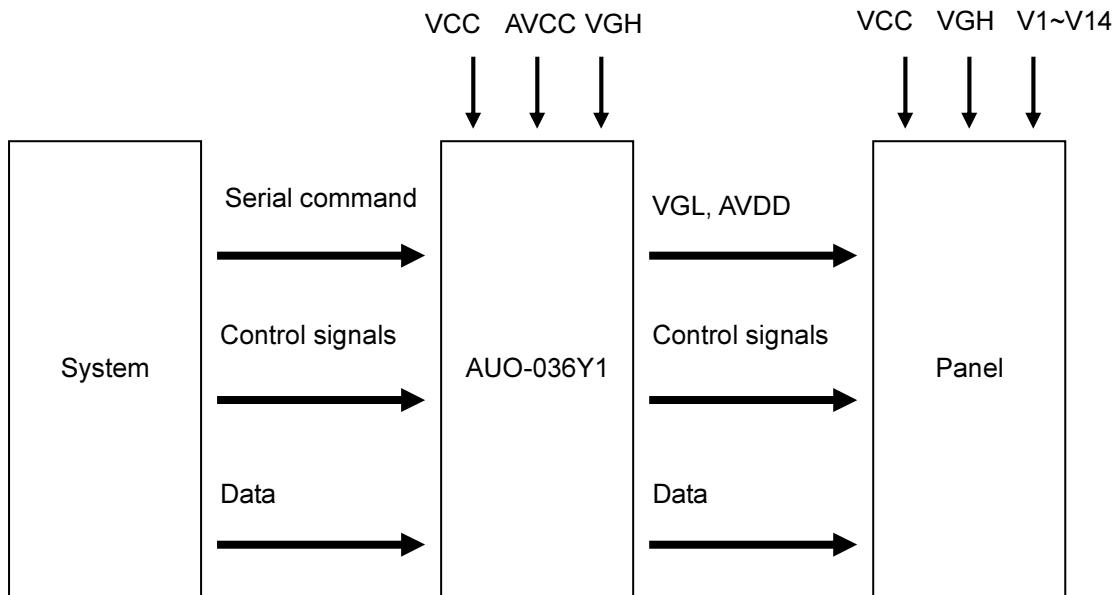
| | | | | |
|----|------|-----|--------------------------|--|
| 66 | DIO1 | I/O | Start pulse signal | |
| 67 | SW6 | I | Control signal | |
| 68 | SW5 | I | Control signal | |
| 69 | SW4 | I | Control signal | |
| 70 | SW3 | I | Control signal | |
| 71 | SW2 | I | Control signal | |
| 72 | SW1 | I | Control signal | |
| 73 | VGL | P | Power for LCD | |
| 74 | VGH | P | Power for LCD | |
| 75 | CK | I | Control signal | |
| 76 | XCK | I | Control signal | |
| 77 | VST | I | Control signal | |
| 78 | NC | | not connected | |
| 79 | NC | | not connected | |
| 80 | VCOM | I | Common electrode voltage | |

I: Input, O: Output, P: Power

Note1: For pin sequence arrangement, please refer to the figure as below:



b. Block Diagram



c. Backlight Driving Section

Connector type: JST PHR-2

| No. | Symbol | I/O | Description | Remark |
|-----|--------|-----|--|--------|
| 1 | GND | - | Ground for backlight unit | -- |
| 2 | HI | I | Power supply for backlight unit (High voltage) | -- |

5. Absolute Maximum Ratings

| Items | Symbol | Product Specification | | | Unit |
|-----------------------|---------|-----------------------|------|---------|------|
| | | Min. | Typ. | Max. | |
| Power Voltage | Vcc | -0.3 | | 4 | V |
| | AVDD | -0.5 | | 13.5 | V |
| | VGH | -0.5 | | 17 | V |
| | VGL | -17 | | 0.5 | V |
| | VGH-VGL | -0.5 | | 26.5 | V |
| Input Signal Voltage | Vin | -0.3 | | VCC+0.3 | V |
| Operating Temperature | Topa | 0 | | 60 | □ |
| Storage Temperature | Tstg | -25 | | 80 | □ |

6. Electrical Characteristics

a. Typical Operation Condition

| Items | Symbol | Product Specification | | | Unit |
|------------------------|--------|-----------------------|----------|-----------|------|
| | | Min. | Typ. | Max. | |
| Power Voltage | VCC | 3.0 | 3.3 | 3.6 | VCC |
| | AVDD | 8 | 10.5 | 12 | AVDD |
| | VGH | 10 | 13.5 | 15 | VGH |
| | VGL | -5 | -7 | -9 | VGL |
| | VCOM | 0.35*AVDD | 0.5*AVDD | 0.65*AVDD | VCOM |
| Input H/L levelVoltage | VIH | 0.7*VCC | — | VCC | VIH |
| | VIL | 0 | — | 0.3*VCC | VIL |

(All value should be measured under the condition of GND=AVss=0V)

b. Current Consumption

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|--------------------|--------|-----------|------|-------|------|------|
| Current For Driver | IGH | VGH=12V | — | 96.82 | | uA |
| | IGL | VGL=-7V | | 48.52 | | uA |
| | ICC | VCC=3.3V | | 2.54 | | mA |
| | IDD | AVDD=10V | | 24.43 | | mA |

c. Backlight Driving Condition

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---------------|--------|-----------|-------|------|------|------|
| Voltage | Vf | Note1 | | 13.2 | 15.2 | Vrms |
| Current | If | Note1 | | 200 | | mA |
| LED life time | | Note 1,2 | 10000 | - | | Hrs |

Note 1: Panel surface temperature should be kept less than content of "D.2. Absolute maximum ratings"

Note 2: The "LEd life time" is defined as the module brightness decrease to 50% original brightness at Ta=25□, IL=200mA

d. Timing Condition

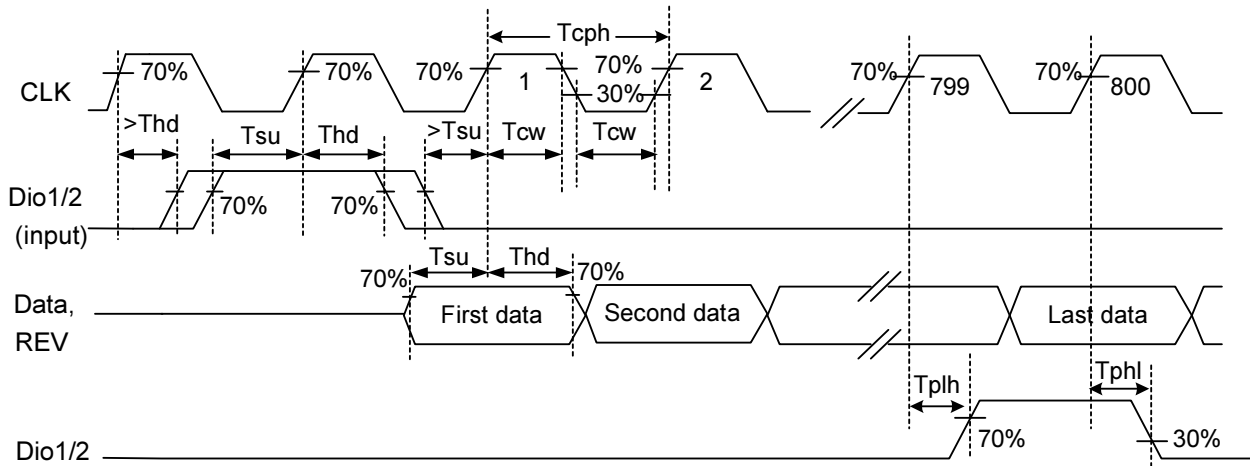
AC Electrical Characteristics (VCC =3V, AVDD=10V, AVSS=GND=0V, TA= 25 °C)

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Conditions |
|---|-------------|------|------|------|------|--------------------------------|
| CLK frequency | Fclk=1/Tclk | - | - | 45 | MHz | As EDGSL="0" |
| CLK frequency | Fclk=1/Tclk | - | - | 22.5 | MHz | As EDGSL="1" |
| CLK pulse width | Tcw | 6 | - | - | ns | |
| Data set-up time | Tsu | 4 | - | - | ns | X1 ~ X5, REV and DIO1/2 to CLK |
| Data hold time | Thd | 2 | - | - | ns | |
| Propagation delay of DIO1/2 high to low level | Tphl | 6 | 10 | 15 | ns | CL=25pF |
| Propagation delay of DIO1/2 low to high level | Tplh | 6 | 10 | 15 | ns | CL=25pF |
| Time that the last data to LD1 | Tld1 | 1 | - | - | Tclk | |
| LD1 pulse width | Twld1 | 2 | - | - | Tclk | |
| Time that LD1 to DIO1/2 | Tlds | 5 | - | - | Tclk | |
| Time that LD1 to LD2 | Tld2 | 2 | - | - | Tclk | |
| LD2 pulse width | Twld2 | 1 | - | - | Tclk | |
| MUX/LINV/POL setup time | Tsu2 | 6 | - | - | ns | |
| MUX/LINV/POL hold time | Thd2 | 6 | - | - | ns | |
| Output stable time | Tst | - | - | - | us | Refer to LD2 timing chart |

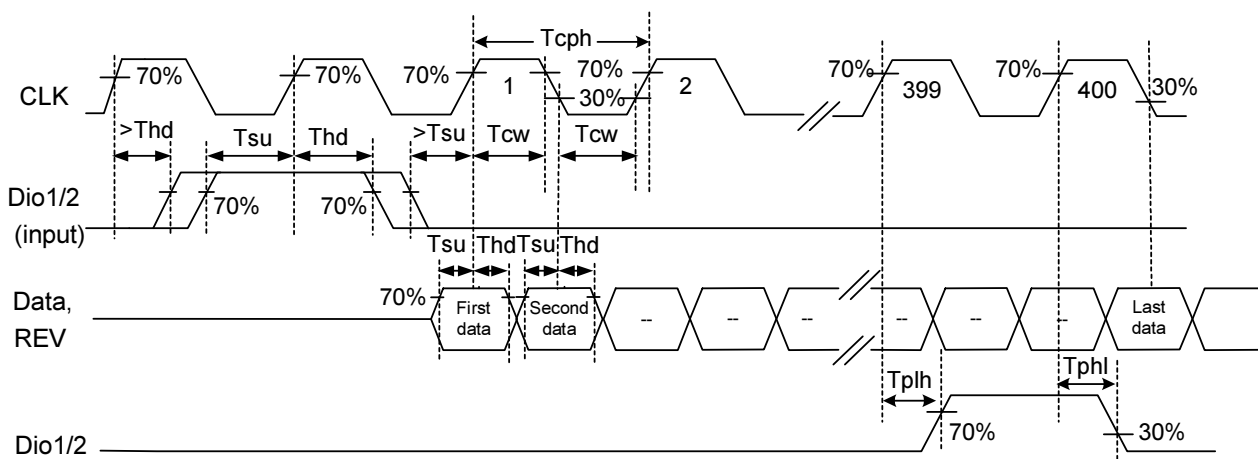
Timing Waveforms

Timing Diagram 1 (CHNSL="1", others setting = Default)

<< EDGSL= "0", Default >>

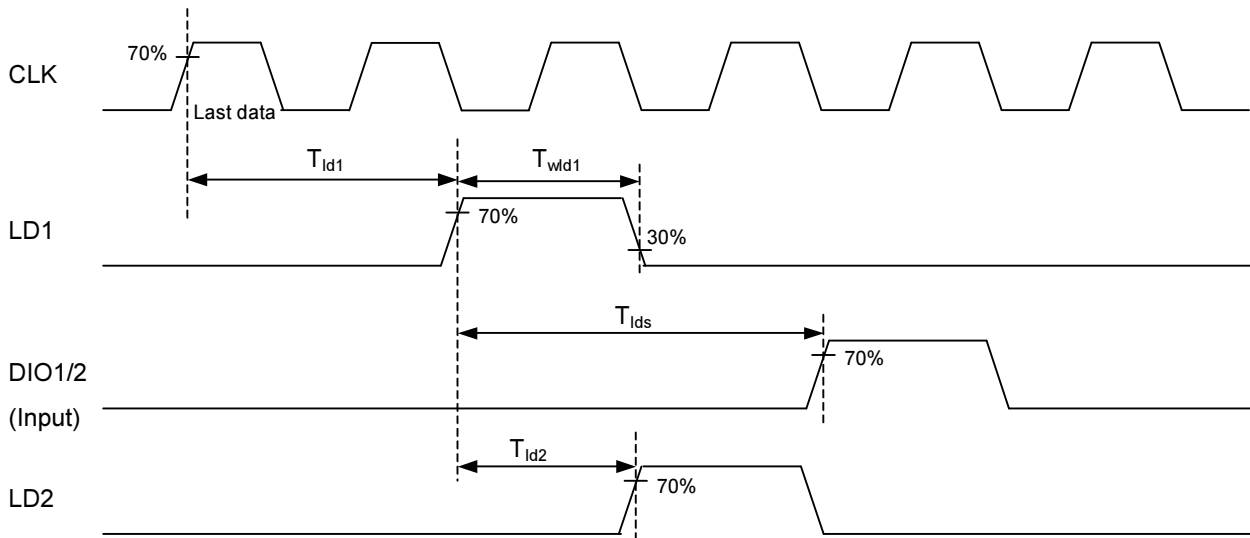


<< EDGSL= "1">>



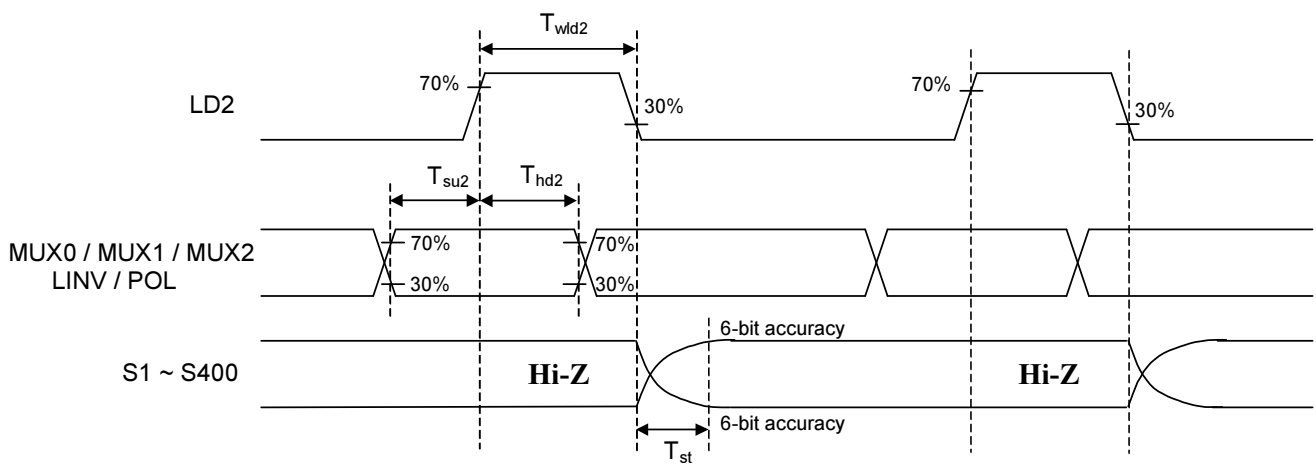
Timing Diagram 2

LD1 Timing Chart



Remark: During source output pre-charging are no relationship(T_{ld2}) of the LD1 and LD2.

LD2 Timing Chart



7. Touch Panel Specifications

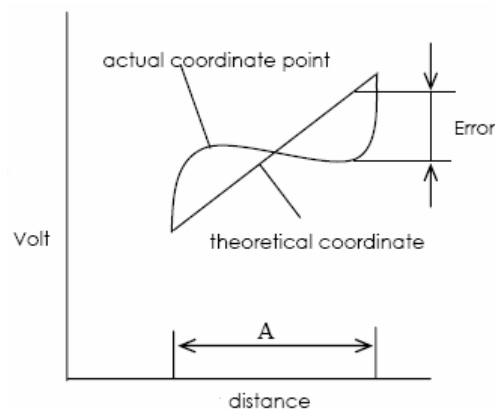
a. FPC Pin Assignment

| Pin No. | Symbol | I/O |
|---------|--------|-----|
| 1 | Right | O |
| 2 | Down | O |
| 3 | Left | O |
| 4 | Up | O |

b. Electrical Characteristics

| Item | Min. | Max. | Unit | Remark | |
|------------------------|--------|------|----------|-------------|--------------|
| Operating Voltage / DC | -- | 7 | V | Standard 5V | |
| Contact Current | -- | 1 | mA | | |
| Operating Current | Film | -- | 20 | mA | |
| | Glass | -- | 20 | mA | |
| Terminal Resistance | X-axis | 200 | 1200 | Ω | At connector |
| | Y-axis | 200 | 900 | | |
| Linearity | -1.5% | 1.5% | -- | Note 1 | |
| Insulation Resistance | 20M | -- | Ω | DC 25V | |
| Response Time | -- | 10 | ms | | |

Note 1: Measurement condition of Linearity: difference between actual voltage & theoretical voltage is an error at any points. Linearity is the value max. error voltage divided by voltage difference on active area.



c. Mechanical Characteristics

| Item | Min. | Max. | Unit | Remark |
|---------------------------------|------|------|------|------------|
| Hardness of Surface | 3 | -- | H | JIS K-5600 |
| Operation Force (Pen or Finger) | -- | 100 | gf | Note 1 |

Note 1: Within "guaranteed active area", but not on the edge and dot-spacer.

d. Durability Test

| Item | Min. | Max. | Unit | Remark |
|---------------------------|-------|------|-------|-----------|
| Touch Test | 1000K | | Times | Note 1 |
| Handwriting Friction Test | 100K | | Times | Note 2, 3 |

Note 1: By using $\Phi 12\text{mm}/R8.0\text{mm}$ silicon rubber, under the loading of 250g to impact the surface of touch panel under the speed of 2 time/second, after repeat knocking 1000k times, goods must fulfill:

Terminal Resistance: as defined in 7.b

Linearity Error: as defined in 7.b

Insulation Resistance: as defined in 7.b

Note 2: By using $\Phi 3.0\text{mm}/R0.8\text{mm}/\text{POM}$ pen with 2.45N (250g) loading under 70mm/sec moving speed, within the touch panel 35mm linear contact range and repeat 100K times(one direction moving as test one time), goods must fulfil:

Terminal Resistance: as defined in 7.b

Linearity Error: as defined in 7.b

Insulation Resistance: as defined in 7.b

Note 3: Test area - Along the diagonals of active area of the touch panel, and the friction center is the same as the center of active area. It means that the distance is 17.5mm extended both at the friction center two sides along the diagonals of active area of the touch panel and proceeding handwriting friction test.

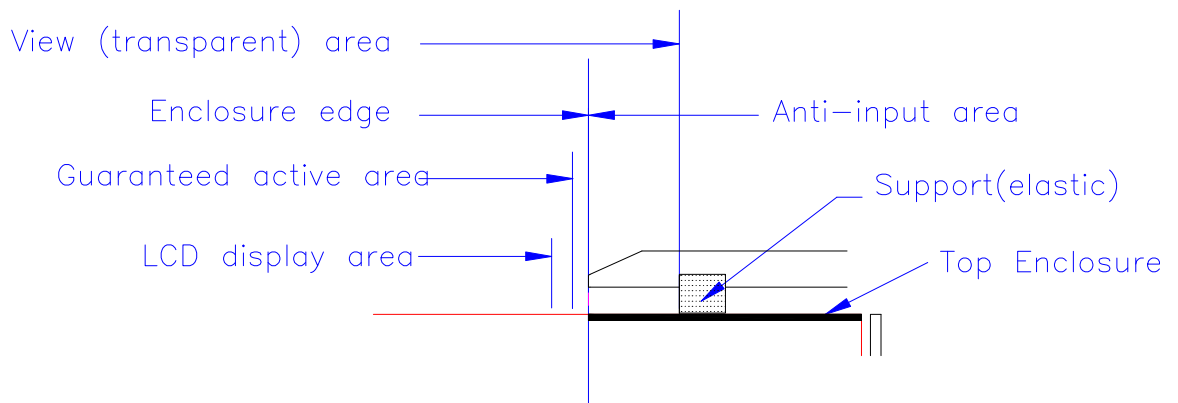
e. Attention

Please pay attention for below matters at mounting design of touch panel of LCD module.

- 1) Do not design enclosure pressing the view area to prevent from miss input.
- 2) Enclosure support must not touch with view area.
- 3) Do not put a heavy force along the edge of the active area.
- 4) Use elastic or non-conductive material to enclosure touch panel.
- 5) Do not bond film of touch panel with enclosure.

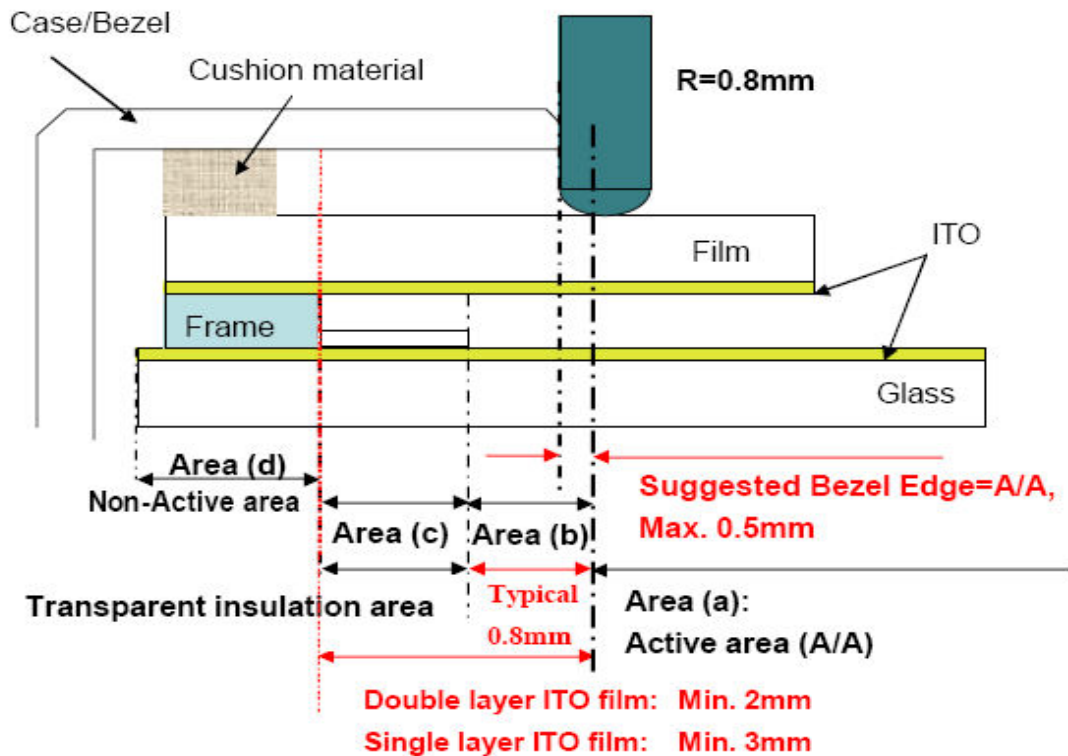
- 6) The touch panel edge is conductive. Do not touch it with any conductive part after mounting.

If user wants to cleaning touch panel by air gun, pressure 2kg/cm² below is suggested. Not to blow glass from FPC site to prevent FPC peeled off



- 7) Do not put a heavy shock or stress on touch panel and film surface. Ex. Don't lift the panel by film face with vacuum.
- 8) Do not lift LCD module by FPC.
- 9) Please use dry cloth or soft cloth with neutral detergent (after wring dry) or one with ethanol at cleaning. Do not use any organic solvent, acid or alkali liquor.
- 10) Do not pile touch panel. Do not put heavy goods on touch panel.
- 11) Structure/area definition: The structure and the performance guaranteed area of this touch panel are defined below:

Below figure illustrates the recommended bezel and cushion design. In order to prevent unusual performance degradation and malfunction of the touch panel, please carry out the set case designing and a touch panel assembling method after surely considering the definition of each area illustrated in below figure.



Area (a): Active area

The active area is guaranteed the position data detectable precision, operation force and other operations. It's strongly recommended to place the operation button or menu keys within the active area. Due to structure, the active area is less durable at the edge or close to the edge.

Area (b): Operating non-guaranteed area

The area doesn't guarantee a touch panel operation and its function. When this area is pressed, touch panel shows degradation of its performance and durability such as a pen sliding durability becomes about one-tenth compared with the active area (Area(a) as guaranteed area) and its operation force requires about double. About 0.5mm outside from a boundary of the active area corresponds to this area.

Area (c): Pressing prohibition area

The area which forbids pressing, because an excessive load is applied to a transparent electrode (ITO) and a serious damage is given to a touch panel function by pressing.

Area (d): Non-active area

The area doesn't activate even if pressed.

8. Optical Specifications

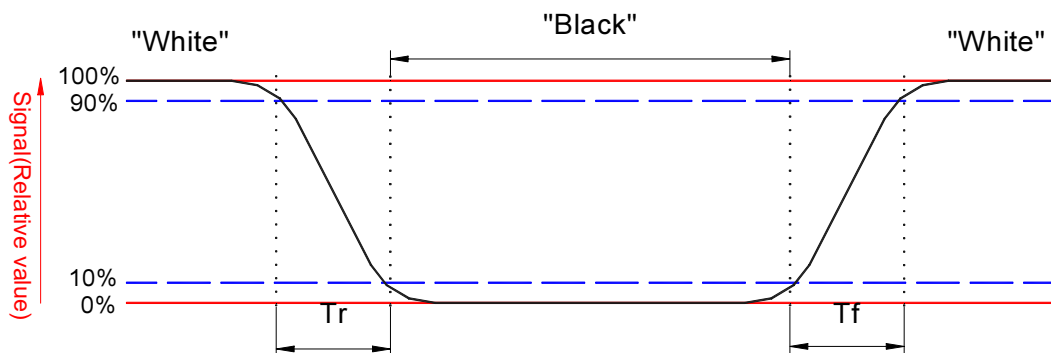
| Item | Symbol | Condition | Min. | Typ. | Max. | Unit | Remark |
|--------------------|--------|------------------------------------|------|------|------|------|------------|
| Response time | Rise | $\theta=0^\circ$ | - | 12 | - | ms | Note 3,5 |
| | Fall | | - | 18 | - | ms | |
| Contrast ratio | CR | At optimized Viewing angle | 150 | 250 | - | | Note 4, 5 |
| Viewing angle | Top | $CR \geq 10$ | 35 | 45 | - | deg. | Note 5 |
| | Bottom | | 50 | 60 | - | | |
| | Left | | 45 | 55 | - | | |
| | Right | | 45 | 55 | - | | |
| Brightness | Y_L | $I_L=200\text{mA}$, 25° | 200 | 250 | - | nits | Note 1,2,6 |
| White chromaticity | x | $\theta=0^\circ$ | 0.27 | 0.32 | 0.37 | | Note 6 |
| | y | $\theta=0^\circ$ | 0.30 | 0.35 | 0.40 | | |

Note 1 : Ambient temperature =25 $^\circ$, and LED current $I_f= 200 \text{ mA}$. To be measured in the dark room.

Note 2 :To be measured on the center area of panel with a viewing cone of 1 $^\circ$ by Topcon luminance meter BM-7, after 10 minutes operation.

Note 3. Definition of response time:

The response time is defined as the time interval between the 10% and 90% of amplitudes. The output signals of photo detector are measured when the input signals are changed from "black" to "white"(falling time) and from "white" to "black"(rising time).



Note 4. Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when LCD is at "White" state}}{\text{Photo detector output when LCD is at "Black" state}}$$

Note 5. White $V_i = V_{i50} \pm 1.5V$

Black $V_i = V_{i50} \mp 2.0V$

“±” means that the analog input signal swings in phase with V_{COM} signal.

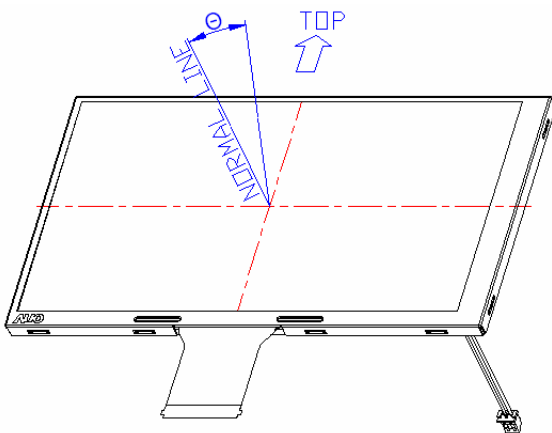
“∓” means that the analog input signal swings out of phase with V_{COM} signal.

V_{i50} : The analog input voltage when transmission is 50%

The 100% transmission is defined as the transmission of LCD panel when all the input terminals of module are electrically opened.

Note 6. Measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.

Note 7. Definition of viewing angle, Refer to figure as below.



Note 8. Measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.

9. Reliability Test Items

| No. | Test items | Conditions | Remark |
|-----|----------------------------|---|----------------------------------|
| 1 | High temperature storage | Ta= 80□ 240Hrs | |
| 2 | Low temperature storage | Ta= -25□ 240Hrs | |
| 3 | High temperature operation | Ta= 60□ 240Hrs | |
| 4 | Low temperature operation | Ta= 0□ 240Hrs | |
| 5 | High temperature and high | Ta= 60□, 90% RH 240Hrs | Operation |
| 6 | Heat shock | -20□- -70□/100 cycles 1Hrs/cycle | Non-operation |
| 7 | Electrostatic discharge | ±200V,200pF(0Ω), once for each terminal | Non-operation |
| 8 | Vibration | Frequency : 10~55Hz | JIS C7021 A-10 condition A |
| | | Stoke : 1.5mm | |
| | | Sweep : 10 ~ 55 ~ 10Hz | |
| | | 2 hours for each direction of X,Y,Z (6 hours for total) | |
| 9 | Mechanical shock | 100G, 6ms, ±X,±Y,±Z 3 times for each direction | JIS C7021, A-7 condition C |
| 10 | Vibration (with carton) | Random vibration: 0.015G ² /Hz from 5~200Hz -6dB/octave from 200~500Hz | IEC 68-34 |
| 11 | Drop (with carton) | Height: 60cm 1 corner, 3 edges, 6 surfaces | JIS Z0202 |

Note 1: Ta: Ambient temperature.

Note 2: In the standard conditions, there is not display function failure issue occurred. All the cosmetic specification is judged before the reliability stress.

10. Handling Precautions

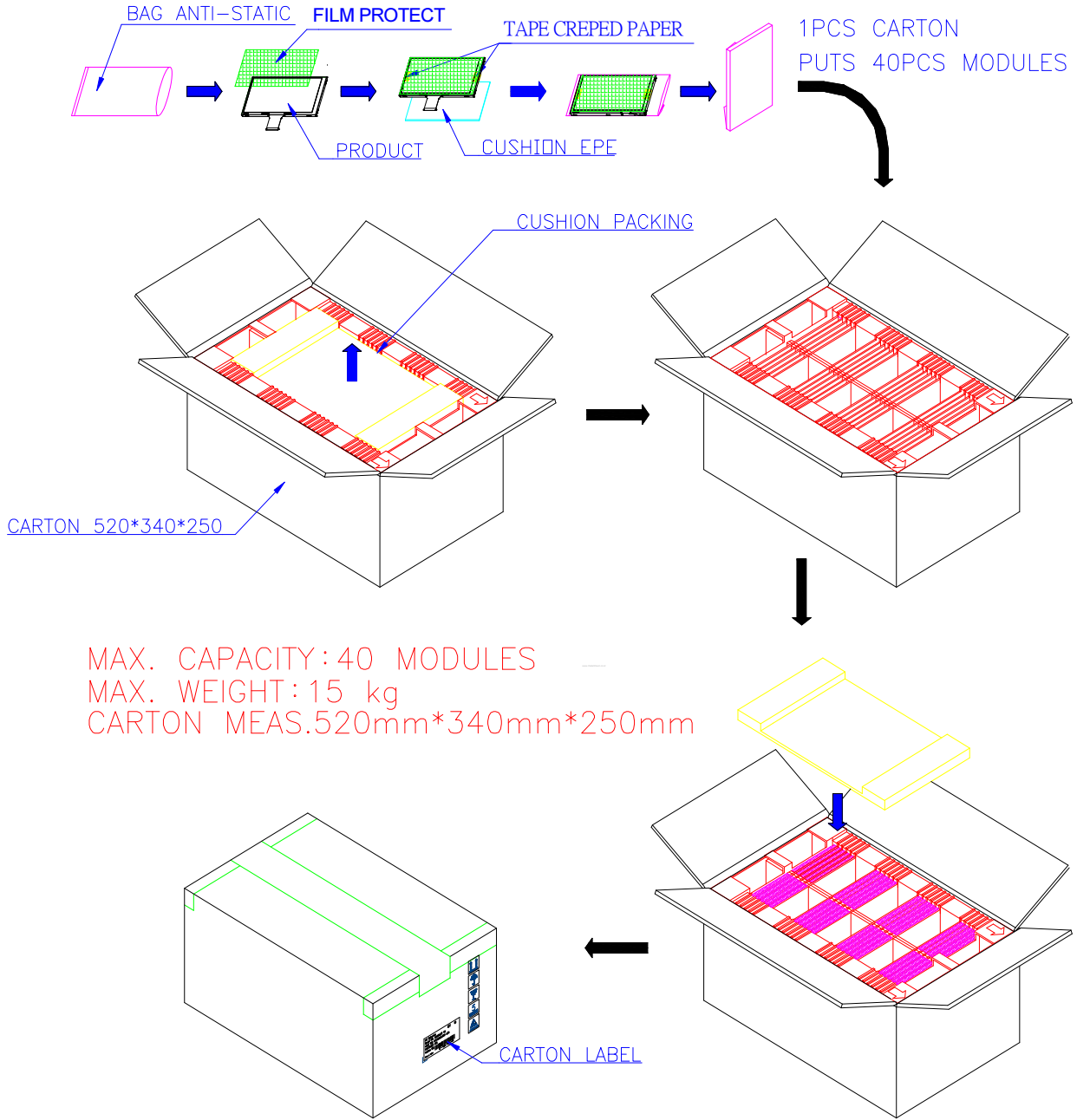
- a Since the touch panel is easily damaged, pay attention not to scratch it.
- b Be sure to turn off power supply when inserting or disconnecting from input connector.
- c Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
- d When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.



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- e Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
- f Do not open nor modify the Module Assembly.
- g Do not press the reflector sheet at the back of the module to any directions.
- h At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
- i After installation of the TFT Module into a system enclosure, do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.

12. Packing Form





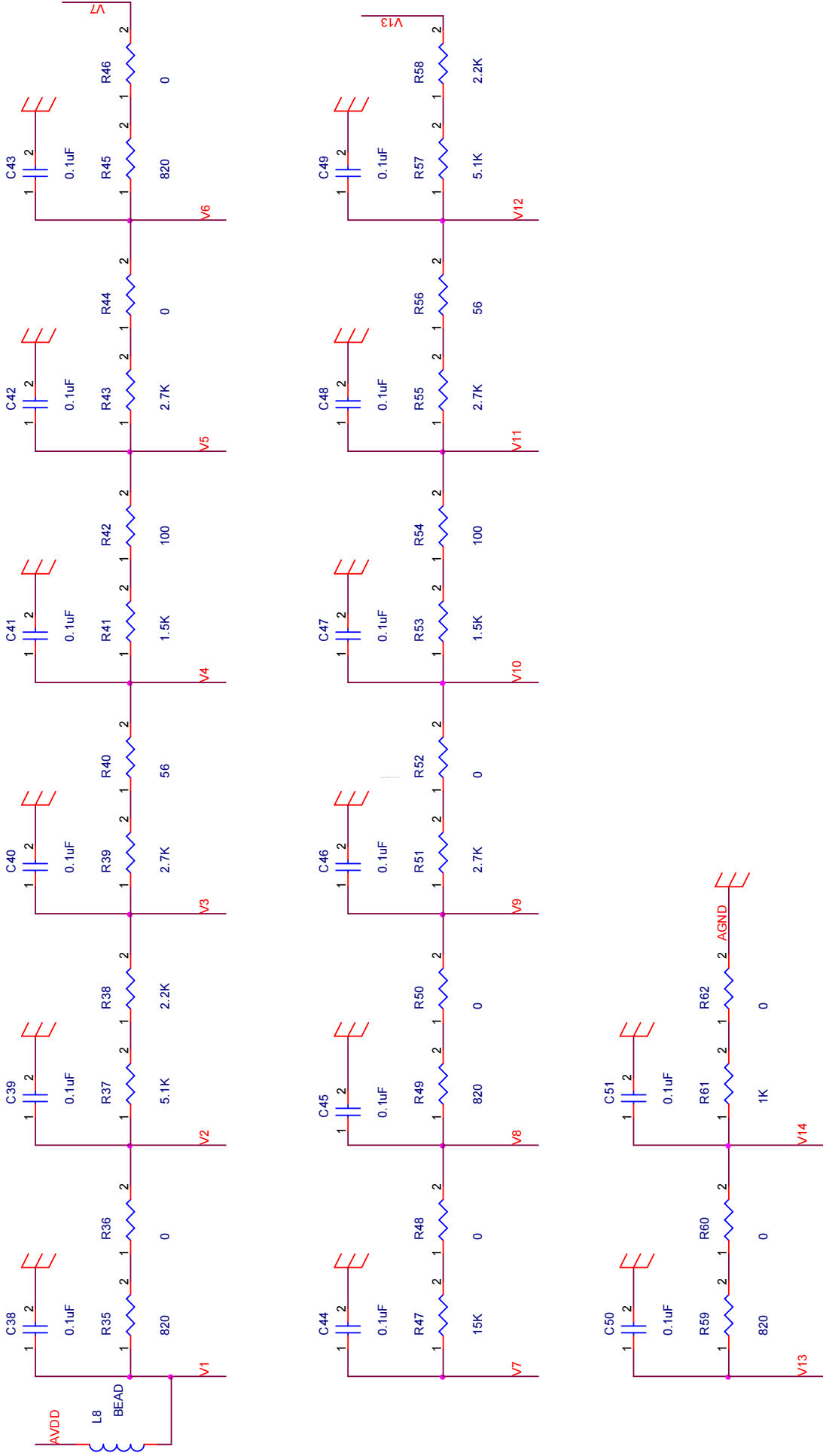
友達光電
AUOptronics

Model A065VL01 V2

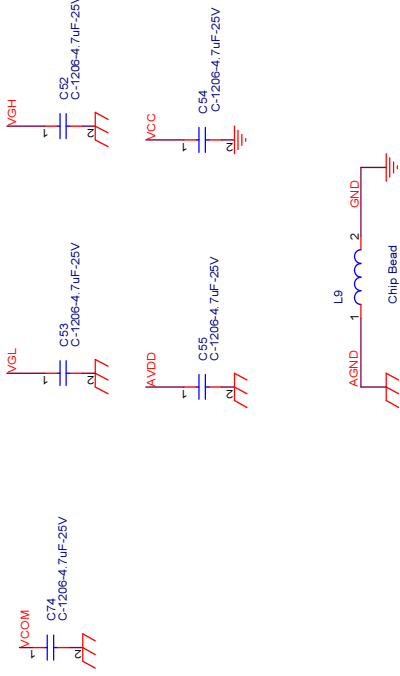
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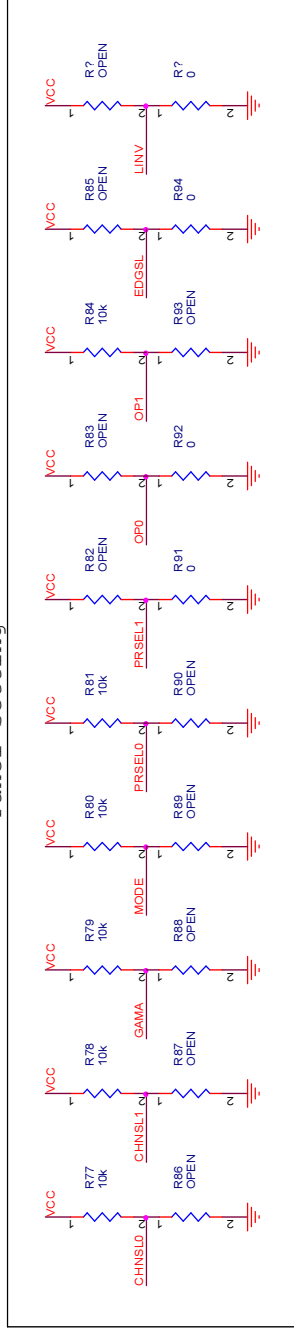
AUO-036 Circuit design



Gamma Circuit



Panel setting



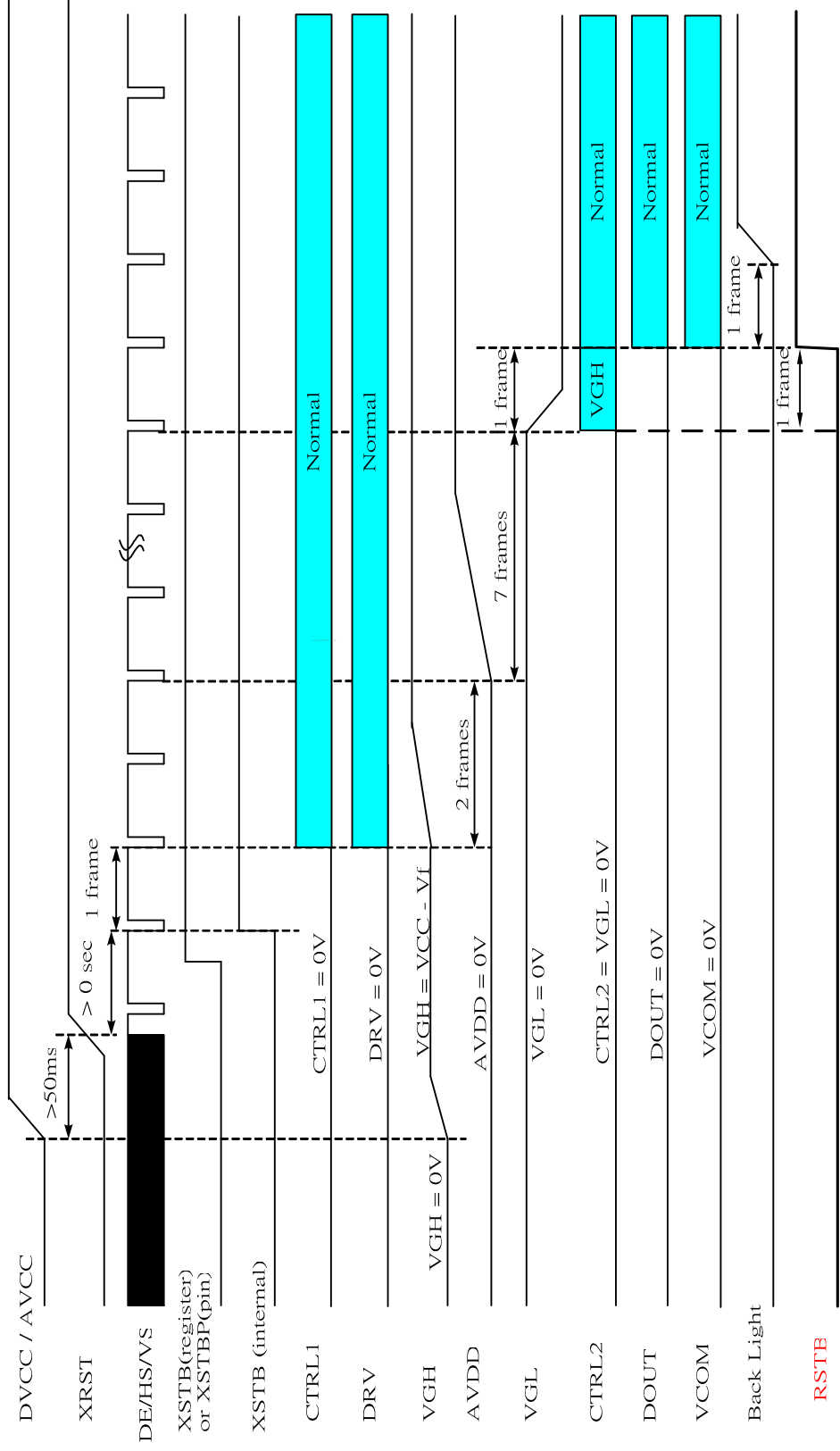
FH16-80S-0.3SH(05) 80pin 0.3mm

| | |
|---------|----|
| VCOM | 80 |
| NC | 79 |
| VS | 78 |
| VS1 | 77 |
| ACK | 76 |
| CK | 75 |
| VGH | 74 |
| VCL | 73 |
| SW1 | 72 |
| SW2 | 71 |
| SW3 | 70 |
| SW4 | 69 |
| SW5 | 68 |
| SW6 | 67 |
| DI01 | 66 |
| AGND | 65 |
| VCC | 64 |
| VCC | 63 |
| EDGSL | 62 |
| DCLK | 61 |
| SHL | 60 |
| PRESEL0 | 59 |
| PRESEL1 | 58 |
| CHNSLT | 57 |
| R0 | 56 |
| R1 | 55 |
| R2 | 54 |
| R3 | 53 |
| R4 | 52 |
| R5 | 51 |
| GND | 50 |
| G0 | 49 |
| G1 | 48 |
| G2 | 47 |
| G3 | 46 |
| G4 | 45 |
| G5 | 44 |
| SRD | 43 |
| AVDD | 42 |
| V1 | 41 |
| V2 | 40 |
| V3 | 39 |
| V4 | 38 |
| V5 | 37 |
| V6 | 36 |
| V7 | 35 |
| V8 | 34 |
| V9 | 33 |
| V10 | 32 |
| V11 | 31 |
| V12 | 30 |
| V13 | 29 |
| V14 | 28 |
| AGND | 27 |
| B0 | 26 |
| B1 | 25 |
| B2 | 24 |
| B3 | 23 |
| B4 | 22 |
| B5 | 21 |
| B6 | 20 |
| MODE | 19 |
| OP0 | 18 |
| OP1 | 17 |
| LD1 | 16 |
| LD2 | 15 |
| MUX0 | 14 |
| MUX1 | 13 |
| MUX2 | 12 |
| MUX3 | 11 |
| MUX4 | 10 |
| RFV | 9 |
| POL | 8 |
| VCC | 7 |
| CHNSLO | 6 |
| CHNSL1 | 5 |
| AVDD | 4 |
| DI02 | 3 |
| VGH | 2 |
| | 1 |



2. Power On/Off Sequence

Panel Setting



Power ON sequence

Note1: The using of standby mode signal **XSTBP**, please refer to AUO-036Y1 spec. P28.

Note2: Panel reset signal **RSTB**, please follow the power on sequence.

Note3: Input mode selection signal **IMOD**

IMOD="Low" : DE mode, please set VSYNC and HSYNC to "high".

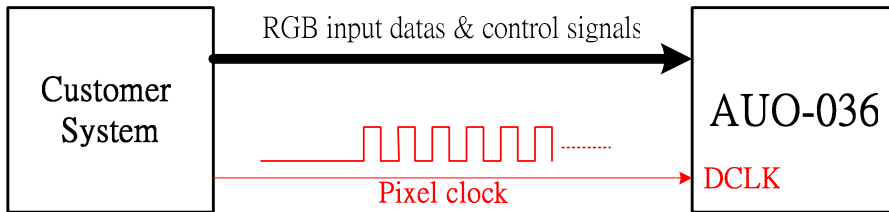
IMOD="high" : HSYNC/VSYNC mode, please set DE to "low".

Recommended register setting

| Reg NO. | Reg Name | Register Data | | | | | | | | Note |
|---------|-----------|---------------|----|----|----|----|----|----|----|-----------|
| | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 0 | VDD_ADJ | X | X | X | 0 | 1 | 1 | 1 | 1 | VDD=11v |
| 1 | VEE_ADJ | X | X | X | X | 0 | 1 | 0 | 0 | (Default) |
| 2 | COMDC | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | (Default) |
| 3 | VPOSITION | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | (Default) |
| 4 | HPOSITION | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | |
| 5 | PANEL | X | 1 | 1 | 0 | 0 | 0 | 0 | 1 | |
| 6 | FUNCTION | X | X | X | 1 | 1 | 1 | 0 | 1 | |
| 128 | BLANK(1) | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | (Default) |
| 129 | PREC(1) | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | (Default) |
| 130 | SWITCH(1) | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | (Default) |
| 131 | INT(1) | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | (Default) |
| 132 | BLANK(2) | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | (Default) |
| 133 | PREC(2) | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | (Default) |
| 134 | SWITCH(2) | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | (Default) |
| 135 | INT(2) | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | (Default) |
| 136 | BLANK(3) | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | (Default) |
| 137 | PREC(3) | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | (Default) |
| 138 | SWITCH(3) | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | (Default) |
| 139 | INT(3) | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | (Default) |

Important Note

1. In customer system, the initial state of the pixel clock output (DCLK pin of AUO-036) must be set to **Low**.



2. Please do not cut off the pixel clock during system operation.