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μPD78044 Family (μPD78042/043/044/P044) 8-Bit, K-Series Microcontrollers With FIP Controller/Driver and A/D Converter

Preliminary

September 1993

Description

The μPD78042, μPD78043, μPD78044, and μPD78P044 are members of the K-Series® of microcontrollers featuring a FIP® (VF) controller/driver, A/D converter, 8-bit hardware multiply and divide instructions, bit manipulation instructions, four banks of main registers, an advanced interrupt handling facility, and a powerful set of memory-mapped on-chip peripherals.

Timing is generated by two oscillators. The main oscillator normally drives the CPU and most peripherals. The 32.768-kHz subsystem oscillator provides time keeping when the main oscillator is turned off. Since CMOS power dissipation is proportional to clock rate, the μPD78044 family provides a software selectable instruction cycle time from 0.48 μs to 122 μs. The STOP and HALT modes turn off parts of the microcontroller for additional savings. The data retention mode keeps RAM contents valid down to 2.0 V.

These devices are ideally suited for applications in portable battery-powered equipment, office automation, communications, automotive and consumer electronics, home appliances, and PC peripherals.

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Features

- FIP controller/driver
  - Up to 34 lines of direct-drive, high-voltage output
  - Eight software-controller intensity levels
  - 48 bytes of display RAM
  - Refresh of display without CPU intervention
  - Key scan capability
- Eight-channel, 8-bit A/D converter
- Two-channel serial communications interface
  - 8-bit clock-synchronous interface 0
    - Full-duplex, three-wire mode
    - NEC serial bus interface (SBI) mode
    - Half-duplex, two-wire mode
  - 8-bit clock-synchronous interface 1
    - Full-duplex, three-wire mode
    - Automatic transfer, full-duplex three-wire mode
- Timers; six channels
  - Watchdog timer
  - 16-bit timer/event counter
  - Two 8-bit timer/event counters usable as one 16-bit timer/event counter
  - 6-bit up/down counter for external events
  - Watch (clock) timer
- 68 I/O and bidirectional I/O lines, including high voltage lines for FIP drive
  - Two CMOS input-only lines
  - 27 CMOS bidirectional I/O lines
  - Five n-channel, open-drain I/O lines at 15 V maximum
  - 16 p-channel, open-drain I/O lines at 35 V maximum
  - 18 p-channel, open-drain output lines at 35 V maximum
  - Software or mask selectable pullup or pulldown resistors available on many port lines
- Powerful instruction set
  - 8-bit unsigned multiply and divide
  - 16-bit arithmetic and data transfer instructions
  - 1-bit and 8-bit logic instructions
- Minimum instruction execution times
  - 0.48/0.95/1.91/3.81/7.63 μs using 4.19-MHz main system clock
  - 122 μs using 32.768-kHz subsystem clock
- Memory-mapped on-chip peripherals
  - Special function registers
- Programmable priority, vectored-interrupt controller (two levels)
- Programmable buzzer and clock outputs
- Power-saving and battery back up
  - Variable CPU clock rate
  - STOP mode
  - HALT mode
  - 2-V data retention mode
- CMOS operation; V_{DD} from 2.7 to 6.0 V

Internal High-Capacity ROM and RAM

	78042	78043	78044	78P044
ROM	16K bytes	24K bytes	32K bytes	—
PROM	—	—	—	32K bytes
High-speed RAM	512 bytes	1024 bytes	1024 bytes	1024 bytes
Serial buffer RAM	64 bytes	64 bytes	64 bytes	64 bytes
FIP display RAM	48 bytes	48 bytes	48 bytes	48 bytes

3e

Ordering Information

Part Number	ROM	Package (Package Dwg)
μPD78042GF-xxx-3B9	16K mask ROM	80-pin plastic QFP (P80GF-80-3B9-1)
μPD78043GF-xxx-3B9	24K mask ROM	
μPD78044GF-xxx-3B9	32K mask ROM	
μPD78P044GF-3B9	32K OTP ROM	
μPD78P044KL-S	32K UV EPROM	80-pin ceramic LCC with window (X80KW-80A)

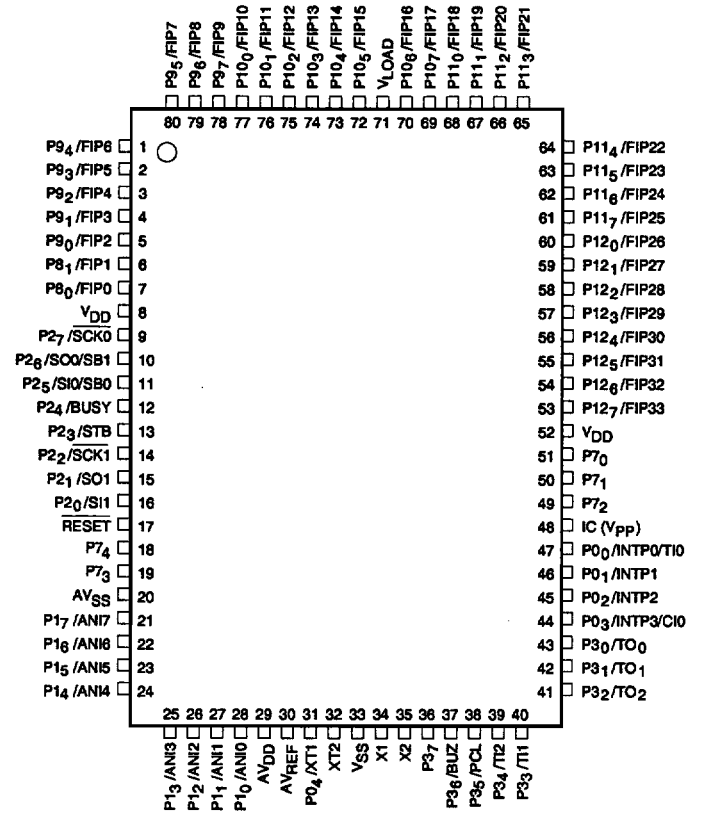
Notes:

(1) xxx indicates ROM code suffix

(2) All devices listed are Standard Quality Grade.

Pin Configurations

80-Pin Plastic QFP or Ceramic LCC With Window



Notes:

(1) Connect IC (internally connected) pin (V_{PP} on μPD78P044) to V_{SS}.

(2) AV_{DD} should be connected to V_{DD}.

(3) AV_{SS} should be connected to V_{SS}.

83YL-9518B (9/93)

3e

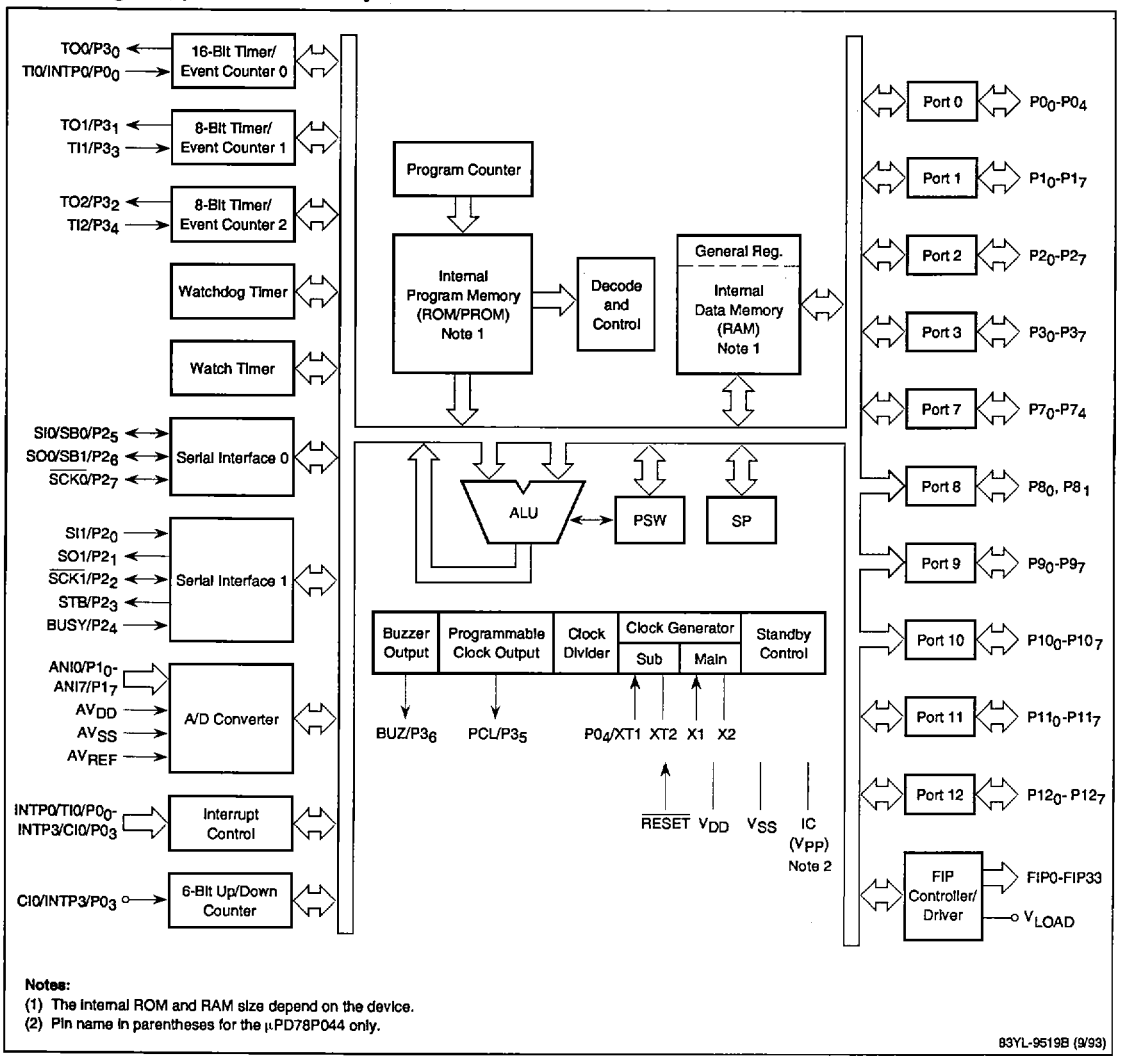
Pin Functions; Normal Operating Mode

Symbol	First Function	Symbol	Alternate Functions
$P0_0$	Port 0; 5-bit, bit-selectable I/O. (Bits 0 and 4 are input only)	INTP0 TI0	External maskable interrupt External count clock input to timer 0
$P0_1$		INTP1	External maskable interrupt
$P0_2$		INTP2	External maskable interrupt
$P0_3$		INTP3 CI0	External maskable interrupt Up/down counter clock input
$P0_4$		XT1	Crystal oscillator or external clock input for subsystem clock
$P1_0$ - $P1_7$	Port 1; 8-bit, bit-selectable I/O port.	ANI0 - ANI7	Analog input to A/D converter
$P2_0$	Port 2; 8-bit, bit-selectable I/O port.	SI1	Serial data input; three-wire serial I/O mode
$P2_1$		SO1	Serial data output; three-wire serial I/O mode
$P2_2$		$\overline{SCK1}$	Serial clock I/O for serial interface 1
$P2_3$		STB	Serial interface; automatic transmit/receive strobe output
$P2_4$		BUSY	Serial interface; automatic transmit/receive busy input
$P2_5$		SI0 SB0	Serial data input; three-wire serial I/O mode Two- or three-wire serial I/O mode
$P2_6$		SO0 SB1	Serial data output; three-wire serial I/O mode Two- or three-wire serial I/O mode
$P2_7$		$\overline{SCK0}$	Serial clock I/O for serial interface 0
$P3_0$	Port 3; 8-bit, bit-selectable I/O port.	TO0	Timer output from timer 0
$P3_1$		TO1	Timer output from timer 1
$P3_2$		TO2	Timer output from timer 2
$P3_3$		TI1	External count clock input to timer 1
$P3_4$		TI2	External count clock input to timer 2
$P3_5$		PCL	Programmable clock output
$P3_6$		BUZ	Programmable buzzer output
$P3_7$		—	
$P7_0$ - $P7_4$	Port 7; 5-bit,bit selectable I/O port. N-channel, open drain.	—	
$P8_0$ - $P8_1$	Port 8; 2-bit, output port. P-channel, open drain.	FIP0, FIP1	FIP digit select outputs
$P9_0$ - $P9_7$	Port 9; 8-bit, output port. P-channel, open drain.	FIP2 - FIP9	FIP digit select outputs
$P10_0$ - $P10_5$	Port 10; 8-bit, output port. P-channel, open drain.	FIP10 - FIP15	FIP digit select or segment outputs
$P10_6$ - $P10_7$		FIP16 - FIP17	FIP segment outputs
$P11_0$ - $P11_7$	Port 11; 8-bit, bit selectable I/O port. P-channel open drain.	FIP18 - FIP25	FIP digit select outputs
$P12_0$ - $P12_7$	Port 12; 8-bit, bit selectable I/O port. P-channel open drain.	FIP26 - FIP33	FIP digit select outputs
V_{LOAD}	FIP controller/driver; pulldown resistor connection.		
$\overline{RESET}$	External system reset input		
X1	Crystal/ceramic resonator connection or external clock input for main system clock		

Pin Functions; Normal Operating Mode (cont)

Symbol	First Function	Symbol	Alternate Functions
X2	Crystal/ceramic resonator connection or inverse of external clock for main system clock		
XT2	Crystal oscillator or left open when not using the subsystem clock		
AV_{REF}	A/D converter reference voltage		
AV_{DD}	A/D converter power supply input		
AV_{SS}	A/D converter ground		
V_{DD}	Power supply input		
V_{PP}	μPD78P044 PROM programming power supply input		
V_{SS}	Power supply ground		
IC	Internal connection		

Block Diagram, μPD78044 Family



Notes:
(1) The internal ROM and RAM size depend on the device.
(2) Pin name in parentheses for the μPD78P044 only.

83YL-9519B (9/93)

FUNCTIONAL DESCRIPTION

Central Processing Unit

The central processing unit (CPU) of the μPD78044 family features 8- and 16-bit arithmetic including an 8- by 8-bit unsigned multiply and a 16- by 8-bit unsigned divide (producing a 16-bit quotient and an 8-bit remainder). The multiply executes in 3.82 μs and the divide in 5.97 μs using the fastest clock cycle with a 4.19-MHz main system clock.

A CALLT vector table and a CALLF area decrease the number of bytes in the call instructions for commonly used subroutines. A one-byte call instruction can access up to 32 subroutines through their addresses contained in the CALLT vector table (40H to 7FH). A two-byte call instruction can access any routine beginning in a specific CALLF area (0800H to 0FFFH).

Internal System Clock Generator

The internal system clocks of the μPD78044 family are derived from the main system or subsystem clock oscillator. See figure 1. The clocks for the watch timer and programmable clock output are derived from the subsystem clock (f_{XT}) or main system clock (f_X). The clocks for all other peripheral hardware are derived from the main system clock.

The CPU clock (ϕ) can be supplied from the main system clock (f_X) or subsystem clock (f_{XT}). Using the processor clock control register (PCC), a CPU clock frequency equal to f_X, $f_X/2$, $f_X/4$, $f_X/8$, $f_X/16$ or the subsystem clock f_{XT} can be selected. The CPU clock selected should be based on the power supply voltage available and the desired power consumption. On power up, the CPU clock defaults to the lowest speed from the main system clock and can be changed while the microcomputer is running.

Since the shortest instruction takes two CPU clocks to execute, the fastest instruction execution time (t_{CY}) of 0.48 μs is achieved with a 4.19-MHz main system clock and a V_{DD} of 4.5 to 6.0 volts. The fastest instruction execution time available across the full voltage range of 2.7 to 6.0 volts is 0.96 μs with a 4.19-MHz main system clock. For the lowest power consumption, the CPU can be operated from the subsystem clock and the fastest instruction execution time is 122 μs at 32.768 kHz.

Memory Space

Program and data memory are mapped into the 64K-byte address space (0000H-FFFFH). See figure 2. The μPD78044 family is optimized for single-chip operation and does not permit external memory.

Internal Program Memory

All devices in the μPD78044 family have internal program memory. The μPD78042, μPD78043, and μPD78044 contain 16K, 24K, and 32K bytes of internal ROM, respectively. The μPD78P044 contains 32K bytes of UV EPROM or one-time programmable ROM. To allow the μPD78P044 to emulate the mask ROM devices, the amount of internal program memory available in the μPD78P044 can be selected using the memory size switching register (IMS).

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Internal RAM

Internal RAM comprises three types: high-speed, buffer, and FIP display. The μPD78042 has 624 bytes of internal RAM and the μPD78043/044/P044 have 1136 bytes.

High-speed RAM contains the general register banks and the stack. Unused portions of RAM and unused register bank locations are available for general storage. The μPD78042 has 512 bytes (FD00H-FEFFH) of high-speed RAM; the μPD78043/044/P044 has 1024 bytes (FB00H-FEFFH).

All devices contain 64 bytes (FA80H-FAFFH) of buffer RAM and 48 bytes (FA50H-FA7FH) of FIP display RAM. The buffer area is used for the automatic transfer mode of serial interface 1 or for general storage. The FIP display area is for display data; unused portions are available for general storage.

CPU Control Registers

Program Counter. The program counter is a 16-bit binary counter register that holds the address of the next instruction to be executed. During reset, the program counter is loaded with the address stored in locations 0000H and 0001H.

Stack Pointer. The stack pointer is a 16-bit register that holds the address of the last item pushed onto the stack. It is decremented before new data is pushed onto the stack and incremented after data is popped off the stack.

Figure 1. Internal System Clock Generator

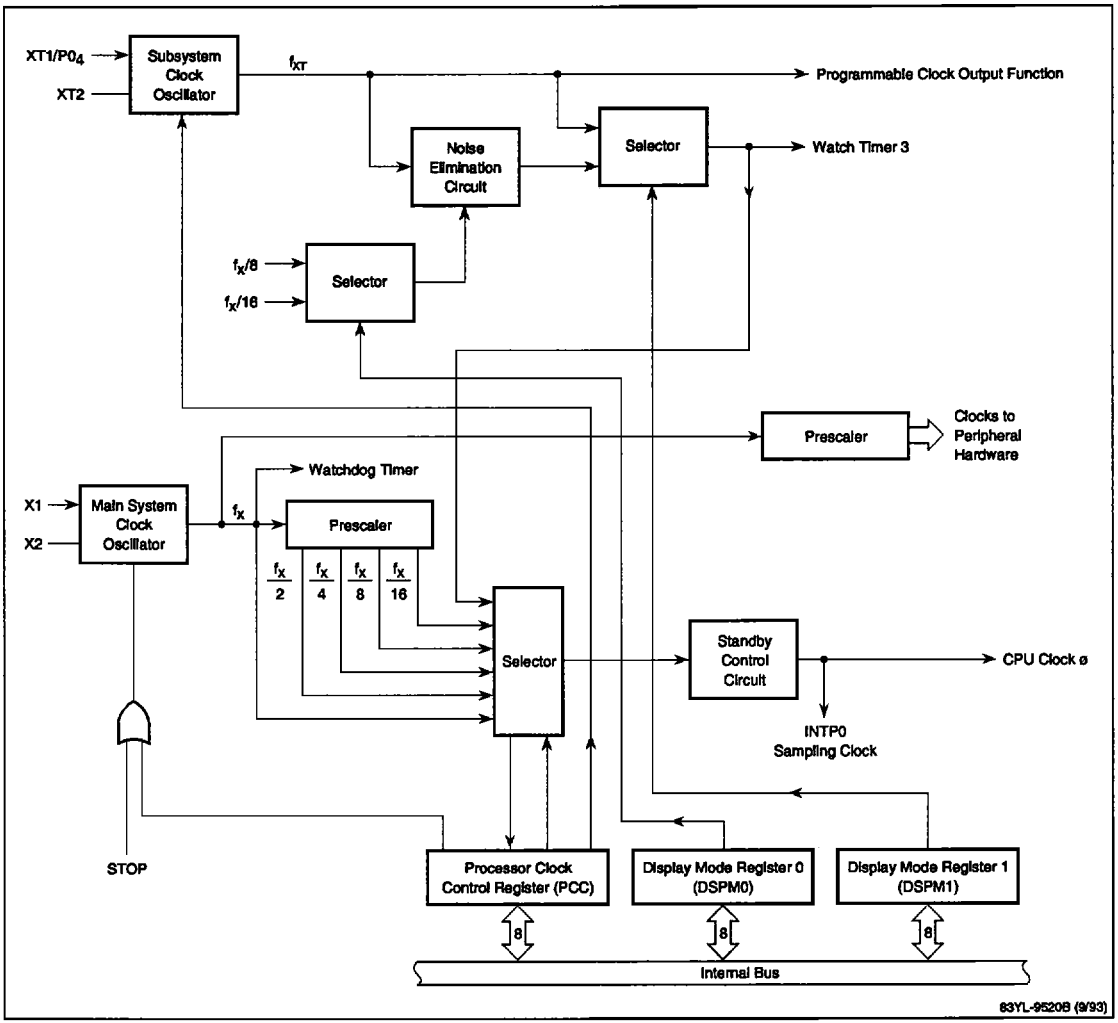
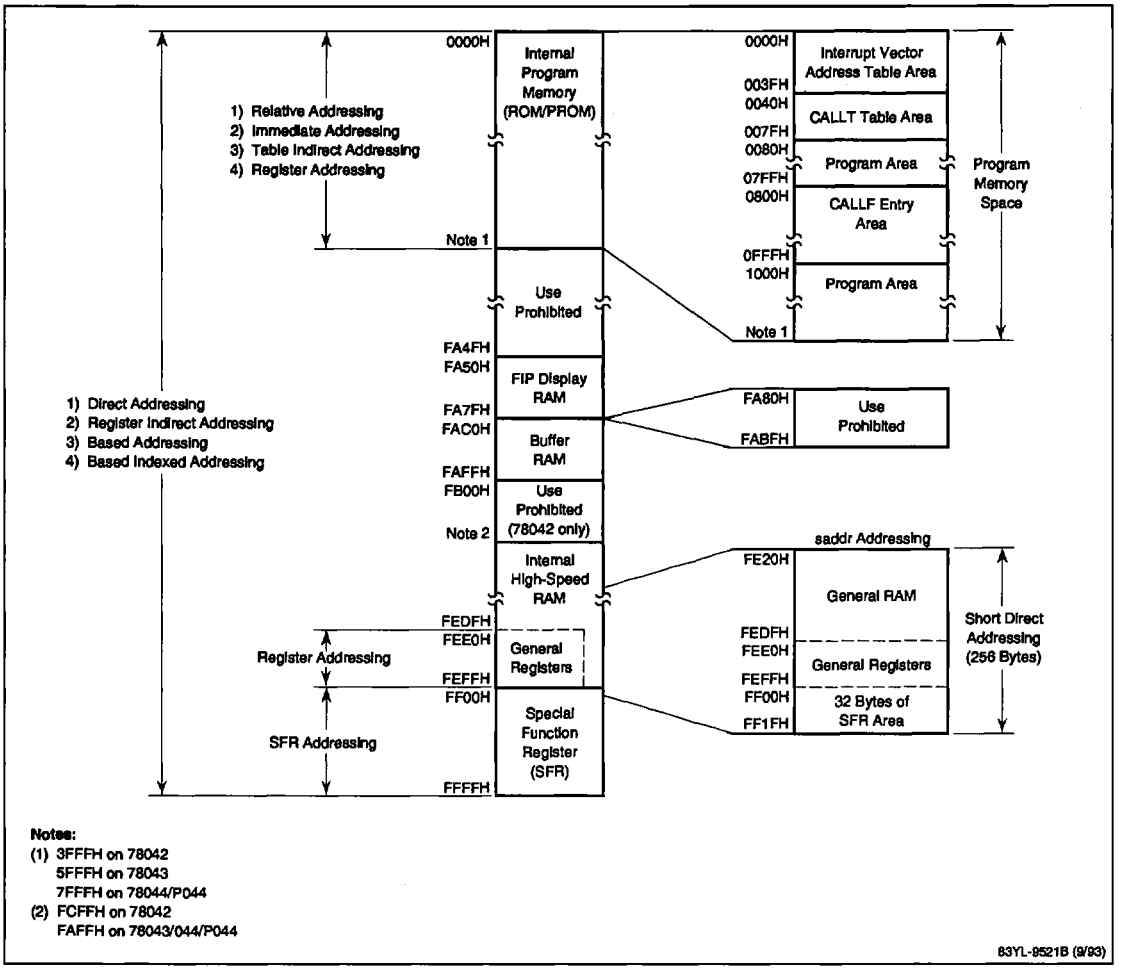


Figure 2. Memory Map



Notes:
(1) 3FFFH on 78042
5FFFH on 78043
7FFFH on 78044/P044
(2) FCFFH on 78042
FAFFH on 78043/044/P044

83YL-9521B (9/93)

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Program Status Word. The program status word (PSW) is an 8-bit register containing flags that are set or reset according to the results of an instruction execution. This register can be written to or read from 8 bits at a time. The individual flags can also be manipulated on bit-by-bit basis. The assignment of PSW bits follows:

7							0
IE	Z	RBS1	AC	RBS0	0	ISP	CY

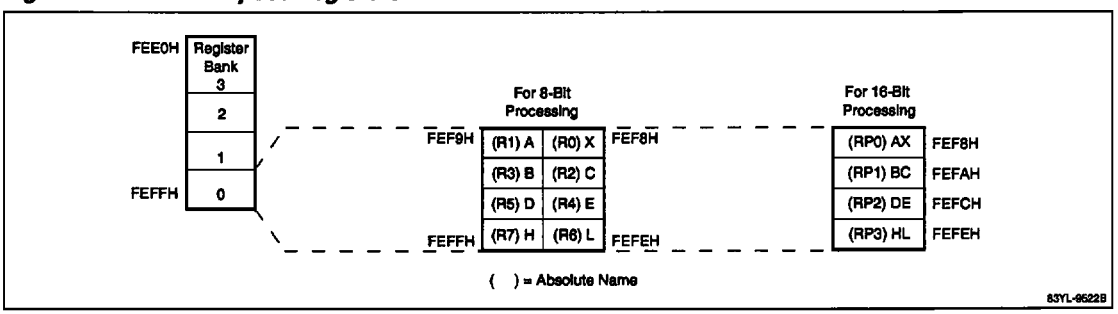
CY	Carry flag
ISP	Inservice (interrupt) priority flag
RBS0, RBS1	Register bank selection flags
AC	Auxiliary carry flag
Z	Zero flag
IE	Interrupt enable flag

General-Purpose Registers

The general-purpose registers (figure 3) are in four banks at addresses FEE0H to FEFFH in high-speed internal RAM. Each bank comprises eight 8-bit registers, which can be paired as four 16-bit registers. Bits RBS0 and RBS1 in the PSW, set under program control, identify the active register banks at any time.

Eight-bit registers have functional names A, X, B, C, D, E, H, L, and absolute names R0 thru R7; the four 16-bit registers have functional names AX, BC, DE, HL and absolute names RP0 thru RP3. Either the functional or absolute name is acceptable for the operand identifier "r" or "rp" in an instruction.

Figure 3. General-Purpose Registers



Addressing

The program memory addressing (ROM) modes provided are relative, immediate, table indirect, and register addressing. The operand addressing modes provided are implied, register, direct, short direct (saddr), special-function (SFR), register indirect, based, based indexed, and stack addressing.

The SFR addressing and saddr addressing modes use direct addressing and require only 1 byte in the instruction to address RAM. Normally a 65K byte address space requires 2 bytes to address it. One-byte addressing results in faster access times, since the instructions are shorter. SFR addressing addresses the entire 256-byte SFR address space from FF00H to FFFFH. Saddr addressing (see figure 2) addresses the 256-byte address space FE20H to FF1FH. FE20H to FEFFH are composed of 224 bytes of internal high speed RAM; FF00H to FF1FH contain the first 32 bytes in the special function register area.

One-byte addressing is accomplished by using the first byte of the instruction for the opcode (and one operand if register A or AX is used) and the second byte of the instruction as an address (offset) into the 256-byte area. If register A or AX is used, the instructions are 2 bytes long thereby providing fast access times. If immediate data is used, the instruction will be 3 or 4 bytes long depending upon whether the immediate data is a byte or a word. Many 16-bit SFRs are in the space FF00H to FF1FH. Using AX as an operand to these SFRs will provide fast access, since the instructions will only 2 bytes long.

Special Function Registers

The input/output ports, timers, capture and compare registers, and the mode and control registers for the peripherals and the CPU are collectively known as special function registers (table 1). They are all memory-mapped between FF00H and FFFFH and can be accessed either by main memory addressing or by one-byte SFR addressing. FF00H to FF1H can also be accessed using saddr addressing. They are 8 or 16 bits, as required; many of the 8-bit registers are capable of single-bit access as well.

Table 1. Special Function Registers

Address	Register (SFR)	Symbol	R/W	Access Units (Bits) 1	8	16	State After Reset
FF00H	Port 0	P0	R/W	x	x	—	00H
FF01H	Port 1	P1	R/W	x	x	—	00H
FF02H	Port 2	P2	R/W	x	x	—	00H
FF03H	Port 3	P3	R/W	x	x	—	00H
FF07H	Port 7	P7	R/W	x	x	—	00H
FF08H	Port 8	P8	W	x	x	—	00H
FF09H	Port 9	P9	W	x	x	—	00H
FF0AH	Port 10	P10	W	x	x	—	00H
FF0BH	Port 11	P11	R/W	x	x	—	00H
FF0CH	Port 12	P12	R/W	x	x	—	00H
FF10H-FF11H	Compare register 00	CR00	R/W	—	—	x	Undefined
FF12H-FF13H	Capture register 01	CR01	R	—	—	x	Undefined
FF14H-FF15H	16-bit timer register	TM0	R	—	—	x	00H
FF16H	Compare register 10	CR10	R/W	—	x	—	Undefined
FF17H	Compare register 20	CR20	R/W	—	x	—	Undefined
FF18H	8-bit timer register 1	TM1	R	x	x	—	00H
FF19H	8-bit timer register 2	TM2	R	x	x	—	00H
FF18H-FF19H	16-bit timer register	TMS	R	—	—	x	0000H
FF1AH	Serial I/O shift register 0	SIO0	R/W	—	x	—	Undefined
FF1BH	Serial I/O shift register 1	SIO1	R/W	—	x	—	Undefined
FF1FH	A/D conversion result register	ADCR	R	—	x	—	Undefined
FF20H	Port mode register 0	PM0	R/W	x	x	—	1FH
FF21H	Port mode register 1	PM1	R/W	x	x	—	FFH
FF22H	Port mode register 2	PM2	R/W	x	x	—	FFH
FF23H	Port mode register 3	PM3	R/W	x	x	—	FFH
FF27H	Port mode register 7	PM7	R/W	x	x	—	1FH
FF2BH	Port mode register 11	PM11	R/W	x	x	—	FFH
FF2CH	Port mode register 12	PM12	R/W	x	x	—	FFH
FF40H	Timer clock select register 0	TCL0	R/W	x	x	—	00H
FF41H	Timer clock select register 1	TCL1	R/W	—	x	—	00H
FF42H	Timer clock select register 2	TCL2	R/W	—	x	—	00H
FF43H	Timer clock select register 3	TCL3	R/W	—	x	—	88H
FF47H	Sampling clock select register	SCS	R/W	—	x	—	00H
FF48H	16-bit timer mode control register	TMC0	R/W	x	x	—	00H
FF49H	8-bit timer mode control register	TMC1	R/W	x	x	—	00H
FF4AH	Watch timer mode control register	TMC2	R/W	x	x	—	00H
FF4EH	16-bit timer output control register	TOC0	R/W	x	x	—	00H
FF4FH	8-bit timer output control register	TOC1	R/W	x	x	—	00H
FF60H	Serial operating mode register 0	CSIM0	R/W	x	x	—	00H
FF61H	Serial bus interface control register	SBIC	R/W	x	x	—	00H

Table 1. Special Function Registers (cont)

Address	Register (SFR)	Symbol	R/W	Access Units (Bits) 1	8	16	State After Reset
FF62H	Slave address register	SVA	R/W	—	x	—	Undefined
FF63H	Interrupt timing specify register	SINT	R/W	x	x	—	00H
FF68H	Serial operation mode register 1	CSIM1	R/W	x	x	—	00H
FF69H	Automatic data transmit/receive control register	ADTC	R/W	x	x	—	00H
FF6AH	Automatic data transmit/receive address pointer register	ADTP	R/W	—	x	—	00H
FF6BH	Automatic data transmission/reception interval specification register	ADTI	R/W	x	x	—	00H
FF80H	A/D converter mode register	ADM	R/W	x	x	—	01H
FF84H	A/D converter input select register	ADIS	R/W	—	x	—	00H
FFA0H	Display mode register 0	DSPM0	R/W	(Note 1)	x	—	00H
FFA1H	Display mode register 1	DSPM1	R/W	—	x	—	00H
FFA8H	6-bit up/down counter mode register	UDM	R/W	x	x	—	00H
FFA9H	6-bit up/down counter	UDC	R/W	—	x	—	00H
FFAAH	6-bit up/down counter compare register	UDCC	R/W	—	x	—	00H
FFE0H	Interrupt flag register L	IF0L	R/W	x	x	—	00H
FFE1H	Interrupt flag register H	IF0H	R/W	x	x	—	00H
FFE0H-FFE1H	Interrupt flag register	IF0	R/W	—	—	x	0000H
FFE4H	Interrupt mask flag register L	MK0L	R/W	x	x	—	FFH
FFE5H	Interrupt mask flag register H	MK0H	R/W	x	x	—	FFH
FFE4H-FFE5H	Interrrupt mask flag register	MK0	R/W	—	—	x	FFFFH
FFE8H	Priority order specify flag register L	PR0L	R/W	x	x	—	FFH
FFE9H	Priority order specify flag register H	PR0H	R/W	x	x	—	FFH
FFE8H-FFE9H	Priority order specify flag register	PR0	R/W	—	—	x	FFFFH
FFECH	External interrupt mode register	INTM0	R/W	—	x	—	00H
FFF0H	Memory size switch register (Note 2)	IMS	W	—	x	—	C8H
FFF7H	Pullup resistor option register	PU0	R/W	x	x	—	00H
FFF9H	Watchdog timer mode register	WDTM	R/W	x	x	—	00H
FFFAH	Oscillation stabilization time select register	OSTS	R/W	—	x	—	04H
FFFBH	Processor clock control register	PCC	R/W	x	x	—	04H

Notes:

(1) Bits 0-6 are read/write and bit 7 is read only.

(2) μPD78P044 only.

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Input/Output Ports

There are 68 port lines on each device in the μPD78044 family. Table 2 lists the port features and figure 4 shows the circuits at the I/O interfaces.

Table 2. Digital Port Features

Port	Input/Output	Notes	Configuration	Direct Drive	Software Pullup Resistors (Note 1)
0	5-bit I/O	2	Bit selectable	—	Byte selectable, input bits only
1	8-bit I/O	—			
2	8-bit I/O	—			
3	8-bit I/O	3	Bit selectable	LED	
7	5-bit, n-channel I/O	4	Bit selectable	—	Not available
8	2-bit, p-channel output	5, 6	N/A	LED, FIP	
9	8-bit, p-channel output	6, 7	NA	LED, FIP	
10	8-bit, p-channel output	6, 7, 8	N/A	LED, FIP	
11	8-bit, p-channel I/O	7	Bit selectable	FIP	
12	8-bit, p-channel I/O	7	Bit selectable	FIP	

Notes:

(1) Software pullup resistors can be internally connected (only on a port basis) to port bits set to input mode.

(2) $P0_0$ and $P0_4$ are input only and do not have a software pullup resistor.

(3) Mask ROM products: pulldown resistors are selectable per bit with a mask option. Not available on the μPD78P044.

(4) Mask ROM products: pullup resistors are selectable per bit with a mask option. Not available on the μPD78P044.

(5) Mask ROM products: pulldown resistors are selectable per bit with a mask option (connection to V_{LOAD} or V_{SS} specifiable as a 2-bit unit).

(6) μPD78P044: pulldown resistors incorporated for all bits (connection to V_{LOAD}).

(7) Mask ROM products: pulldown resistors are selectable per bit with a mask option (connection to V_{LOAD} or V_{SS} specifiable as 4-bit units).

(8) $P10_0$ - $P10_5$: LED, FIP direct drive. $P10_6$ - $P10_7$: FIP direct drive.

Figure 4. Pin Input/Output Circuits

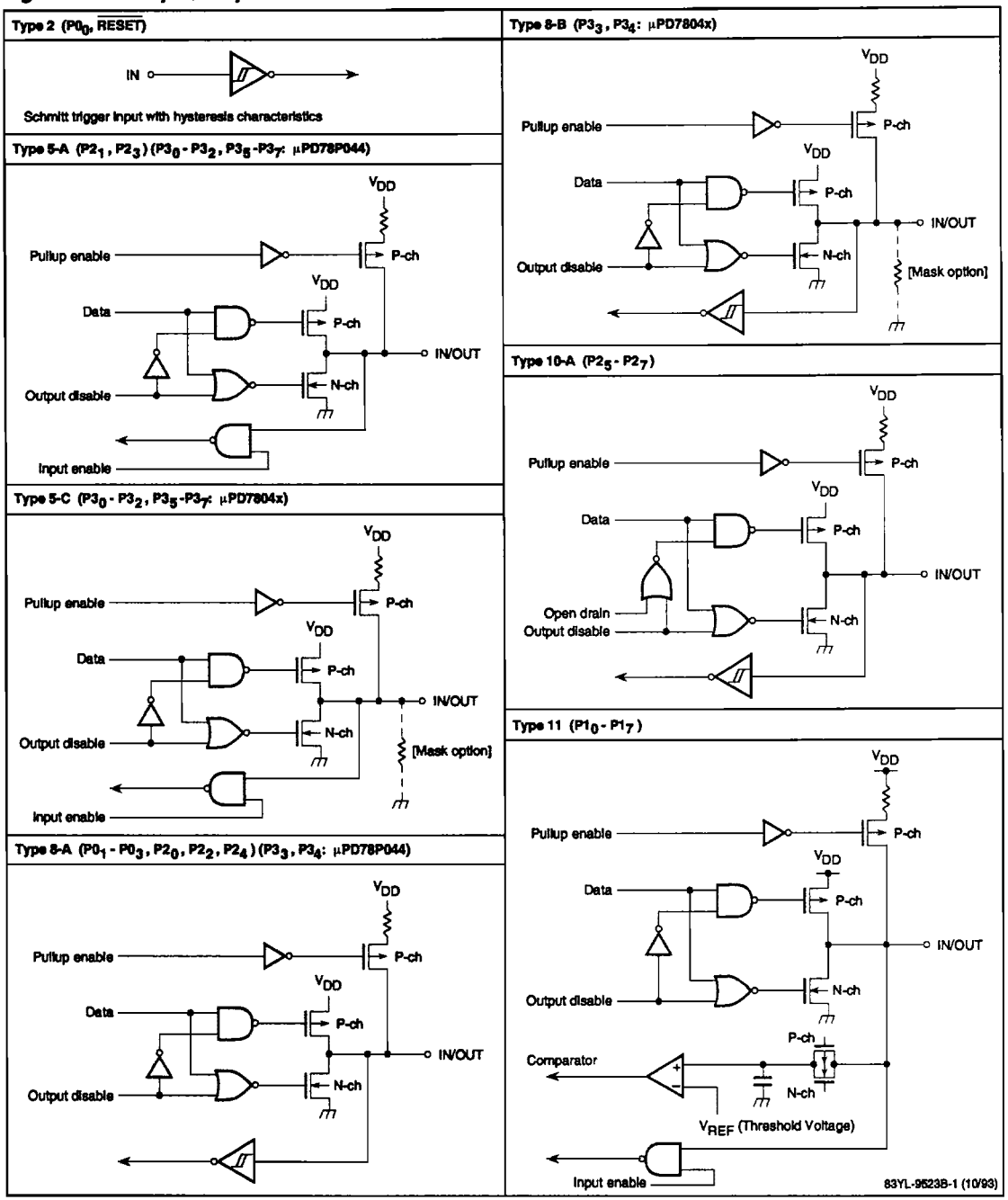

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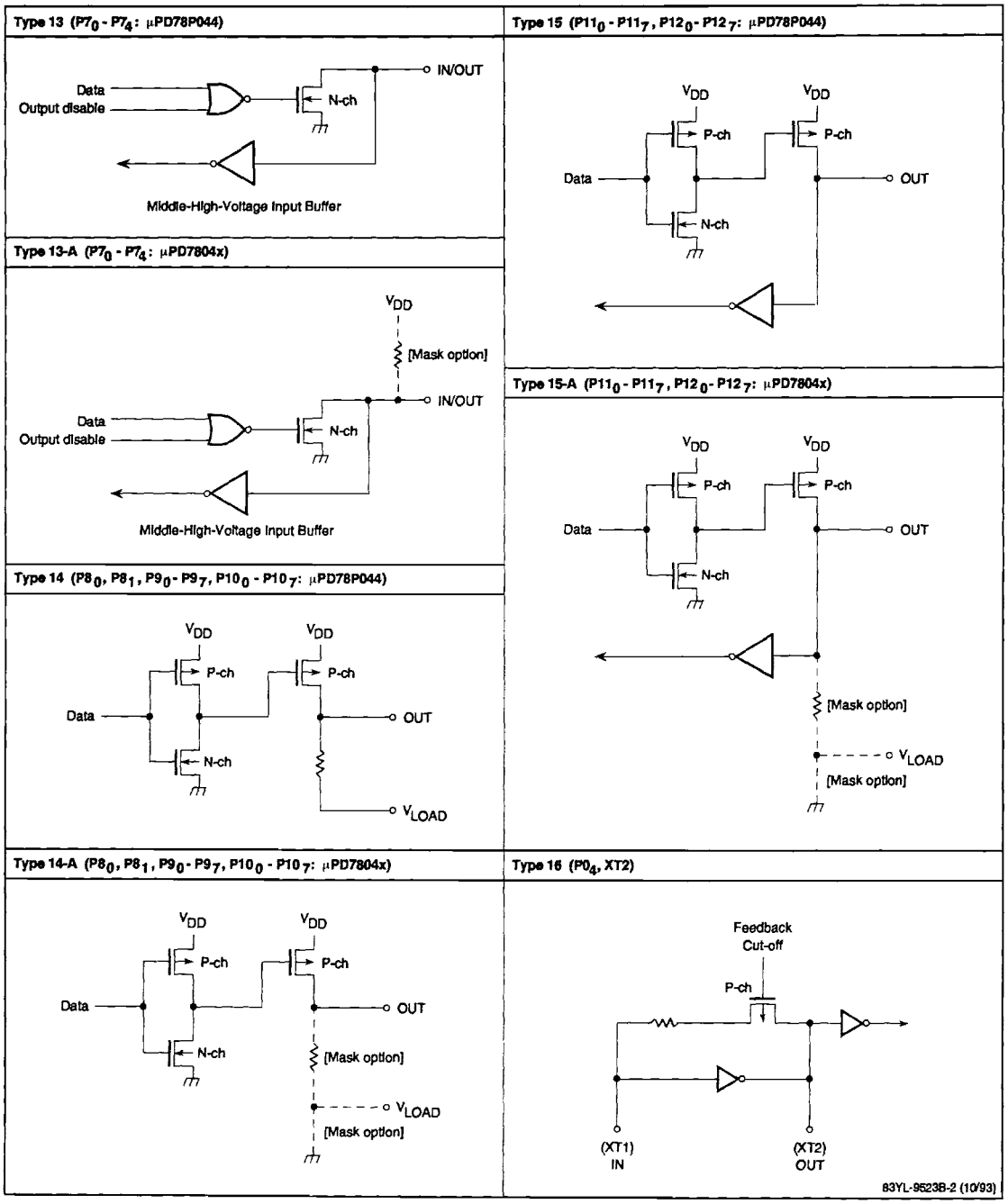
Figure 4. Pin Input/Output Circuits (cont)



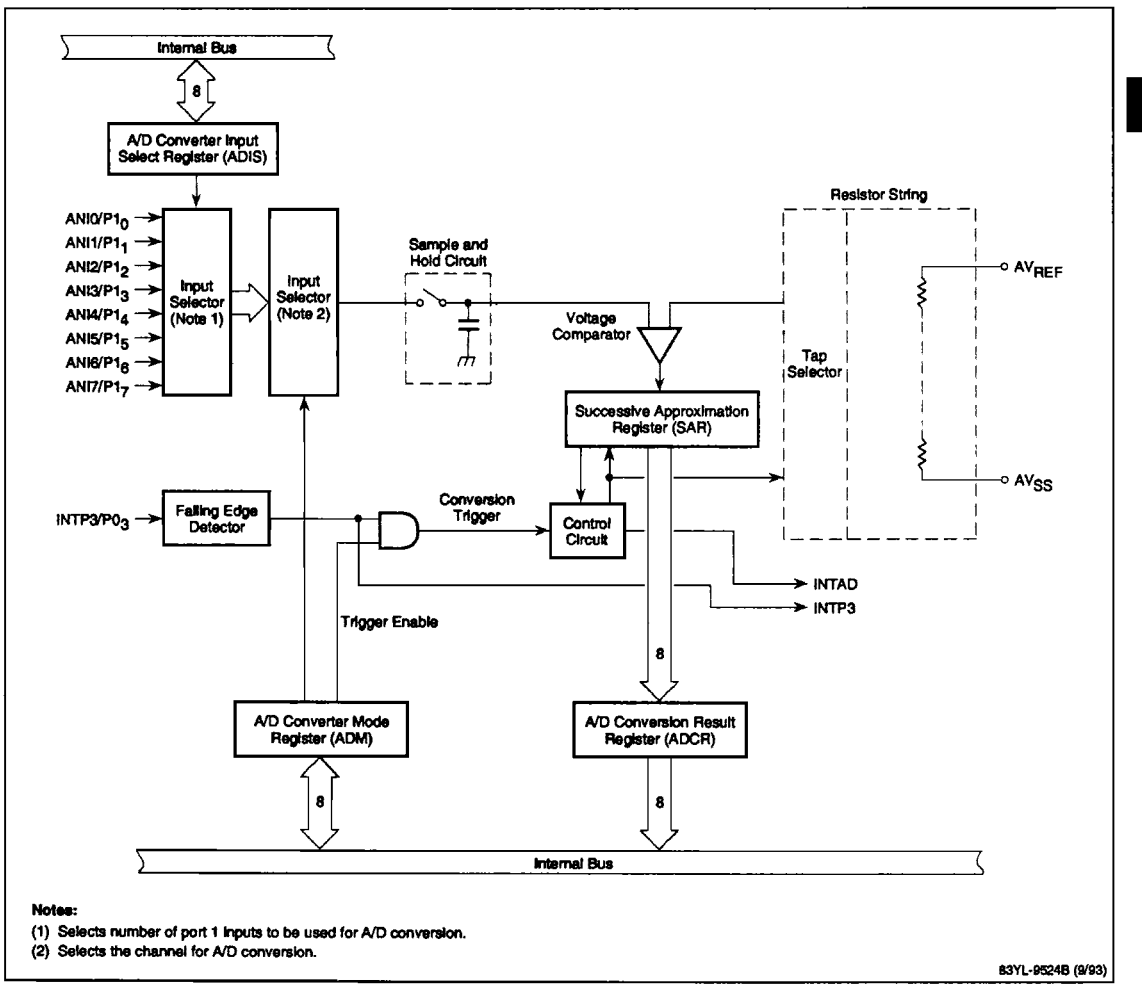
A/D Converter

The μPD78044 family's analog-to-digital converter (figure 5) uses the successive-approximation method for converting one of eight multiplexed analog inputs into 8-bit digital data. The minimum conversion time per input is 38.1 μs at 4.19-MHz operation.

The A/D converter input select register (ADIS) selects the number of inputs that are used in A/D conversion. The remaining inputs are used as ports. The analog input to be converted is selected by programming the A/D converter mode register (ADM). Conversion is started by external interrupt INTP3, or by writing to the ADM register. When conversion is completed, the results are stored in the A/D conversion result register (ADCR) and an INTAD interrupt is generated.

If the A/D converter was started by an external interrupt, it stops after the interrupt is generated. If the A/D converter was started by software, it repeats the conversion until new data is written to the ADM register.

Figure 5. A/D Converter



Notes:
(1) Selects number of port 1 inputs to be used for A/D conversion.
(2) Selects the channel for A/D conversion.

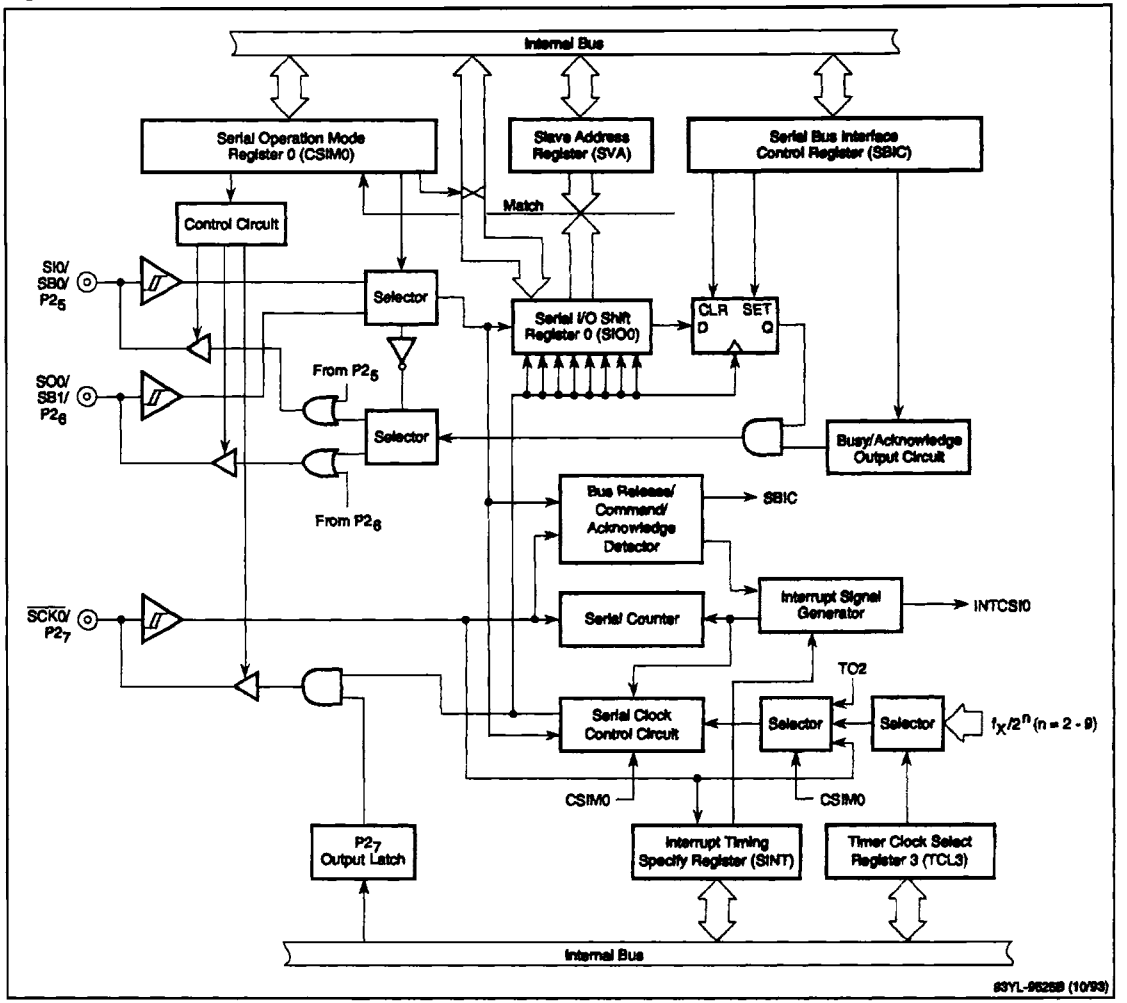
83YL-9524B (9/93)

3e

Serial Interface 0

Serial interface 0 is an 8-bit, clock-synchronous interface. It can be operated in three-wire serial I/O mode, NEC serial bus interface (SBI) mode, or two-wire serial I/O mode. The serial clock can be provided from one of eight internal clocks, the output of 8-bit timer register 2, or external clock line $\overline{SCK0}$. See figure 6.

Figure 6. Serial Interface 0

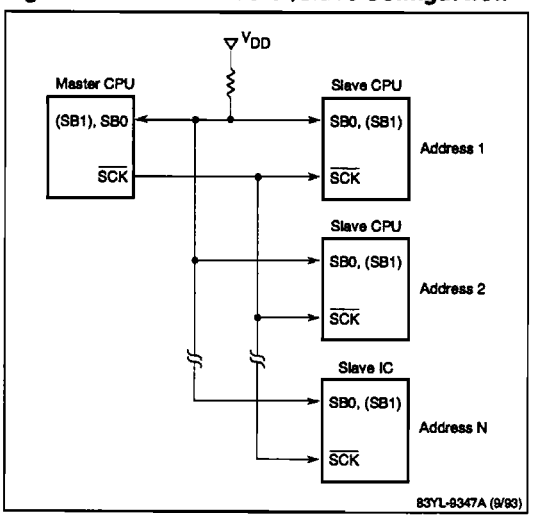


Three-Wire Interface. In the three-wire serial I/O mode, the 8-bit shift register (SIO0) is loaded with a data byte and eight clock pulses are generated. The clock pulse falling edges shift the data byte out to the SO0 line (either MSB or LSB first), while the rising edges shift data in from the SI0 line, providing full-duplex operation. The INTCSI0 interrupt is generated after each 8-bit transfer.

SBI Interface. The NEC SBI mode is a two-wire, high-speed, proprietary serial interface available on most devices in the NEC μPD75xxx and μPD78xxx families. Devices are connected in a master/slave configuration. See figure 7. There is only one master device at a time; all others are slaves. The master sends addresses, commands, and data over one of the serial bus lines (SB0 or SB1) using a fixed hardware protocol synchronized with the $\overline{SCK0}$ line.

Each slave device of the μPD78044 family can be programmed to respond in hardware to any one of 256 addresses set in its slave address register (SVA). There are also 256 commands and 256 data types. Since all commands are user definable, many software protocols, simple or complex, can be defined. It is even possible to develop commands that change a slave into a master and the previous master into a slave.

Figure 7. SBI Mode Master/Slave Configurtion



Two-Wire Interface. The two-wire serial I/O mode provides half-duplex operation using either the SB0 or SB1 line and the $\overline{SCK0}$ line. Communication format and handshaking can be handled in software by controlling the output levels of the data and clock lines between transfers. For data transmission, when 8-bit shift register (SIO0) is loaded with a data byte and eight clock pulses are generated. The falling edges shift the data byte out either the SB0 or SB1 line, MSB first. In addition, this data byte is also shifted back into SIO0 on the rising pulse edges providing a means of verifying that the transmission was correct.

For data reception, the SIO0 register is preloaded with the value FFH. As this data value is shifted out on the falling edge of the serial clock, it disables the n-channel open-drain driver. This allows the receive data to be driven onto the serial line and shifted into the SIO0 register on the rising edge of the serial clock. The INTCSI0 interrupt is generated after each 8-bit transfer.

3e

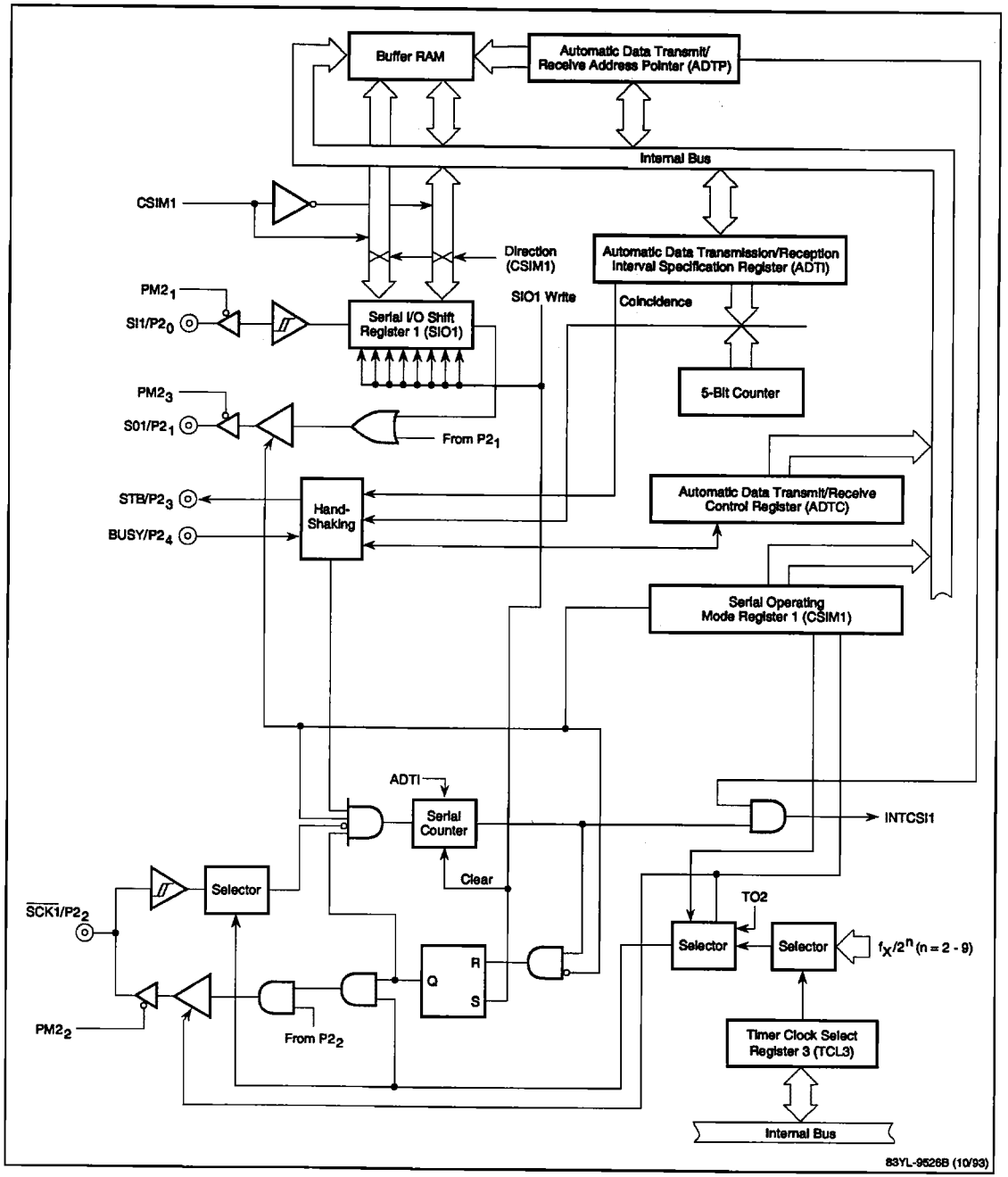
Serial Interface 1

Serial interface 1 is also an 8-bit, clock-synchronous interface (figure 8). It can be operated in either a three-wire serial I/O mode or a three-wire serial I/O mode with automatic transmit/receive. The serial clock can also be provided from one of eight internal clocks (common clock for both interfaces), the output of 8-bit timer register 2, or the external clock line $\overline{SCK1}$.

Three-Wire. In the three-wire serial I/O mode, the 8-bit shift register (SIO1) is loaded with a data byte and eight clock pulses are generated. The clock pulse falling edges shift the data byte out of the SO1 line (MSB or LSB first) while the rising edges shift the data in from the SI1 line, providing full-duplex operation. The INTCSI1 interrupt is generated after each 8-bit transfer.

Three-Wire With Auto Xmt/Rcv. In the three-wire serial I/O mode with automatic transmit/receive, up to 64 data bytes can be transferred with minimal CPU overhead. The data to be transmitted and received is stored in the buffer RAM. Handshaking over the BUSY input line or the strobe (STB) output line, or both, can be selected by the program. Error detection of bit drift due to noise is available for each byte transferred when using the BUSY input line. This automatic transmit/receive mode is ideally suited for transferring data to/from external peripheral devices such as on-screen display (OSD) and LSC controller/driver devices.

Figure 8. Serial Interface 1



While in three-wire serial I/O mode with automatic data transfer, the interface can be operated full duplex or transmit only in single or repetitive operation. In full duplex, a data byte is transferred from the first location in the buffer RAM and shifted out the SO1 line (MSB or LSB first) while the received data is shifted in the SI1 line and stored back in the first buffer location. After the preset number of bytes have been transferred, the INTCSI1 interrupt is generated.

In single-operation transmit mode, the preset number of bytes from the buffer RAM are transmitted out the SO1 line (MSB or LSB first) and the INTCSI1 interrupt is generated after all bytes have been transferred. In repetitive-operation transmit mode, data in the buffer is transmitted repeatedly.

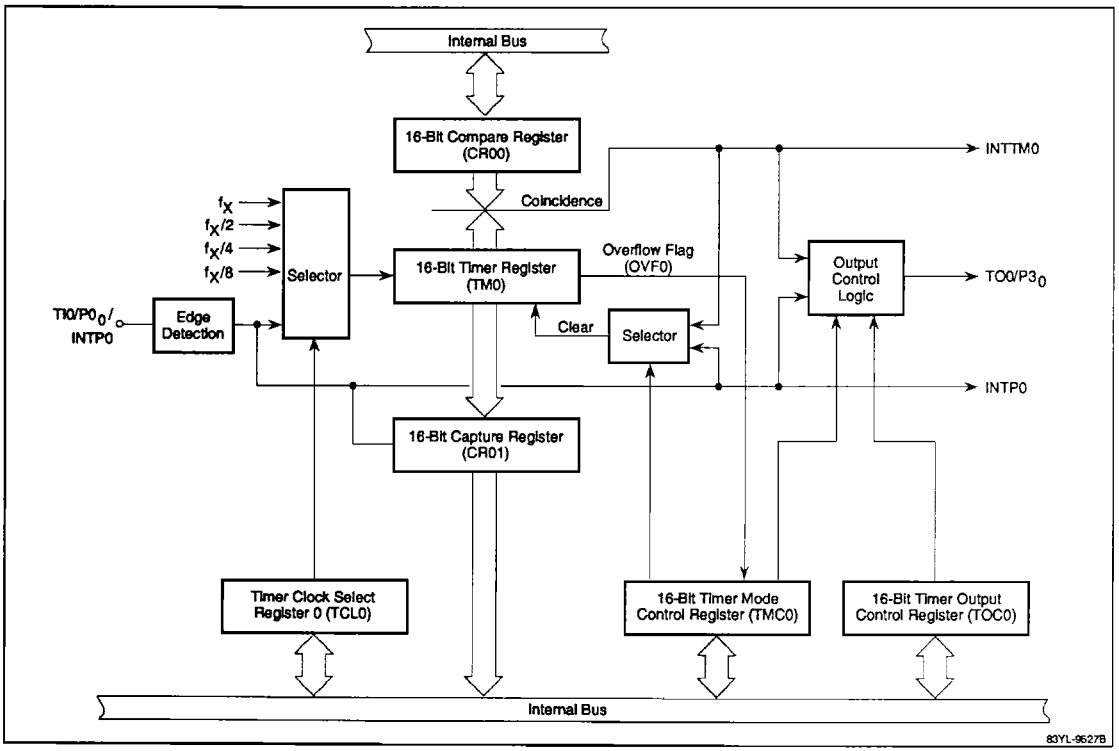
Timers

The μPD78044 family has a 16-bit timer/event counter, two 8-bit timer/event counters (combinable for 16-bit operation), a 6-bit up/down counter, a watch timer, and a watchdog timer. All except the up/down counter can be programmed to count a number of prescaled values of the main system clock. The watch timer can also count the subsystem clock. All timer/event counters and the up/down counter can count external events.

16-Bit Timer/Event Counter 0. Timer/event counter 0 (figure 9) includes a 16-bit counter (TM0), a 16-bit compare register (CR00), a 16-bit capture register (CR01), and a timer output (TO0). Timer 0 can be used (1) as an interval timer, (2) to count external events on the timer input (TI0) pin, (3) to output a programmable square wave or a 14-bit pulse-width modulated output, or (4) to measure pulse widths.

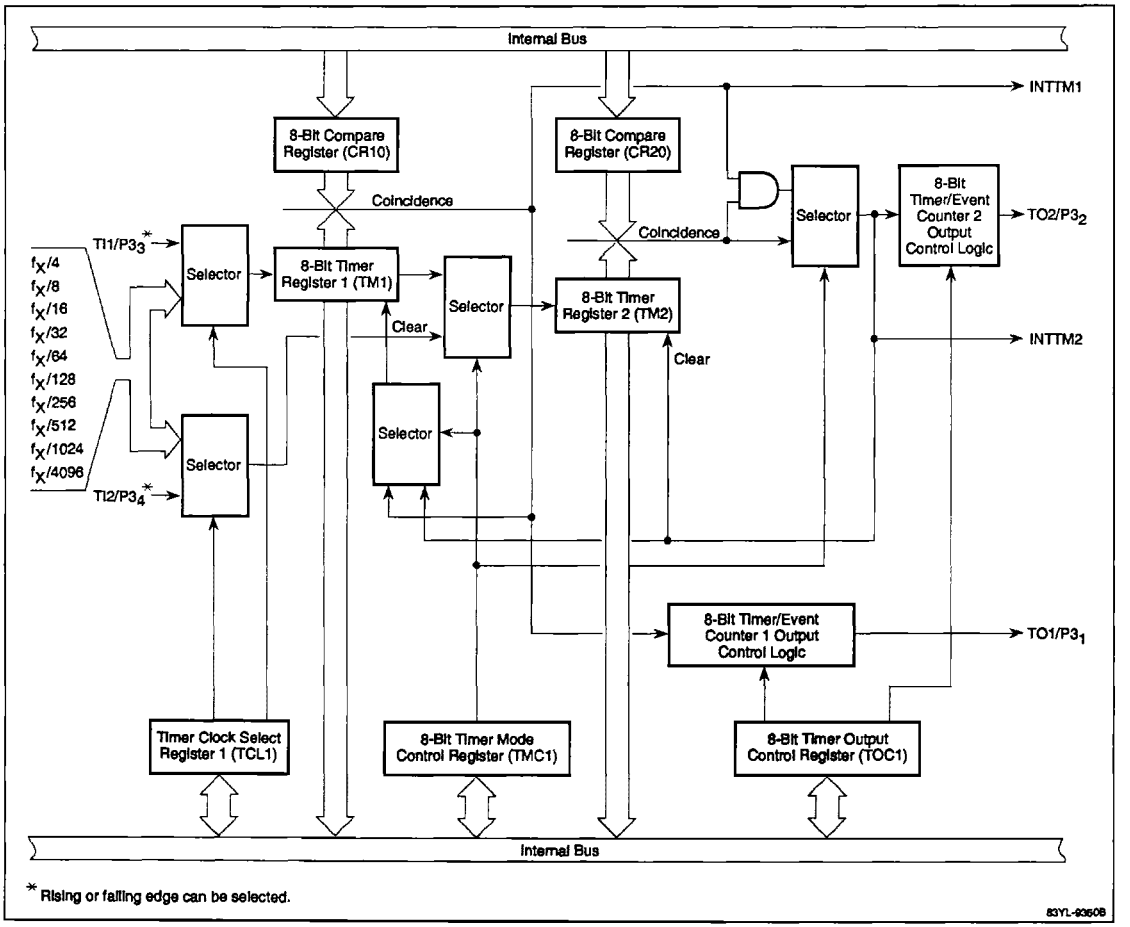
3e

Figure 9. 16-Bit Timer/Event Counter 0



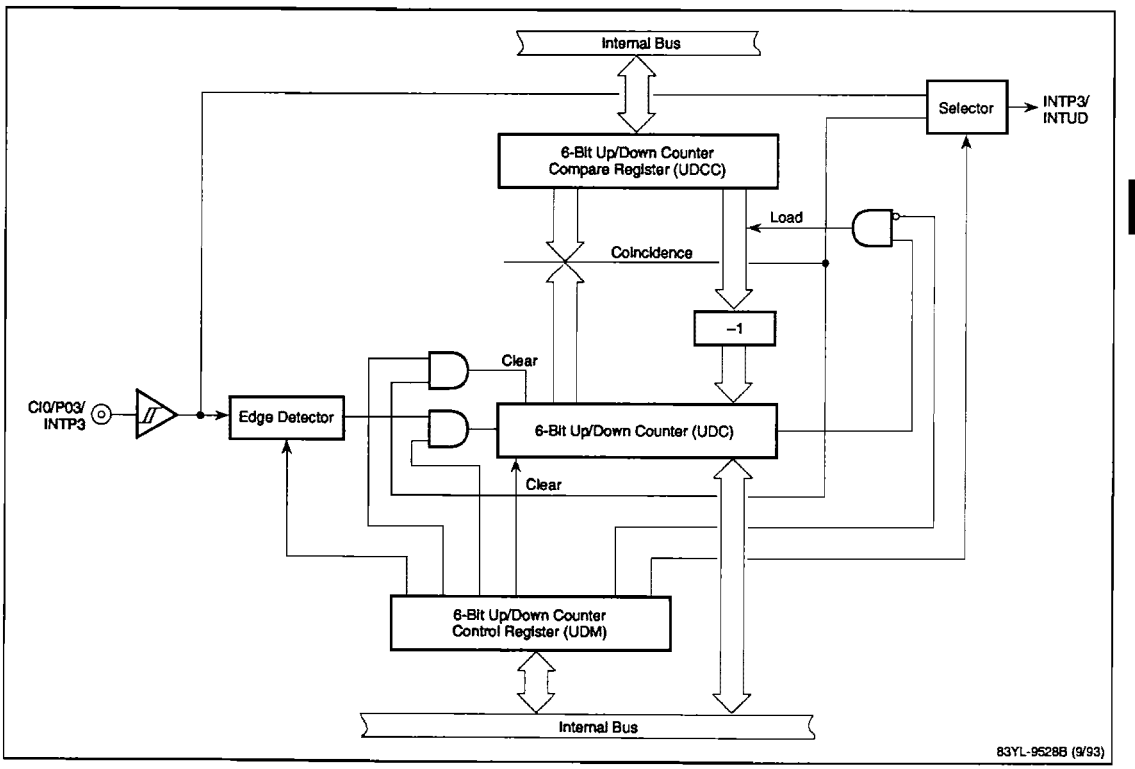
8-Bit Timer/Event Counters 1 and 2. Timer/event counters 1 and 2 (figure 10) each consists of an 8-bit timer register (TM1 or TM2), an 8-bit compare register (CR10 or CR20), and a timer output control logic (TO1 or TO2). The timers are controlled by registers TCL1, TMC1, and TOC1 via five selectors. Timer/event counters 1 and 2 each can be used as an 8-bit interval timer, to count external events on timer input pin TI1 or TI2, or to output a programmable square wave. Also, timers 1 and 2 can be combined as a 16-bit timer/event counter and used as a 16-bit interval timer, to count external events on TI1, or to output a programmable square wave on TO2.

Figure 10. 8-Bit Timer/Event Counters 1 and 2



6-Bit Up/Down Counter. The up/down counter (figure 11) includes counter UDC and compare register UDCC. It counts external events (up or down) on the counter input pin (CI0) and generates an interrupt (INTUD) when the count matches the compare register. The counter is loaded with –1 (down-count mode) or cleared (up-count mode) upon interrupt generation.

Figure 11. 6-Bit Up/Down Counter



Watch Timer 3. Watch timer 3 (figure 12) is a 5-bit timer that can be used as a time source to keep track of time of day, to release the STOP or HALT mode at regular intervals, or to initiate any other task that must be performed at regular intervals. When driven by the subsystem clock, the watch timer continues to operate in the STOP mode.

The watch timer can function as both a watch timer and an interval timer simultaneously. In watch timing, interrupt request INTWT (not a vectored interrupt) can be generated using the main system clock every 0.5 or 1.0 second or by using the subsystem clock every 0.5 or 0.25 second.

In interval timing, vectored interrupt request INTTM3 is generated at preselected time intervals. With a 4.19-MHz main system clock, the following time intervals can be selected: 978 μs; 1.96, 3.91, 7.82, 15.6, or 31.3 ms. With a 32.768-kHz subsystem clock, the following time intervals can be selected: 488 or 978 μs; 1.96, 3.91, 7.82, or 15.6 ms.

Watchdog Timer. The watchdog timer (figure 13) can also perform interval timing. As a watchdog timer, it protects against inadvertent program run-away. It can be selected to generate a nonmaskable interrupt (INTWDT), which vectors to address 0004H, or to generate an internal reset signal, which vectors to the restart address 0000H if the timer is not cleared by the program before it overflows. Eight program-selectable intervals based on the main system clock are available. With a 4.19-MHz main system clock, they are 0.489, 0.978, 1.96, 3.91, 7.82, 15.6, 31.3, and 125 ms. Once initialized and started, the timer cannot change modes and can be stopped only by an external reset.

In interval timing, maskable interrupts (INTWDT), which vector to address 0004H, are generated repeatedly at a preset interval. The time intervals available are the same as in the watchdog timer mode.

Programmable Clock Output

The μPD78044 family has a programmable clock output (PCL) that can be used as carrier output for remote controlled transmissions or as clock output for peripheral devices. The main system clock (f_X) divided by 8, 16, 32, 64, 128, or 256 or the subsystem clock (f_{XT}) can be output on the PCL pin. With a 4.19-MHz main system clock, the following frequencies are available: 524, 262, 131, 65.5, 32.7, and 16.4 kHz. With a 32.768-kHz subsystem clock, 32.768 kHz is also available. See figure 14.

Buzzer Output

The μPD78044 family also has a programmable buzzer output (BUZ). The buzzer output frequency can be programmed to equal the main system clock (f_X) divided by 1024, 2048, or 4096. With a 4.19-MHz main system clock, the buzzer can be set to 4.1, 2.0, or 1.0 kHz. See figure 15.

FIP Controller/Driver

The μPD78044 family can directly drive up to 34 FIP (fluorescent indicator panel) display output lines of which 9 to 24 segments and 2 to 16 digits can be selected through software. The number of digits is selected by display mode register 0 (DSPM0) and the number of segments by display mode register 1 (DSPM1). If an attempt is made to select a total of more than 34 digit and segment outputs, the digit selection will take priority. Any unused pins can be used as outputs or I/O depending on the type.

There are 48 bytes of display data RAM mapped from FA50H to FA7FH. Each display memory bit corresponds to a specific display element. Any bits not used for FIP display can be used for general purpose.

Segment and digit signal output is automatically controlled by a DMA operation from the FIP controller to the display data RAM. The display cycle period is $1024/f_X$ or $2048/f_X$. Register DSPM1 selects the display cycle and one of eight intensity levels. The on-chip circuitry controls the intensity level by varying the driving signal pulse width.

The on-chip circuitry has been designed to allow easy interface to a keyboard. At the end of the display cycle, vectored interrupt INTKS is generated and the controller outputs key scan data (ports 11 and 12) on segment output pins FIP18 to FIP33. Flag KSF indicates key scan or display timing to the key scan software routine.

Pulldown resistors for all FIP lines are mask-selected and can be connected to V_{LOAD} or V_{SS}. Pulldown resistors for FIP0 to FIP17 lines are incorporated in the μPD78P044 and are connected to V_{LOAD}.

Figure 12. Watch Timer 3

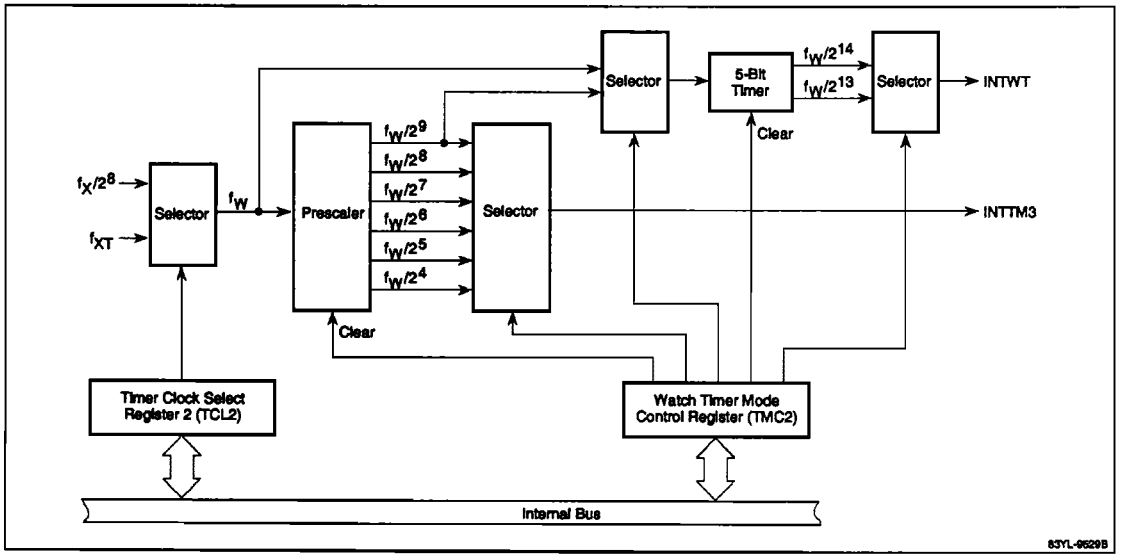


Figure 13. Watchdog Timer

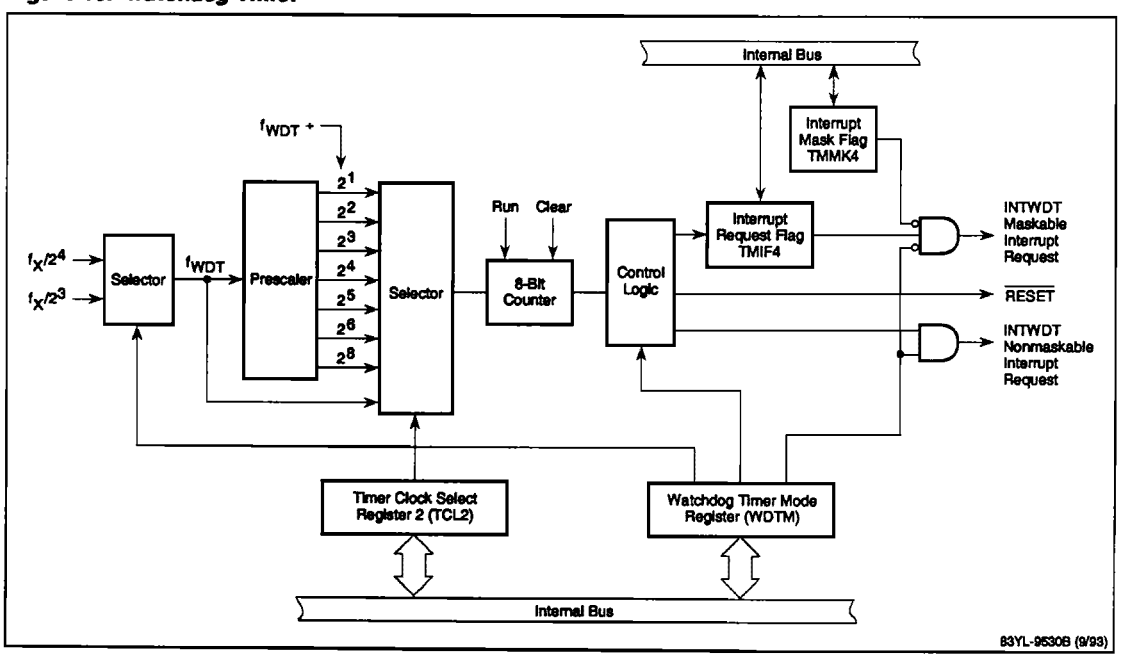


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Figure 14. Programmable Clock Output

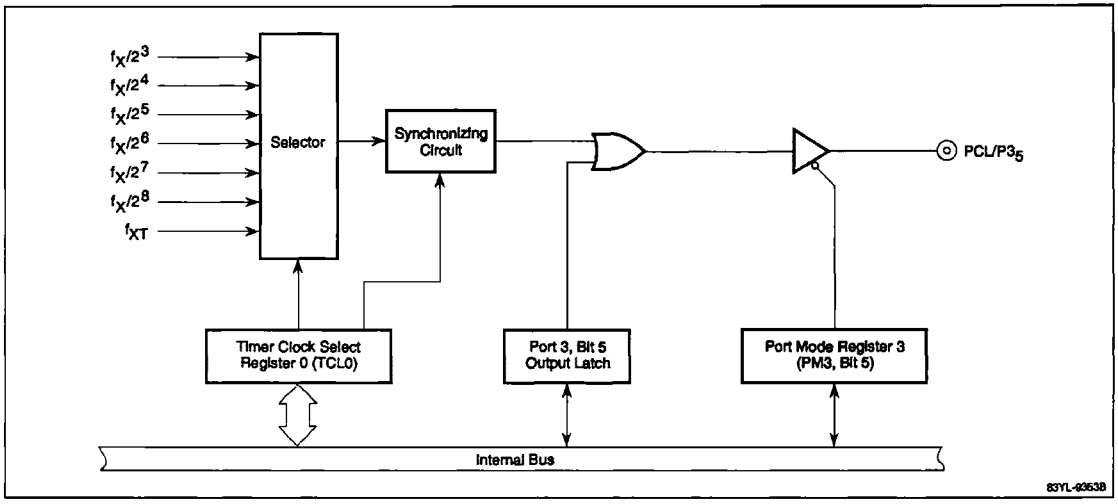


Figure 15. Buzzer Output

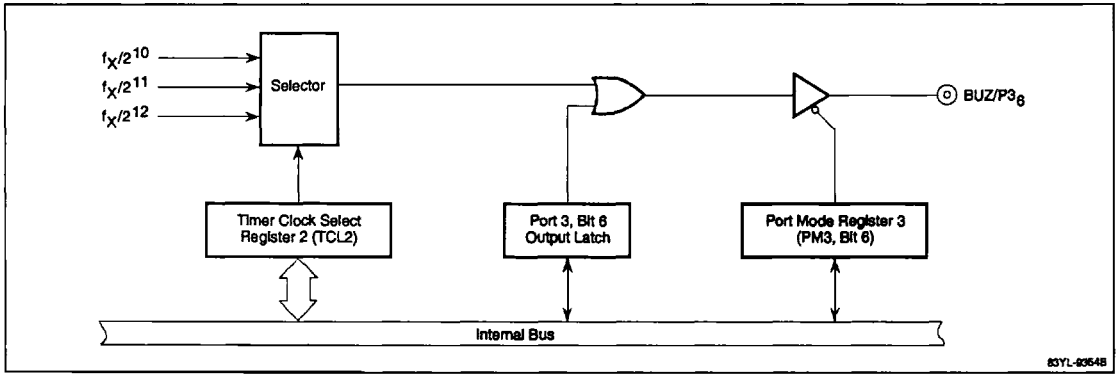
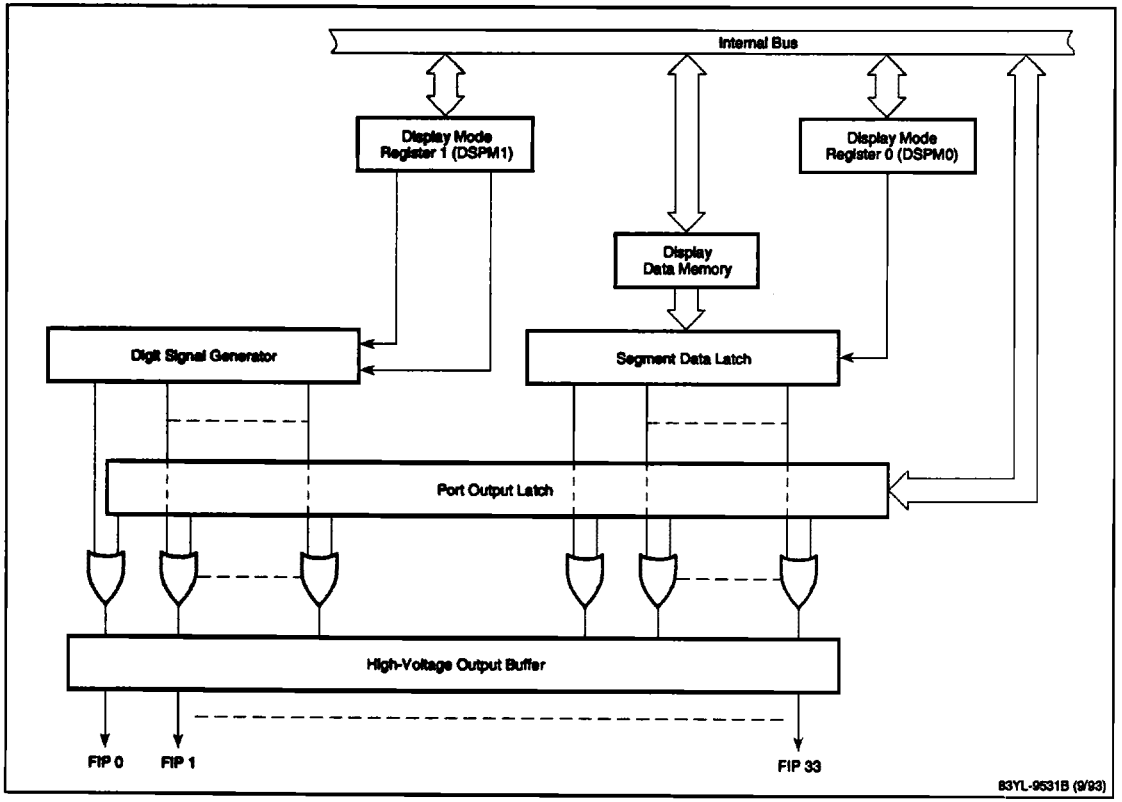


Figure 16. FIP Controller/Driver



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Interrupts

The μPD78044 family has 14 maskable hardware interrupt sources: four are external, nine are internal, and one (INTP3/INTUD) can be set for either external or internal. Thirteen of them cause a vectored interrupt; one testable input-only generates an interrupt request. All 14 maskable interrupts can be used to release the HALT mode except INTP0 (when SCS = 0) and INTKS; all except INTKS and INTP0 can release the STOP mode.

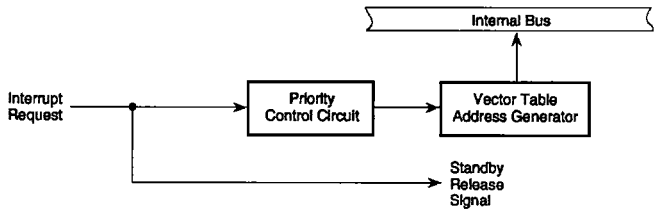
In addition, there is one nonmaskable interrupt from the watchdog timer, one software interrrupt, and a RESET interrupt. The watchdog timer overflow interrupt (interrupt vector table address 0004H) can be initialized to be a nonmaskable interrupt or the highest default priority maskable interrupt. The software interrupt generated by the BRK instruction is not maskable. See table 3 and figure 17.

Table 3. Interrupt Sources and Vector Addresses

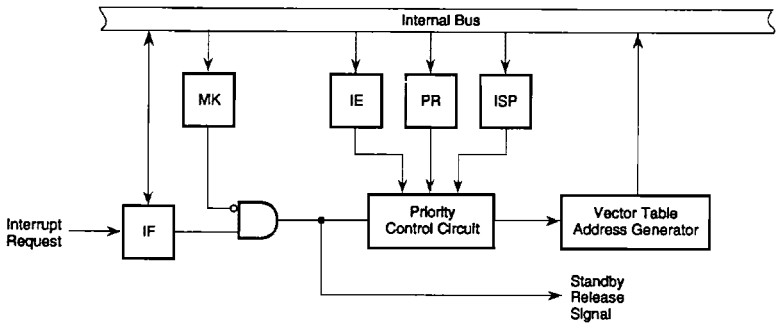
Type of Request	Default Priority	Signal Name	Interupt Source	Location	Vector Address	Interrupt Configuration
Restart	—	RESET	$\overline{\text{RESET}}$ input pin	External	0000H	—
		INTWDT	Watchdog timer overflow (when reset mode selected)	Internal		
Nonmaskable		INTWDT	Watchdog timer overflow (when nonmaskable interrupt selected)	Internal	0004H	A
Maskable	0	INTWDT	Watchdog timer overflow (when interval timer selected)	Internal	0004H	B
	1	INTP0	External interrupt edge detection	External	0006H	C
	2	INTP1	External interrupt edge detection	External	0008H	D
	3	INTP2	External interrupt edge detection	External	000AH	D
	4	INTP3	External interrupt edge detection	External	000CH	D
		INTUD	Up/down counter coincidence signal	Internal		B
	5	INTCSI0	End of clocked serial interface 0 transfer	Internal	000EH	B
	6	INTCSI1	End of clocked serial interface 1 transfer	Internal	0010H	B
	7	INTTM3	Watch timer reference time interval signal	Internal	0012H	B
	8	INTTM0	16-bit timer/event counter coincidence signal	Internal	0014H	B
	9	INTTM1	8-bit timer/event counter 1 coincidence signal	Internal	0016H	B
	10	INTTM2	8-bit timer/event counter 2 coincidence signal	Internal	0018H	B
	11	INTAD	End of A/D conversion	Internal	001AH	B
	12	INTKS	Key scan interrupt generated by FIP controller	Internal	001CH	B
Software		—	BRK instruction	Internal	003EH	E
Test input		INTWT	Clock timer overflow	Internal	—	F

Figure 17. Interrupt Configuration

Type A: Internal nonmaskable interrupt



Type B: Internal maskable interrupt



Type C: External maskable interrupt (INTP0)

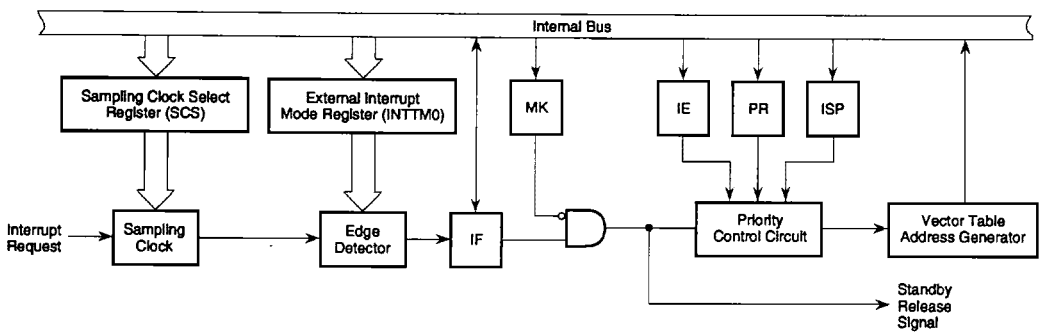


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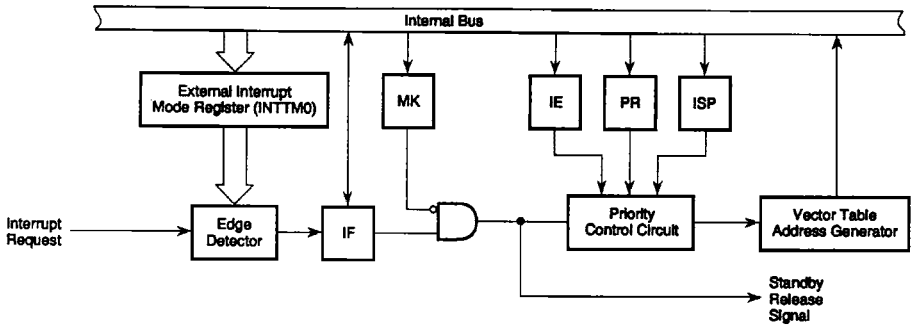
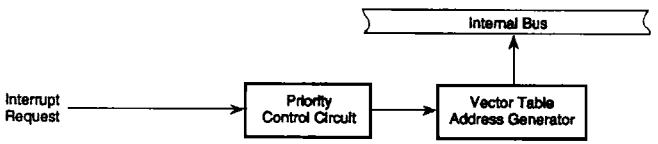
Figure 17. Interrupt Configuration (cont)

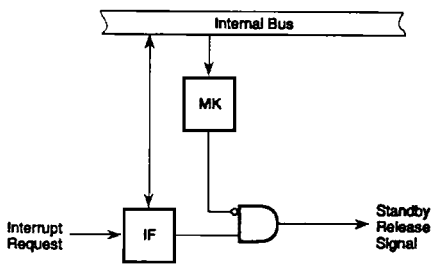
Type D: External maskable interrupt (except INTP0)



Type E: Software interrupt



Type F: Test input



Abbreviations:

IF: Interrupt request flag
IE: Interrupt enable flag
ISP: In-service priority flag
MK: Interrupt mask flag
PR: Priority specify flag

83YL-80668 (2)

Interrupt Servicing. The μPD78044 family provides two levels of programmable hardware priority control and services all interrupt requests except the testable interrupt (INTWT) using vectored interrupts. The programmer can choose the priority of servicing each maskable interrupt by the interrupt control registers.

Interrupt Control Registers. The μPD78044 family has three 16-bit interrupt control registers. The interrupt request flag register (IF0) contains an interrupt request flag for each interrupt. The interrupt mask register (MK0) is used to enable or disable any individual interrupt. The priority flag register (PR0) can specify a high or a low priority level for each interrupt except the testable interrupt (INTWT).

Three other 8-bit registers are associated with interrupt processing. The external interrupt mode register (INTM0) selects a rising or falling edge (or both) as the valid edge for external interrupts INTP0, INTP1, and INTP2 (INTP3 is always falling edge). The sampling clock select register (SCS) selects a sampling clock for the noise eliminator circuit on external interrupt INTP0.

The IE and ISP bits of the program status word also control interrrupts. If the IE bit is zero, all maskable interrupts are disabled. The IE bit can be set or cleared by the EI or DI instruction, respectively, or by directly writing to the PSW. The IE bit is cleared each time an interrupt is accepted. The ISP bit is used by hardware to hold the priority level flag of the interrupt being serviced.

Interrupt Priority. If the watchdog timer overflow interrupt (INTWDT) has been initialized to be a nonmaskable interrupt, it has priority over all other interrupts. Two hardware-controlled priority levels are available for all maskable interrupts that generate a vectored interrupt (that is, all except the testable interrupt). Either a high or a low priority level can be assigned by software to each of the maskable interrupts.

Interrupt requests of the same priority or a priority higher than the processor's current priority level are held pending until interrupts in the current service routine are enabled by software or until one instruction has been executed after returning from the current service routine. Interrupt requests of a lower priority are always held pending until one instruction has been executed after returning from the current service routine.

The default priorities in table 3 are fixed by hardware; they are effective only when necessary to choose between two interrupt requests of the same software-assigned priority. For example, after the completion of a high-priority routine, if two interrupts of the same software priority were pending.

The software interrupt, initiated by the BRK instruction, is executed regardless of the procesor's priority and the state of the IE bit. It does not alter the processor's priority.

Vectored Interrupt Servicing. When a vectored interrupt is acknowledged, the program status word and the program counter are saved on the stack, the processor's priority is set to that specified for the interrupt, the IE bit in the PSW is set to zero, and the routine whose address is in the interrupt vector table is entered. At the completion of the service routine, the RETI instruction (RETB instruction for the software interrupt) reverses the process and the μPD78044 family microcomputer resumes the interrupted routine.

3e

Standby Modes

The HALT, STOP, and data retention modes reduce power consumption when CPU action is not required.

The HALT mode is entered by executing a HALT instruction while the CPU is operating from the main system or subsystem clock. In HALT mode, the CPU clock is stopped while the main system and the subsystem clock continue to run. The HALT mode is released by any unmasked interrupt request (except INTP0 if register SCS = 0 and INTKS), a nonmaskable interrupt request, an unmasked test input, or an external reset pulse.

Power consumption may be further reduced by the STOP mode. The STOP mode is entered by executing a STOP instruction while operating from the main system clock. In STOP mode, the main system clock input pin X1 is internally grounded, stopping both the CPU and the peripheral hardware clock. The STOP mode is released by any unmasked interrupt request except INTP0 and INTKS, a nonmaskable interrupt request, an unmasked test input, or an external reset pulse.

Any peripheral using the main oscillator as a clock source will also be disabled in the STOP mode and interrupts from such a peripheral cannot be used to exit the STOP mode. Table 4 summarizes the HALT and STOP standby modes.

When exiting the STOP mode, a wait time occurs before the CPU begins code execution to allow the main system clock oscillator circuit to stabilize. The oscillation stabilization time is selected by programming the OSTS register with one of five values before entering the STOP mode and ranges from $2^{12}/f_X$ to $2^{17}/f_X$ seconds.

Table 4. Standby Mode Operation Status

Item	HALT Mode	STOP Mode
Setting instruction	HALT instruction	STOP instruction
System clock when setting	Main system or subsystem clock	Main system clock
Clock oscillator	Main system and subsystem clocks can oscillate; CPU clock is stopped.	Subsystem clock can oscillate; CPU and main system clocks are stopped.
CPU	Operation stopped	Operation stopped
Ports	Maintain previous state	Maintain previous state
16-bit timer/event counter	Operational from main system clock	Operation stopped
8-bit timer/event counters	Operational from main system clock or with TI1 and TI2 selected as the count clock	Operational only with TI1 and TI2 as count clock
6-bit up/down counter	Operable	Operable
FIP controller/driver	Inoperable	Inoperable
Watch timer	Operational from main system clock or with f_{XT} as count clock	Operational only with f_{XT} as count clock
Watchdog timer	Operational from main system clock	Operation stopped
Serial interface 0	Operational from main system clock or with external clock	Operational only with external clock
Serial interface 1	Operational from main system clock or with external clock; no automatic transmit/receive mode	Operational only with external clock; no automatic transmit/receive mode
A/D converter	Operational from main system clock	Operation stopped
External interrupts	Operational except for INTP0 when its sampling clock is based on the CPU clock	INTP0 not operational; INTP1 to INTP3 operational

Once in the STOP mode, power consumption can be further minimized by lowering the power supply voltage V_{DD} to 2 volts. This places the device in the data retention mode. The contents of internal RAM and the registers are retained. This mode is released by first raising V_{DD} to the proper operating range and then releasing the STOP mode.

External Reset

The μPD78044 family is reset by taking the $\overline{\text{RESET}}$ pin low or by an overflow of the watchdog timer (if enabled). The $\overline{\text{RESET}}$ input pin is a Schmitt trigger input with hysteresis characteristics to protect against spurious system resets by noise. On power-up, the $\overline{\text{RESET}}$ pin must remain low for 10 μs minimum after the power supply reaches its operating voltage.

There is no functional difference between an external reset and an internal reset caused by watchdog timer overflow. In both cases, the main system clock oscillation is stopped and the subsystem clock oscillation continues. During reset, the program counter is loaded with the address in the reset vector (addresses 0000H, 0001H). Once the reset is cleared and the oscillation stabilization time of $2^{17}/f_X$ has elapsed, program execution starts at that address.