

SN55121, SN75121 DUAL LINE DRIVERS

D1334, SEPTEMBER 1973 REVISED SEPTEMBER 1986

- Designed for Digital Data Transmission over 50-Ω to 500-Ω Coaxial Cable, Strip Line, or Twisted Pair
- High-Speed
 $t_{pd} = 20 \text{ ns Max at } C_L = 15 \text{ pF}$
- TTL Compatible With Single 5-V Supply
- 2.4-V Output at $I_{OH} = -75 \text{ mA}$
- Uncommitted Emitter-Follower Output Structure for Party-Line Operation
- Short-Circuit Protection
- AND-OR Logic Configuration
- Designed for Use With Triple Line Receivers SN55122, SN75122
- Designed to Be Interchangeable With Signetics N8T13

description

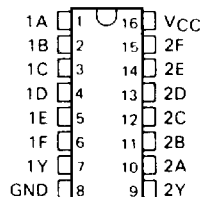
The SN55121 and SN75121 dual line drivers are designed for digital data transmission over lines having impedances from 50 to 500 ohms. They are also compatible with standard TTL logic and supply voltage levels.

The low-impedance emitter-follower outputs of the SN55121 and SN75121 will drive terminated lines such as coaxial cable or twisted pairs. Having the outputs uncommitted allows wired-OR logic to be performed in party-line applications. Output short-circuit protection is provided by an internal clamping network which turns on when the output voltage drops below approximately 1.5 V. All of the inputs are in conventional TTL configuration and the gating can be used during power-up and power-down sequences to ensure that no noise is introduced to the line.

The SN55121 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN75121 is characterized for operation from 0°C to 70°C .

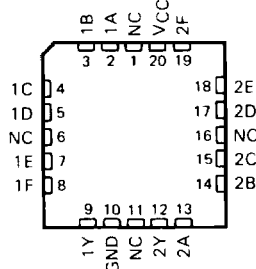
SN55121 . . . J PACKAGE SN75121 . . . D, J, OR N PACKAGE

(TOP VIEW)



SN55121 . . . FK PACKAGE

(TOP VIEW)



NC - No internal connection

FUNCTION TABLE

INPUTS						OUTPUT
A	B	C	D	E	F	Y
H	H	H	H	X	X	H
X	X	X	X	H	H	H
All other input combinations						L

H - high level
L - low level
X - irrelevant

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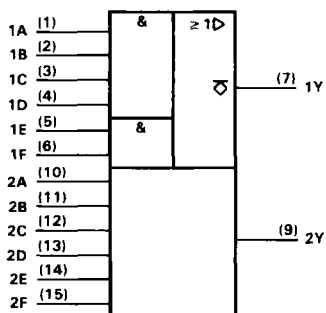
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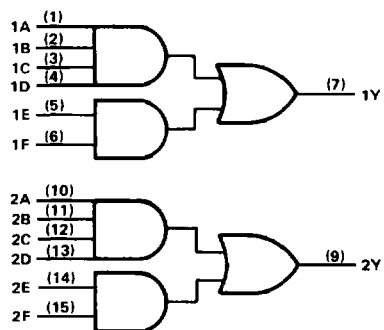
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SN55121, SN75121 **DUAL LINE DRIVERS**

logic symbol†

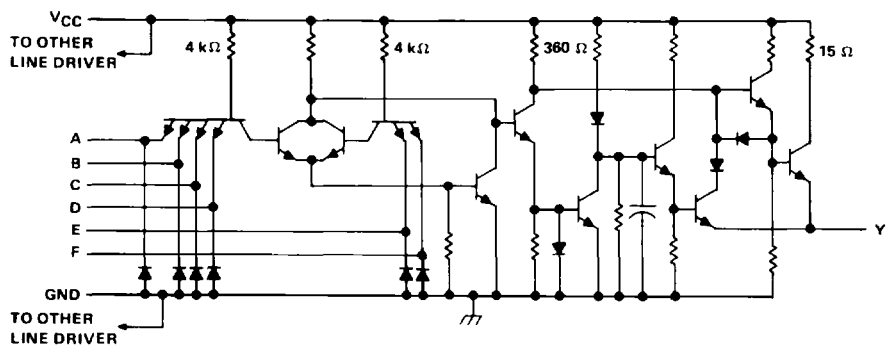


logic diagram (positive logic)



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

schematic (each driver)



All resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	SN55121	SN75121	UNIT
Supply voltage, V_{CC} (see Note 1)	6	6	V
Input voltage	6	6	V
Output voltage	6	6	V
Continuous total power dissipation (see Note 2)	See Dissipation Rating Table		
Operating free-air temperature range	-55 to 125	0 to 70	°C
Storage temperature range	-65 to 150	-65 to 150	°C
Case temperature for 60 seconds: FK package	260		°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package		260	°C

- NOTES: 1. All voltage values are with respect to both ground terminals connected together.
2. In the FK and J packages, SN55121 chips are either silver glass or alloy mounted and SN75121 chips are glass mounted.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	—
FK	1375 mW	11.0 mW/°C	880 mW	275 mW
J (SN55121)	1375 mW	11.0 mW/°C	880 mW	275 mW
J (SN75121)	1025 mW	8.2 mW/°C	656 mW	—
N	1150 mW	9.2 mW/°C	736 mW	—

recommended operating conditions

	SN55121			SN75121			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.75	5	5.25	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			2			V
Low-level input voltage, V_{IL}			0.8			0.8	V
High-level output current, I_{OH}			-75			-75	mA
Operating free-air temperature, T_A	-55		125	0		70	°C



SN55121, SN75121 DUAL LINE DRIVERS

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
V_{IK} Input clamp voltage	$V_{CC} = 5\text{ V}$, $I_I = -12\text{ mA}$		-1.5	V
$V_{(BR)}$ Input breakdown voltage	$V_{CC} = 5\text{ V}$, $I_I = 10\text{ mA}$	5.5		V
V_{OH} High-level output voltage	$V_{IH} = 2\text{ V}$, $I_{OH} = -75\text{ mA}$, See Note 3	2.4		V
I_{OH} High-level output current	$V_{CC} = 5\text{ V}$, $V_{IH} = 4.5\text{ V}$, $V_{OH} = 2\text{ V}$, $T_A = 25^\circ\text{C}$, See Note 3	-100	-250	mA
I_{OL} Low-level output current	$V_{IL} = 0.8\text{ V}$, $V_{OL} = 0.4\text{ V}$, See Note 3		-800	μA
$I_{O(off)}$ Off-state output current	$V_{CC} = 3\text{ V}$, $V_O = 3\text{ V}$		500	μA
I_{IH} High-level input current	$V_I = 4.5\text{ V}$		40	μA
I_{IL} Low-level input current	$V_I = 0.4\text{ V}$	-0.1	-1.6	mA
I_{OS} Short-circuit output current [†]	$V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$		-30	mA
I_{CCH} Supply current, outputs high	$V_{CC} = 5.25\text{ V}$, All inputs at 2 V, Outputs open		28	mA
I_{CCL} Supply current, outputs low	$V_{CC} = 5.25\text{ V}$, All inputs at 0.8 V, Outputs open		60	mA

[†]Not more than one output should be shorted at a time.

NOTE 3: The output voltage and current limits are valid for any appropriate combination of high and low inputs specified by the function table for the desired output.

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output	$R_L = 37\ \Omega$, $C_L = 15\text{ pF}$, See Figure 1		11	20	ns
t_{PHL} Propagation delay time, high-to-low-level output	$R_L = 37\ \Omega$, $C_L = 1000\text{ pF}$, See Figure 1		8	20	ns
t_{PLH} Propagation delay time, low-to-high-level output	$R_L = 37\ \Omega$, $C_L = 1000\text{ pF}$, See Figure 1		22	50	ns
t_{PHL} Propagation delay time, high-to-low-level output	$R_L = 37\ \Omega$, $C_L = 1000\text{ pF}$, See Figure 1		20	50	ns

PARAMETER MEASUREMENT INFORMATION

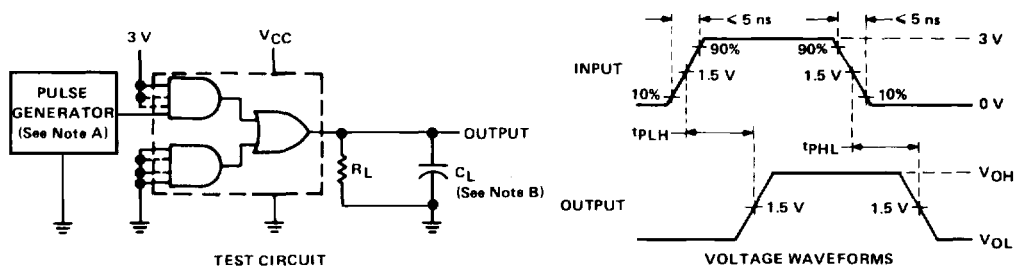


FIGURE 1. SWITCHING TIMES

NOTES: A. The pulse generators have the following characteristics: $Z_0 \approx 50\ \Omega$, $t_w = 200\text{ ns}$, duty cycle $\leq 50\%$, PRR $\leq 500\text{ kHz}$.
B. C_L includes probe and jig capacitance.

TYPICAL CHARACTERISTICS

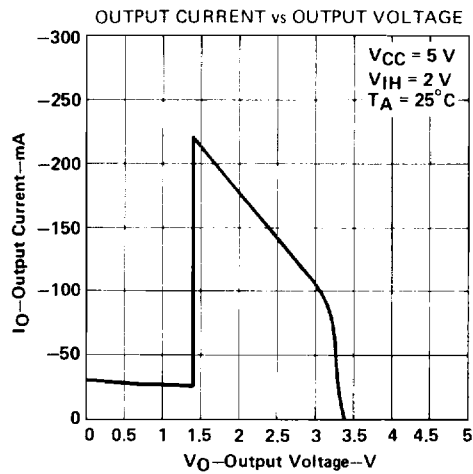


FIGURE 2

APPLICATION INFORMATION

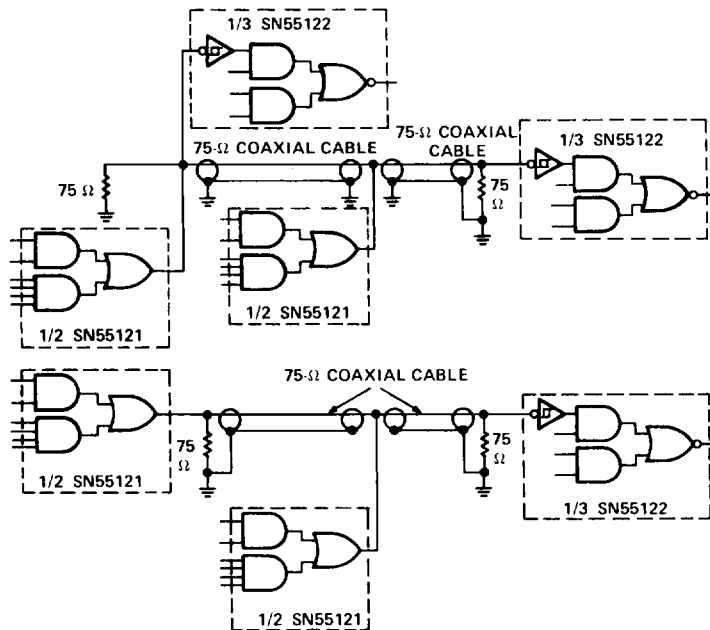


FIGURE 3. SINGLE-ENDED PARTY LINE CIRCUITS

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