TOSHIBA

Physical Layer Controller

1 9 9 8

SONET STS-3c/STS-1

PRELIMINARY

VERSION 0.45

DATA BOOK

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Primary Features of PLC2

1) SONET:STS-3c, STS-1, STS-1/2, SDH:STM-1
2) 155MHz PECL serial line interface with on-chip clock recovery
   and on-chip clock synthesis
3) Cell interface operates in following mode:
   - UTOPIA Level-2 single-PHY(compatible with UTOPIA Level-1) with 8 bit data bus.
   - UTOPIA Level-2 Multi-PHY with 8 bit data bus.
   - UTOPIA Level-2 Multi-PHY with 16 bit data bus.
4) Programmable SOH/POH handling
5) 19.44MHz/6.48MHz/3.24MHz internal operation
6) Maximum 40MHz cell interface operation
7) 0.6μm CMOS technology
8) 5.0V single power supply
9) 144pin thin plastic QFP

Functional Summary of PLC2

Receive Functions

1) Clock recovery from 156/52/26Mbps NRZ signal
2) Byte alignment and frame synchronization
3) Frame descrambling
4) Frame overhead analysis
5) ATM cell synchronization
6) ATM cell header error correction
7) ATM cell payload descramble

Transmit Functions

1) ATM cell payload scramble
2) ATM HEC generation
3) Frame overhead generation
4) Frame assembly
5) Frame scrambling

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1. General

The PLC2 supports SONET STS-3c(SDH STM-1), STS-1 and STS-1/2. The following sections 1.1-1.5 review the frame format, frame overhead, error status, alarm signaling and performance monitoring.

1.1 Frame Format

(1) STS-3c (STM-1)

The STS-3c (STM-1) has a frame of 270 columns (in bytes) and 9 rows, with 9 columns of overhead and 261 columns of payload as shown in Figure 1.1.1. The virtual container VC4 is mapped into the payload area of STS-3c(STM-1). VC4 has a column of overhead called POH (Path Overhead) and 260 columns of payload. The ATM cells are mapped into the payload area of VC4.

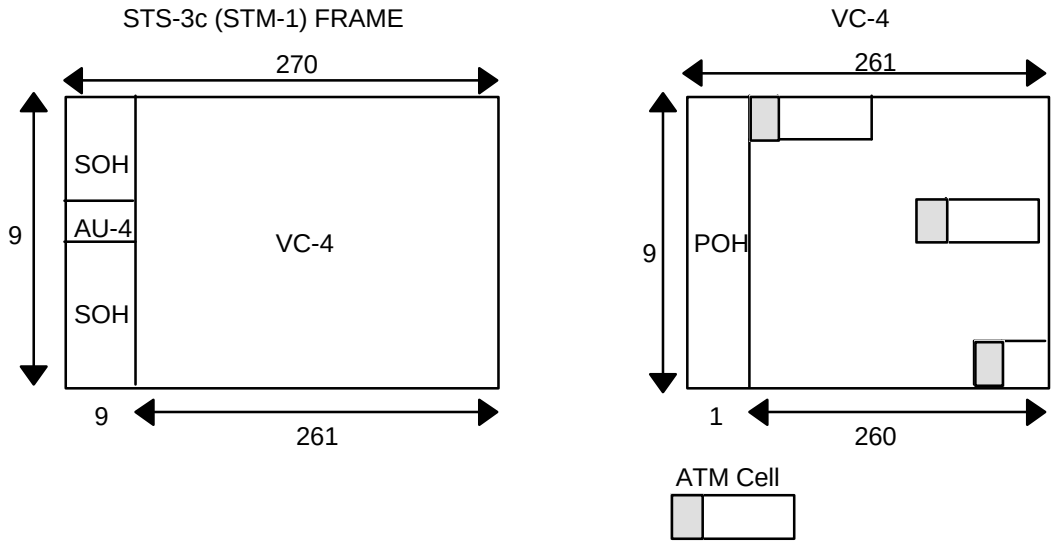


Figure 1.1.1 STS-3c (STM-1) Frame Format

(2) STS-1, STS-1/2

The STS-1 has a frame of 90 columns (in bytes) and 9 rows, with 3 columns of overhead called SOH and 87 columns of payload as shown in Figure 1.1.2. The STS-1 SPE(=Synchronous Payload Envelope), which is mapped into the payload area, has a column of overhead called POH(=Path Overhead) and 87 columns of payload. The ATM cells are mapped into the payload area of STS-1 SPE except for the 30th and 59th columns which are designated stuff columns. STS-1/2 has the same frame format with STS-1.

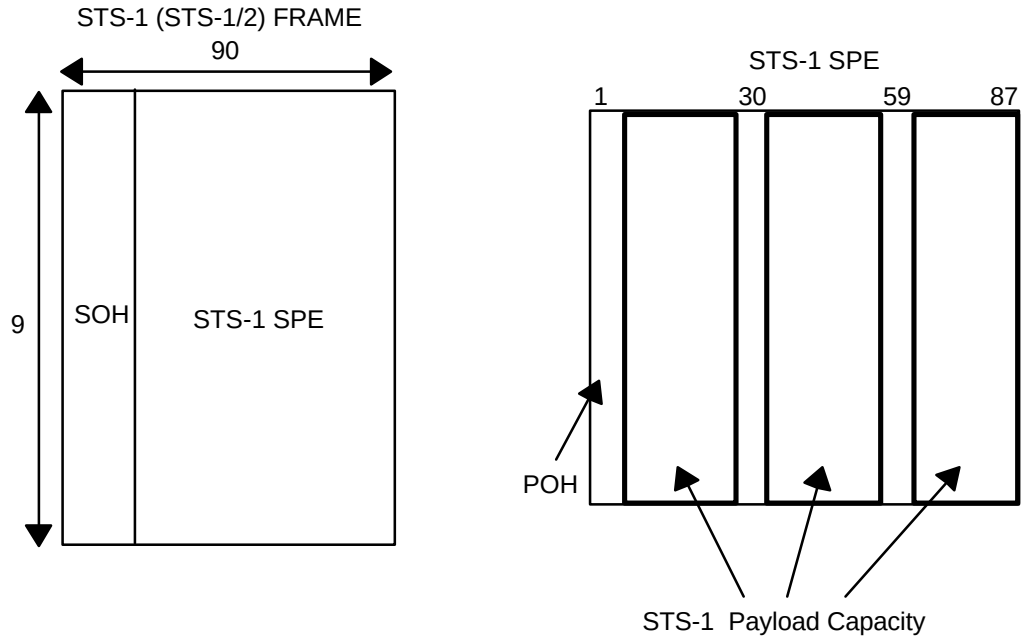


Figure 1.1.2 STS-1 (STS-1/2) Frame Format

1.2 Frame Overhead

The overhead bytes are assigned into SOH and POH as shown in Figure 1.2.1 for STS-3c(STM-1) and Figure 1.2.2 for STS-1 and STS-1/2.

SOH									POH
A1	A1	A1	A2	A2	A2	C1	C1	C1	J1
B1	**	**	E1	**	**	F1	**	**	B3
D1	**	**	D2	**	**	D3	**	**	C2
H1	H1	H1	H2	H2	H2	H3	H3	H3	G1
B2	B2	B2	K1	**	**	K2	**	**	F2
D4	**	**	D5	**	**	D6	**	**	H4
D7	**	**	D8	**	**	D9	**	**	Z3
D10	**	**	D11	**	**	D12	**	**	Z4
Z1	Z1	Z1	Z2	Z2	Z2	E2	**	**	Z5

(** : Not defined)

Figure 1.2.1 STS-3c(STM-1) Overhead Byte Assignment

SOH			POH
A1	A2	C1	J1
B1	E1	F1	B3
D1	D2	D3	C2
H1	H2	H3	G1
B2	K1	K2	F2
D4	D5	D6	H4
D7	D8	D9	Z3
D10	D11	D12	Z4
Z1	Z2	E2	Z5

Figure 1.2.2 STS-1(STS-1/2) Overhead Byte Assignment

The usage of these bytes are almost common for STS-3c(STM-1) , STS-1 and STS1/2. Table 1.2.1 and Table 1.2.2 summarize the usage of the overhead bytes in SOH and POH, respectively.

Name	Function
A1, A2	Frame synchronization.
C1	Identify STS1's in STS-N frame(SONET) / STM-1's in STM-N frame(SDH).
B1	Section BIP-8 error.
E1	Not used in UNI.
F1	Not used in UNI.
D1-D3	Not used in UNI.
H1, H2	AU pointer and Path-AIS.
H3	Stuff operation.
B2	Line BIP-24 for STS-3c and Line BIP-8 for STS-1.
K1	Not used in UNI.
K2	Line AIS and Line RDI.
D4-D12	Not used in UNI.
Z1	Not used in UNI.
Z2	Line FEBE.

Table 1.2.1 Overhead Byte Functions in SOH.

Name	Function
J1	Check path connection.
B3	Monitor Path BIP-8 error.
C2	Indicate the payload type. For ATM cell, the value should be 13H.
G1	Path RDI and Path FEBE.
F2	Not used in UNI.
H4	Indicate the location of the first ATM cell following H4.
Z3	Not used in UNI.
Z4	Not used in UNI.
Z5	Not used in UNI.

Table 1.2.2 Overhead Byte Functions in POH.

1.3 Error Status

PLC2 detects following five error status.

LOS : Loss of Signal

	Condition/Action
Detection	No signal condition continues for T1μsec (2.3 ≤ T 1 ≤ 100).
Release	Two consecutive valid frame alignment patterns (A1's and A2's) have been detected without no LOS between the two valid frame alignment patterns.
Action	Once LOS is detected, the equipment shall send Line AIS, Line RDI, Path AIS or Path RDI.

OOF : Out of Frame

	Condition/Action
Detection	Four consecutive invalid framing patterns have been received.
Release	Two consecutive valid frame alignment patterns have been detected.
Action	The equipment should monitor the duration of OOF.

LOF : Loss of Frame

	Condition/Action
Detection	OOF has continued for 3 msec.
Release	In frame condition has continued for 3 msec.
Action	Once LOF is detected, the equipment shall send Line AIS, Line RDI, Path AIS or Path RDI.

LOP : Loss of Pointer

	Condition/Action
Detection	A valid pointer is not found in N consecutive frames or N consecutive NDF's are detected, where 8 ≤ N ≤ 10.
Release	A valid pointer with normal NDF, or a concatenation indicator, is detected in three consecutive frames. When an all 1's pointer(AIS) is detected in three consecutive frames, the equipment should exit from the LOP state and enter the Path AIS state.
Action	Once LOP is detected, the equipment shall send Path AIS or Path RDI.

LOC : Loss of Cell Delineation

	Condition/Action
Detection	7 consecutive HEC errors have been detected.
Release	7 consecutive normal HEC's have been detected.
Action	When LOC is detected, the equipment shall send Path AIS or Path RDI.

1.4 Alarm Signaling

PLC2 supports following 4 alarm signals.

Line AIS

	Definition
Condition of Generation	State of LOS or LOF.
Generation	K2(b6-8) = 111 and all-ones in the payload of STS-3c/STS-1 frame.
Condition of Removal	Exit from LOS and LOF.
Removal	K2(b6-8) ≠ 111.
Detection of Generation	K2(b6-8) = 111 in five consecutive frames(SONET) / in at least three consecutive frames(SDH).
Detection of Removal	K2(b6-8) ≠ 111 in five consecutive frames(SONET) / in at least three consecutive frames(SDH).

Line RDI

	Definition
Condition of Generation	Detection of LOS, LOF or Line AIS
Generation	K2(b6-8) = 110.
Condition of Removal	Exit from LOS, LOF and Line AIS.
Removal	K2(b6-8) ≠110.
Detection of Generation	K2(b6-8) = 110 in five consecutive frames(SONET) / in at least three consecutive frames(SDH).
Detection of Removal	K2(b6-8) ≠110 in five consecutive frames(SONET) / in at least three consecutive frames(SDH).

Path AIS

	Definition
Condition of Generation	Detection of LOS, LOF, LOP, LOC or Line AIS.
Generation	All-ones in the H1/H2/H3 bytes and the entire payload.
Condition of Removal	Exit from LOS, LOF, LOP, LOC and Line AIS.
Removal	A correct STS pointer with NDF set to '1001' followed by normal pointer operations and normal data in the payload.
Detection of Generation	All-ones in the H1/H2 bytes for three consecutive frames (for SONET and SDH as well).
Detection of Removal	A valid STS Pointer with NDF set to '1001', or a valid STS Pointer with normal NDF in three consecutive frames (for SONET and SDH as well) or LOP is detected (in SDH mode only).

Path RDI

	Definition
Condition of Generation	Detection of LOS, LOF, LOP, LOC, Line AIS or Path AIS.
Generation	G1(b5) = 1.
Condition of Removal	Exit from LOS, LOF, LOP, LOC, Line AIS and Path AIS.
Removal	G1(b5) = 0.
Detection of Generation	G1(b5) = 1 in ten consecutive frames(SONET) / in at least three consecutive frames(SDH).
Detection of Removal	G1(b5) =0 in ten consecutive frames(SONET) / in at least three consecutive frames(SDH).

1.5 Performance Monitoring

PLC2 supports following two performance monitors.

Line FEBE

Line BIP-24 is calculated over the entire area of each frame after descrambling except for the first to third rows of SOH based on 24 bits interleaved parity calculation using even parity. The calculated BIP-24 code is compared with the triple B2 bytes of the following frame. Differences indicates the line level bit errors. The bit errors are counted and inserted to the third Z2 byte of transmit SOH as shown in Figure 1.5.1.

Z2	Z2	Z2	
00H	00H	0	L-FEBE[6:0]

Figure 1.5.1 L-FEBE Insertion to Z2 Byte.

Path FEBE

Path BIP-8 is calculated over the entire area of each VC4 (or SPE for STS-1) after descrambling based on 8bits interleaved parity calculation using even parity. The calculated BIP-8 code is compared with the B3 byte of the following frame. Differences indicates the path level bit errors. The bit errors are counted and inserted to the higher 4 bits of G1 byte of transmit SOH as shown in Figure 1.5.2.

G1		
P-FEBE[3:0]		000

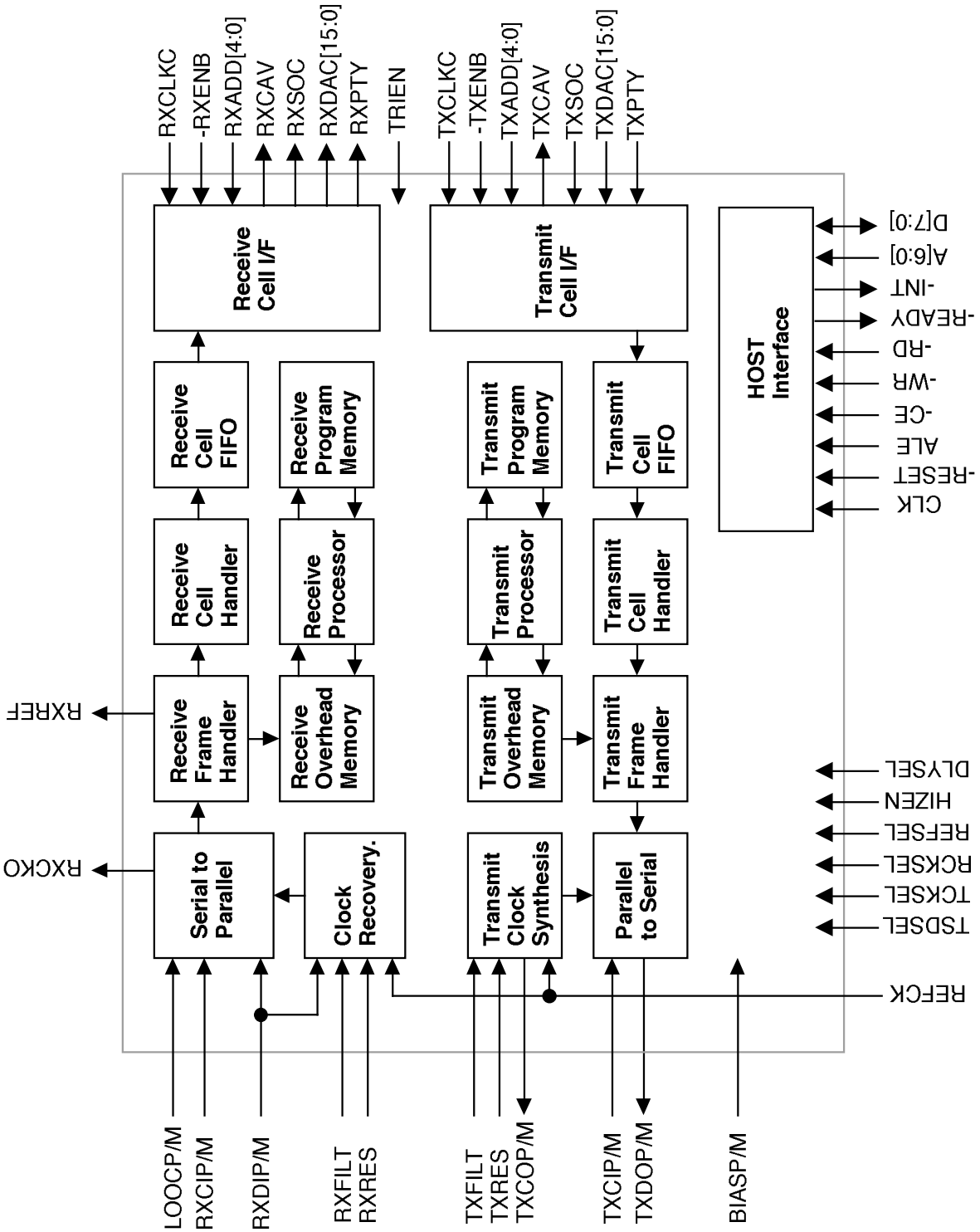
↑P-RDI

Figure 1.5.2 P-FEBE Insertion to G1 Byte.

2. Interface

2.1 Block diagram

PLC2 block diagram is shown below.



2.2 Pin Description

Line I/F (20 pin)

PIN NAME	Pin NO.	I/O	TYPE	Description
RXCIP RXCIM	134, 135	I	P-ECL	Receive clock differential P-ECL input. When RCKSEL is tied low, RXDIP/M is sampled on this clock. They should be terminated to 3.0V via 50 ohm. These pins should be tied to ground when they are not used.
RXDIP RXDIM	128, 129	I	P-ECL	Receive date differential P-ECL input. They should be terminated to 3.0V via 50 ohm.
TXCOP TXCOM	118, 119	O	P-ECL	Transmit clock differential P-ECL output. They should be terminated to 3.0V via 50 ohm.
TXCIP TXCIM	125, 126	I	P-ECL	Transmit reference clock differential P-ECL input. When TCKSEL is tied low, TXDOP/M is updated on this clock. They should be terminated to 3.0V via 50 ohm. These pins should be tied to ground when they are not used.
TXDOP TXDOM	122, 123	O	P-ECL	Transmit data differential P-ECL output. They should be terminated to 3.0V via 50 ohm.
LOOCP LOOCM	131, 132	I	P-ECL	LOOCP/M should be connected with signal detect output SD-/+ of optical module. When LOOC is tied high, RXDI input is fixed to zero inside PLC2 and receive PLL switches to the reference clock REFCK to keep the oscillation. LOOCP/M should be terminated to 3.0V via 50 ohm. These pins should be tied to ground when they are not used.
BIASP BIASM	114, 115	I	P-ECL	This input generates P-ECL voltage level. They should be connected to 3.0V via 50 ohm.
RXCKO	139	O	CMOS	Receive serial clock (recovered from receive data or RXCIP/M depending on RCKSEL) is divided by eight and output from RXCKO when CLKSEL of TSMOD2 register is set to 0. Transmit serial clock is divided by eight and output from RXCKO when CLKSEL is set to 1.
RXFILT	106	AO	Analog	RXFILT should be connected to AVSSR via LPF for receive PLL.
RXRES	107	AO	Analog	RXRES should be connected to AVSSR via resistor for reference current of receive PLL.
TXFILT	111	AO	Analog	TXFILT should be connected with AVSST via LPF for transmit PLL.
TXRES	110	AO	Analog	TXRES should be connected to AVSST via resistor for reference current of transmit PLL.
REFCK	143	I	CMOS	Reference clock of 19.44MHz should be input regardless of transmission rate (STS-3, STS-1, STS-1/2).

Cell I/F (53 pin)

PIN NAME	Pin NO.	I/O	TYPE	Description
TXDAC[15:0]	43, 45-53, 56-61	TI	TTL	The transmit cell data bus from ATM layer.
TXSOC	63	TI	TTL	The transmit start of cell indication is asserted when TXDAC contains the first byte of cell data.
-TXENB	41	I	TTL	The active low cell transfer enable signal is activated when TXDAC contains valid cell data.
TXCAV	42	TO	TTL	The transmit cell available is asserted high when PLC2 can receive a complete cell data from ATM layer.
TXCLKC	40	I	TTL	The operation clock for the transmit cell interface.
TXPTY	62	I	TTL	The parity bit for TXDAC. Both odd parity and even parity are selectable.
TXADD[4:0]	65-69	I	TTL	TX PHY port address
RXDAC[15:0]	6, 7, 9-11, 14-17, 20-23, 25-27	TO	TTL	The receive cell data bus to ATM layer.
RXSOC	30	TO	TTL	The receive start of cell indication is asserted high when RXDAC contains the first byte of cell data.
-RXENB	3	I	TTL	The receive cell transfer enable signal is asserted low when ATM layer device will sample cell data in the next cycle.
RXCAV	5	TO	TTL	The receive cell available is asserted high when PLC2 is ready to transfer a complete cell data to ATM layer.
RXCLKC	2	I	TTL	The operation clock for the receive cell interface.
RXPTY	29	TO	TTL	The parity bit for RXDAC. Both odd parity and even parity are selectable.
RXADD[4:0]	32-34, 38, 39	I	TTL	RX PHY port address
TRIEN	31	I	CMOS	Tri-state enable. When it is tied high, type TO signals of cell interface operate as tri-state output. When it is tied low, they are always in drive mode.

CPU I/F (23 pin)

PIN NAME	Pin NO.	I/O	TYPE	Description
A[6:0]	87-89, 91-94	I	TTL	Address Bus
D[7:0]	76-79, 82-85	Bidirect	TTL	Data Bus
ALE	95	I	TTL	Address Latch Enable. Address A[6:0] is latched at falling edge of ALE. When ALE is high, the internal address latches are transparent.
-CE	96	I	TTL	Active Low Chip Enable
-RD	97	I	TTL	Active Low Read Command
-WR	98	I	TTL	Active Low Write Command
-READY	99	TO	TTL	Active Low Ready Signal
-RESET	75	I	TTL	Active Low Hardware Reset Signal
-INT	101	O	TTL	Active Low Interrupt Signal
CLK	74	I	TTL	CPU I/F clock signal. Recommended to be 19.44MHz.

Monitor Output (1 pin)

PIN NAME	Pin NO.	I/O	TYPE	Description
RXREF	70	O	TTL	When MONSEL bit in TSMOD2 register is set high, 8KHz frame clock is output. It goes high for one byte clock period at one frame interval (STS-3/STM-1, STS-1) or two frame interval (STS-1/2). When MONSEL bit in TSMOD2 register is set low, internal signal "REFSYN" is output.

Mode Select (6 pin)

PIN NAME	Pin NO.	I/O	TYPE	Description
RCKSEL	137	I	CMOS	Receive Clock Select. When it is tied high, internally recovered clock is used to sample RXDIP/M. When it is tied low, external clock RSCIP/M is used to sample RXDIP/M.
TCKSEL	138	I	CMOS	Transmit clock select. When it is tied high, TXPLL generates clock used to serialize transmit data. When tied low, TXCIP/M is used to serialize transmit data. In loop-timing mode, the receive clock is used as transmit clock and TCKSEL has no effect.
REFSEL	141	I	CMOS	When tied high, RXPLL generates x8 clock from REFCK. When tied low, RXPLL recovers clock from receive data as long as receive data is normal.
TSDSEL	142	I	CMOS	Transmit data select. When it is tied low, normal transmit data is output from TXDOP/M. When it is tied high, RXDIP/M is directly output from TXDOP/M.
HIZEN	103	I	CMOS	This input selects following mode 1: All the terminal are set to HI-Z 0: Normal Operation
DLYSEL	102	I	CMOS	This input selects following mode 0: RXDIP/M is sampled on the rising edge of receive serial clock 1: RXDIP/M is sampled on the falling edge of receive serial clock

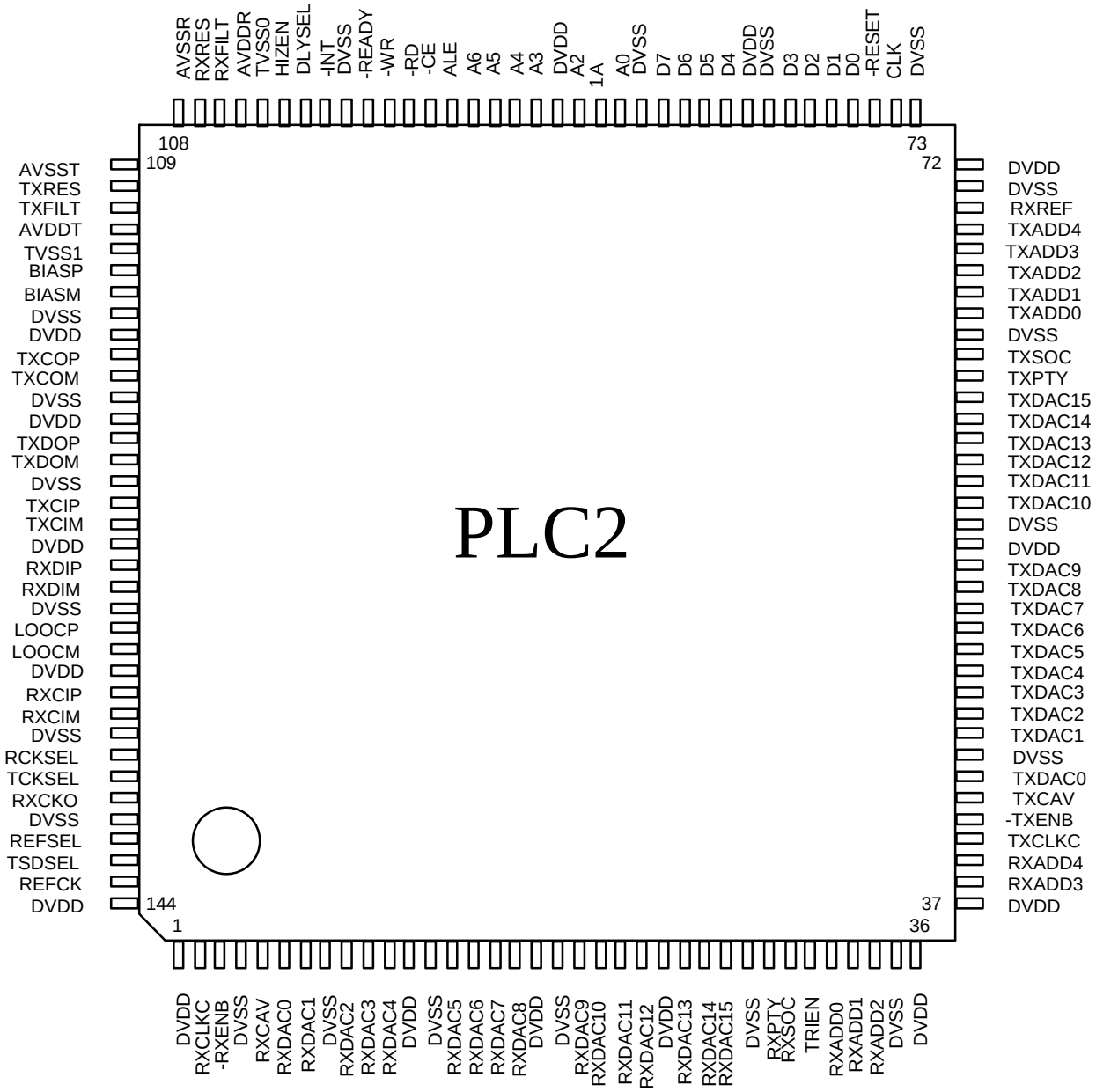
VDD/GND (41 pin)

PIN NAME	Pin NO.	Description
DVDD(15)	1,12,18,24, 36,37,54,72, 81,90,117,121, 127,133,144	VDD for digital block and P-ECL buffer
DVSS(20)	4,8, 13,19, 28,35, 44,55, 64,71, 73,80, 86,100,116,120, 124,130,136,140	VSS for digital block and P-ECL buffer
AVDDR	105	VDD dedicated for receive PLL. It should be coupled with DVDD via filter or ferrite beads.
AVSSR	108	VSS dedicated for receive PLL. It should be coupled with DVSS via filter or ferrite beads.
AVDDT	112	VDD dedicated for transmit PLL. It should be coupled with DVDD via filter or ferrite beads.
AVSST	109	VSS dedicated for transmit PLL. It should be coupled with DVSS via filter or ferrite beads.
TVSS(2)	104, 113	VSS dedicated for guard Pwell. They should be separated with DVSS via filter or ferrite beads.

'-' indicates active low signal

PLC2 pin layout

PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME
1	DVDD	37	DVDD	73	DVSS	109	AVSST
2	RXCLKC	38	RXADD3	74	CLK	110	TXRES
3	-RXENB	39	RXADD4	75	-RESET	111	TXFILT
4	DVSS	40	TXCLKC	76	D0	112	AVDDT
5	RXCAV	41	-TXENB	77	D1	113	TVSS
6	RXDAC0	42	TXCAV	78	D2	114	BIASP
7	RXDAC1	43	TXDAC0	79	D3	115	BIASM
8	DVSS	44	DVSS	80	DVSS	116	DVSS
9	RXDAC2	45	TXDAC1	81	DVDD	117	DVDD
10	RXDAC3	46	TXDAC2	82	D4	118	TXCOP
11	RXDAC4	47	TXDAC3	83	D5	119	TXCOM
12	DVDD	48	TXDAC4	84	D6	120	DVSS
13	DVSS	49	TXDAC5	85	D7	121	DVDD
14	RXDAC5	50	TXDAC6	86	DVSS	122	TXDOP
15	RXDAC6	51	TXDAC7	87	A0	123	TXDOM
16	RXDAC7	52	TXDAC8	88	A1	124	DVSS
17	RXDAC8	53	TXDAC9	89	A2	125	TXCIP
18	DVDD	54	DVDD	90	DVDD	126	TXCIM
19	DVSS	55	DVSS	91	A3	127	DVDD
20	RXDAC9	56	TXDAC10	92	A4	128	RXDIP
21	RXDAC10	57	TXDAC11	93	A5	129	RXDIM
22	RXDAC11	58	TXDAC12	94	A6	130	DVSS
23	RXDAC12	59	TXDAC13	95	ALE	131	LOOCP
24	DVDD	60	TXDAC14	96	-CE	132	LOOCM
25	RXDAC13	61	TXDAC15	97	-RD	133	DVDD
26	RXDAC14	62	TXPTY	98	-WR	134	RXCIP
27	RXDAC15	63	TXSOC	99	-READY	135	RXCIM
28	DVSS	64	DVSS	100	DVSS	136	DVSS
29	RXPTY	65	TXADD0	101	-INT	137	RCKSEL
30	RXSOC	66	TXADD1	102	DLYSEL	138	TCKSEL
31	TRIEN	67	TXADD2	103	HIZEN	139	RXCKO
32	RXADD0	68	TXADD3	104	TVSS	140	DVSS
33	RXADD1	69	TXADD4	105	AVDDR	141	REFSEL
34	RXADD2	70	-RXREF	106	RXFILT	142	TSDSEL
35	DVSS	71	DVSS	107	RXRES	143	REFCK
36	DVDD	72	DVDD	108	AVSSR	144	DVDD



PLC2 Pin Assignment

2.3 Line Interface

(1) Receive Line Interface

RXCIP/M

The bit serial receive clock input is used when the on-chip clock recovery is disabled. The frequency should be 155.52MHz for STS-3, 51.84MHz for STS-1 and 25.92MHz for STS-1/2. When the on-chip clock recovery is enabled, RXCIP/M is not used.

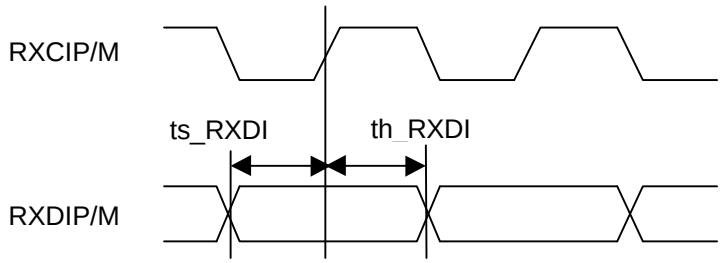


Figure 2.3.1 RX Line Interface Timing

RXDIP/M

The receive differential serial data input RXDIP/M is sampled on the rising edge of receive serial clock, which is RXCIP/M or internally recovered clock depending on RCKSEL. Optionally RXDIP/M can be sampled on the falling edge of receive serial clock by tying DLYSEL pin to high.

(2) Transmit Line Interface

TXCIP/M

The differential transmit clock input is used when the bit serial interface is selected and the on-chip transmit clock synthesis is disabled. The frequency should be 155.52MHz for STS-3, 51.84MHz for STS-1 and 25.92MHz for STS-1/2. When the on-chip transmit clock synthesis is enabled or loop timing mode is selected, TXCIP/M is not used.

TXDOP/M

The transmit differential serial data output is updated on the falling edge of TXCIP/M.

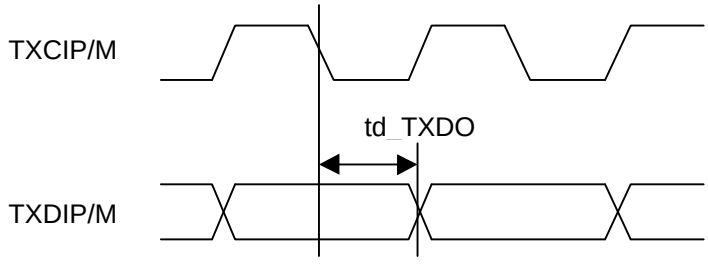


Figure 2.3.2 TX Line Interface Timing

2.4 Cell Interface

(1) Transmit Cell Interface in Single-PHY Mode

The transmit cell interface operates basically in cell mode instead of byte mode, that is, the PLC2 asserts TXCAV when it has capacity for a complete cell. But it can receive the byte mode cell transfer.

TXCLKC

Transmit cell interface clock provided by the ATM layer.

TXCAV

Active high, cell available signal asserted by the PLC2 to indicate it can receive a complete cell. If the PLC2 has no more capacity for a cell, it deasserts TXCAV when the 44th payload of a cell is output on TXDAC[7:0].

TXENB*

Active low enable signal asserted by the ATM layer when TXDAC[7:0] contains a valid data.

TXSOC

Active high, start of cell signal asserted by the ATM layer.

TXADD[4:0]

Polling address input is ignored in Single-PHY mode.

TXDAC[7:0]

Transmit cell data bus driven by the ATM layer device.

TXPTY

The parity bit for TXDAC[7:0]. Both odd parity and even parity are selectable. When a parity error is detected in a cell received by the PLC2, it is just reported to the host CPU and the cell is not discarded.

Figure 2.4.1 shows the consecutive transmit cell transfer without any obstacles. When PLC2 finds the transmit FIFO has a room for a complete cell, it asserts TXCAV at the rising edge of TXCLKC. The ATM layer recognizes this indication and asserts TXENB* and puts valid cell data on TXDAC[7:0]. TXSOC coincides with the first byte of a cell.

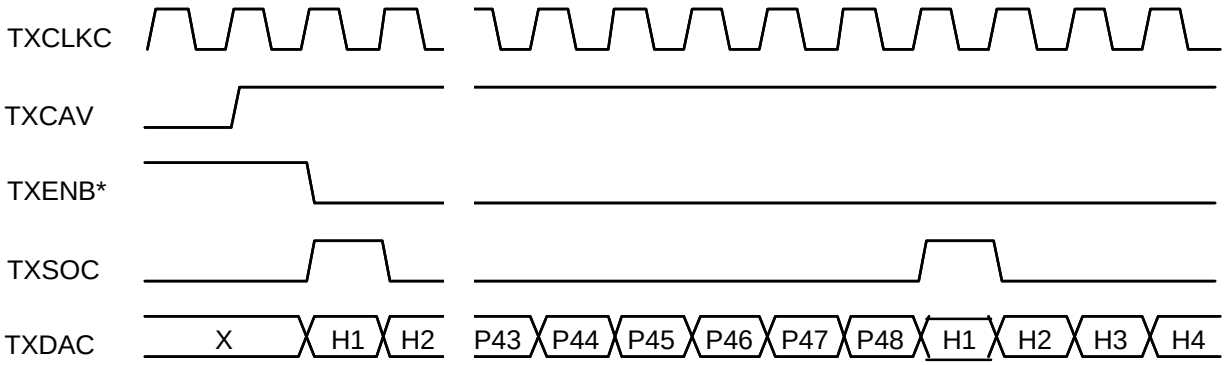


Figure 2.4.1 Transmit Cell Transfer (1)

Figure 2.4.2 shows the case where the ATM layer stops the data transfer for one cycle. The ATM layer deasserts TXENB* to indicate that the data on TXDAC[7:0] is invalid.

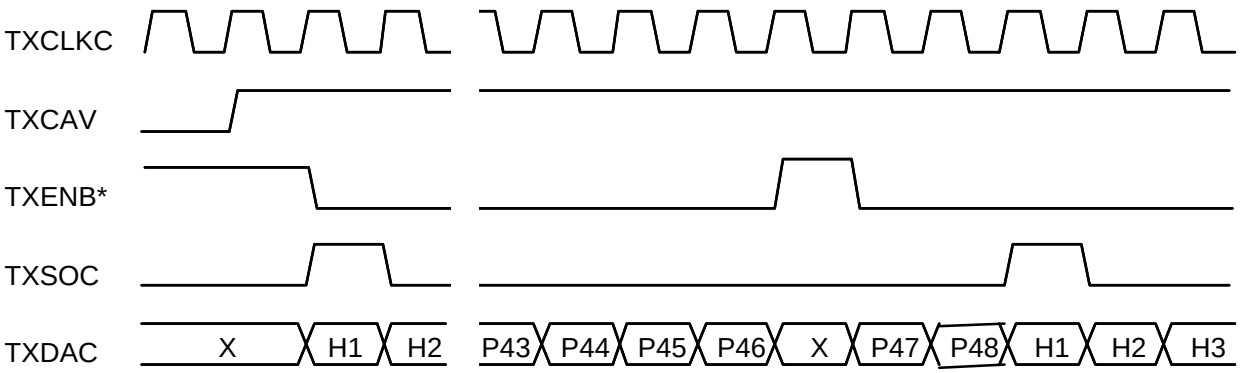


Figure 2.4.2 Transmit Cell Transfer (2)

Figure 2.4.3 shows the case of a single cell data transfer. The PLC2 deasserts TXCAV when the 44th payload byte is on TXDAC, to indicate it cannot accept another cell. The ATM layer stops the cell transfer and deasserts TXENB* after the last byte of the cell has been transferred.

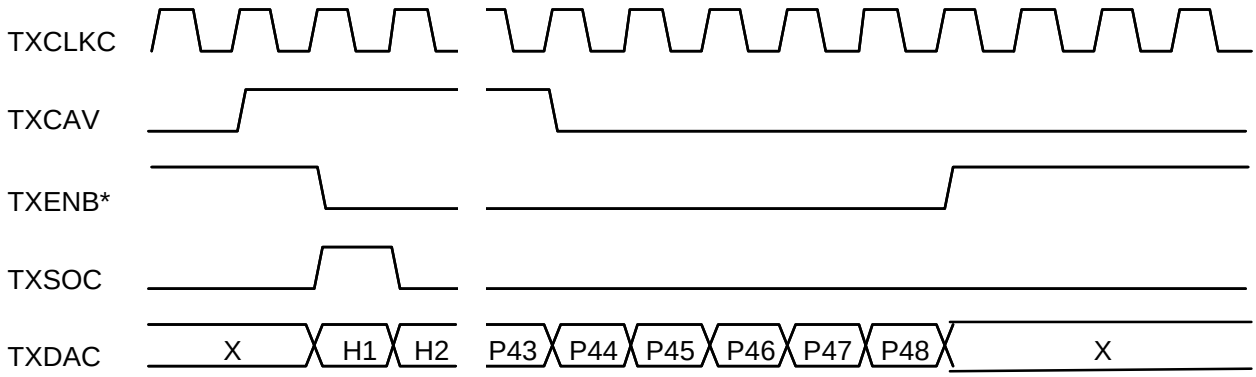


Figure 2.4.3 Transmit Cell Transfer (3)

Figure 2.4.4 shows the case where the PLC2 stops the next cell transfer. The PLC2 finds, when receiving a cell data, no room for another cell and deasserts TXCAV when it is receiving the 44th payload byte. The ATM layer continues the cell transfer and stops it and deasserts TXENB* in the next cycle of the last byte of the cell. At the same instance, the PLC2 finds the transmit FIFO has now a room for a cell and asserts TXCAV. Watching this, the ATM layer resumes the transfer of cell.

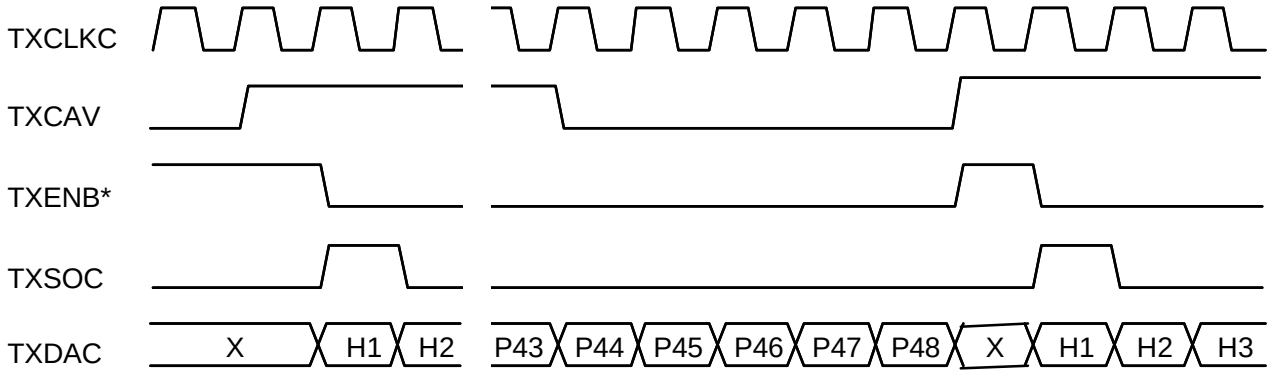


Figure 2.4.4 Transmit Cell Transfer (4)

(2) Receive Cell Interface In Single-PHY Mode

The receive cell interface operates basically in cell mode instead of byte mode, that is, the PLC2 starts cell transfer when is has a complete cell in the receive cell FIFO. But the PLC2 can stop the cell transfer when it is so requested by the ATM layer.

RXCLKC

Receive cell interface operation clock.

RXCAV

Active high, cell available signal asserted by the PLC2 to indicate it has a complete cell available for transfer to the ATM layer.

RXENB*

Active low, enable signal asserted by the ATM layer to indicate that RXDAC and RXSOC will be sampled at the next cycle.

RXSOC

Active high, start of cell signal asserted by the PLC2 when the first byte of the cell appears on RXDAC.

RXADD[4:0]

Polling address input is ignored in Single-PHY mode.

RXDAC[7:0]

Receive cell data bus driven by the PLC. RXDAC[7:0] is tri-state type. When TRIEN is set low, RXDAC is always driven by the PLC2. When TRIEN is set high, RXDAC[7:0] is driven by the PLC2 only in cycles following those with RXENB* asserted.

RXPTY

The parity bit for RXDAC[7:0]. Both odd parity and even parity are selectable. When TRIEN is set low, RXPTY is always driven by the PLC2. When TRIEN is set high, RXPTY is driven by the PLC2 only in cycles following those with RXENB* asserted.

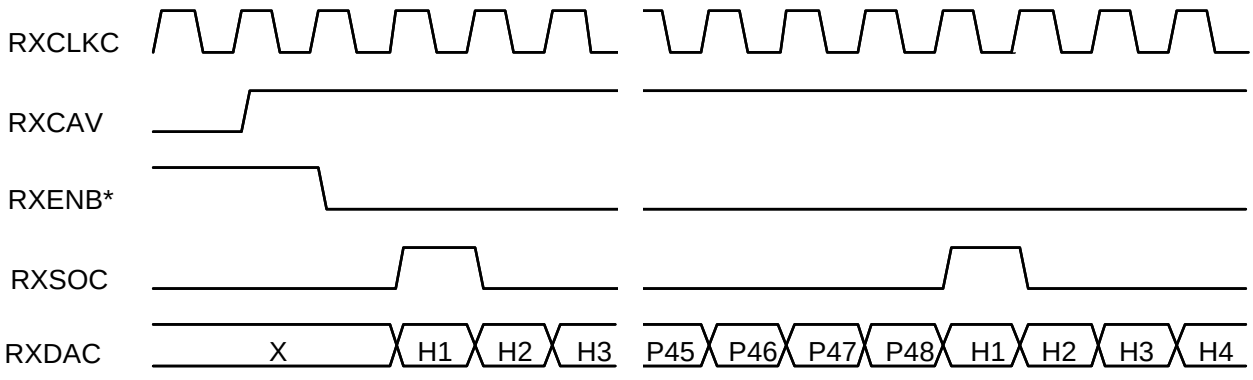


Figure 2.4.5 Receive Cell Transfer (1)

Fig 2.4.5 shows the consecutive receive cell transfer without any obstacles. When the PLC2 has a complete cell to transfer, it activates RXCAV at the rising edge of RXCLKC.

The ATM layer then activates RXENB* indicating that it will sample the data on RXDAC from the next cycle. The PLC2 begin the transfer of the cell data on RXDAC.

Figure 2.4.6 shows the case where the ATM layer stops the cell transfer. The PLC2 recognizes RXENB* deactivated and outputs the 47th payload byte again.

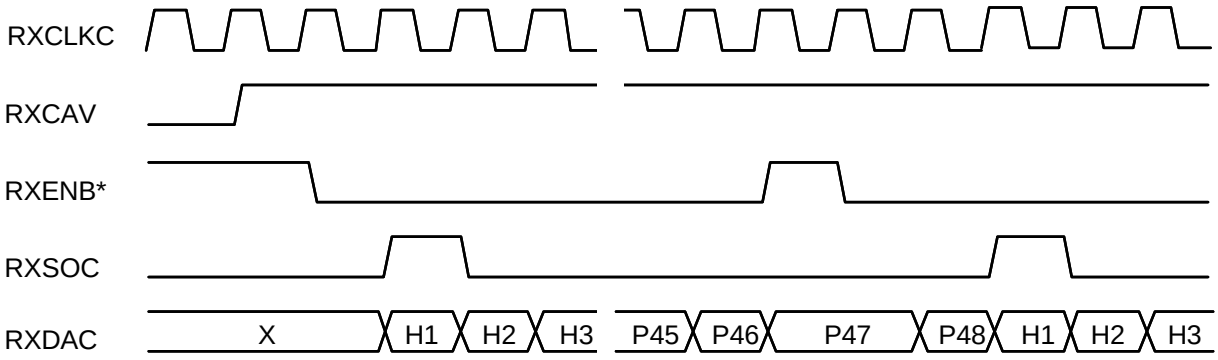


Figure 2.4.6 Receive Cell Transfer (2)

Figure 2.4.7 shows the case where the PLC2 deasserts RXCAV for a cycle after a cell transfer has been completed. In the cycles denoted by X on RXDAC, the ATM layer waits for another cell transfer with keeping RXENB* low.

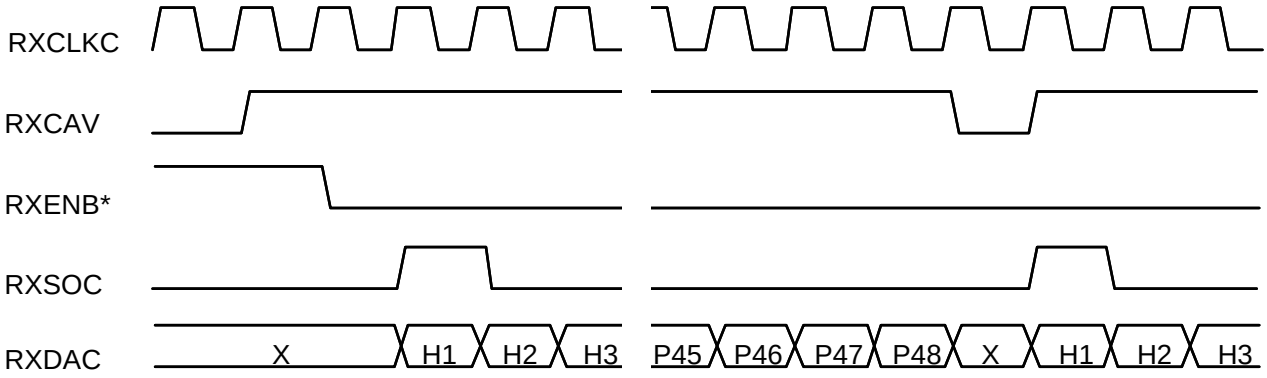


Figure 2.4.7 Receive Cell Transfer (3)

(3) Transmit Cell Interface In Multi-PHY Mode

The transmit cell interface operates basically in cell mode instead of byte mode, that is, the PLC2 asserts TXCAV when it is polled and it can receive a complete cell into the transmit cell FIFO. But the ATM layer can halt ongoing cell transmission anytime by deasserting -TXENB.

TXCLKC

Transmit cell interface clock provided by the ATM layer.

TXCAV

Active high, cell available signal asserted by the PLC2 to indicate it can receive a complete cell. When PLC2 is polled, PLC2 drives TXCAV high or low in the following cycle, depending on the condition of the transmit cell FIFO of the port. When the FIFO can receive a cell, TXCAV is driven high, otherwise TXCAV is driven low. TXCAV is always driven by PLC2 when TRIEN is tied low.

TXENB*

-TXENB indicates that TXDAC[15:0] contains valid data when asserted low. It is also used to select a port to send cell data. For port selection, -TXENB is kept high and at the same time, TXADD[4:0] indicates which port should be selected. In the following cycle, -TXENB is asserted and TXDAC[15:0] outputs valid cell data.

TXSOC

Active high, start of cell indication asserted by the ATM layer.

TXADD[4:0]

Transmit polling address driven by the ATM layer.

TXDAC[15:0]

Transmit cell data bus driven by the ATM layer.

TXPTY

The parity bit for TXDAC[15:0]. Both odd parity and even parity are selectable. When a parity error is detected in a cell received by the PLC2, it is reported to the host CPU and the cell is not discarded.

Fig. 2.4.8 shows polling at transmit interface. The polling takes two steps. For instance, at clock edge #2, ATM layer indicates that port "N" is to be polled. Then at clock edge #3, ATM layer does not change the level of -TXENB and PLC2 drives or not drive TXCAV depending on the condition in PLC2. The PLC2 drives TXCAV high if port "N" exists in PLC2 and the port is ready to receive a cell from ATM layer. It drives TXCAV low if port "N" exists in PLC2 and the port is not ready to receive a cell from ATM layer. It does not drive TXCAV at clock edge #3 if port address "N" does not match the port address in PLC2. The port address is stored in CIADR register. ATM layer should not change the level of -TXENB from high to low during polling phase because such a move is considered by PLC2 as "selection" and PLC2 starts to receive cell. Care should be taken that when ATM

layer transmits cell to port N, it should not poll the port N. Such polling behavior is not assumed.

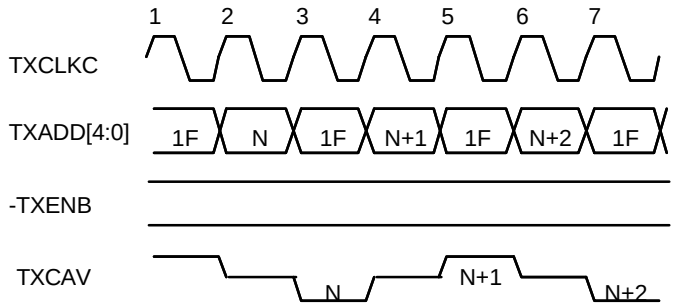


Figure 2.4.8 Polling at Transfer Interface

Figure 2.4.9 shows selection at transmit interface. At clock edge #4 ATM layer indicates the port address to be selected on TXADD[4:0] and at clock edge #5 asserts -TXENB to indicate that selection is being done. At clock edge #5, ATM layer starts cell transmission. This figure shows a case of the minimum interval between adjacent cell transmission.

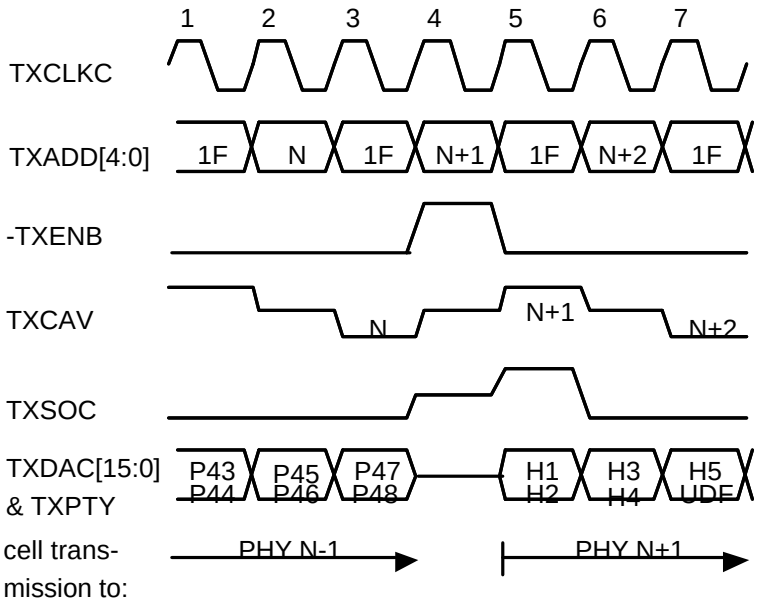


Figure 2.4.9 Selection at Transmit Interface

Figure 2.4.10 shows a case where polling is done before restart of cell transmission. During polling, ATM layer leaves TXSOC, TXPTY and TXADD[15:0] in Hi-Z state.

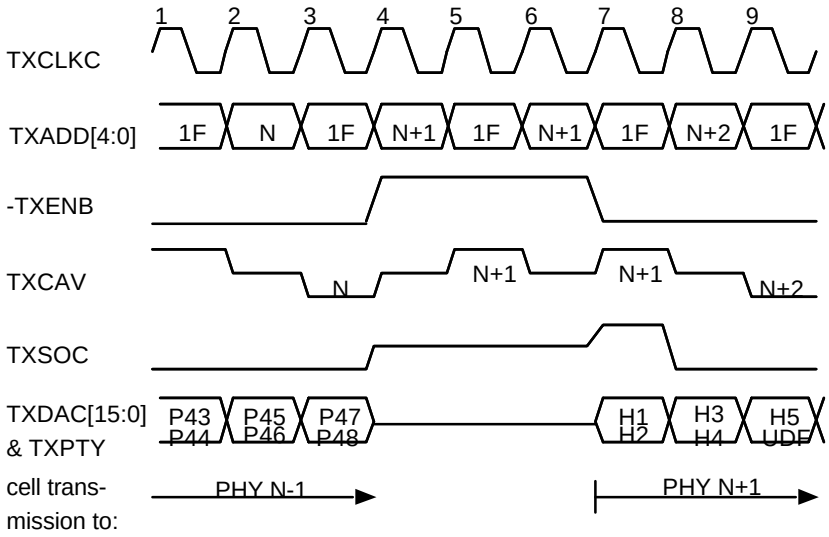


Figure 2.4.10 End and Restart of Cell Transmission at Transmit Interface

Figure 2.4.11 shows a case where cell transmission is paused halfway. To restart the cell transmission ATM layer selects port M explicitly at clock edge #7.

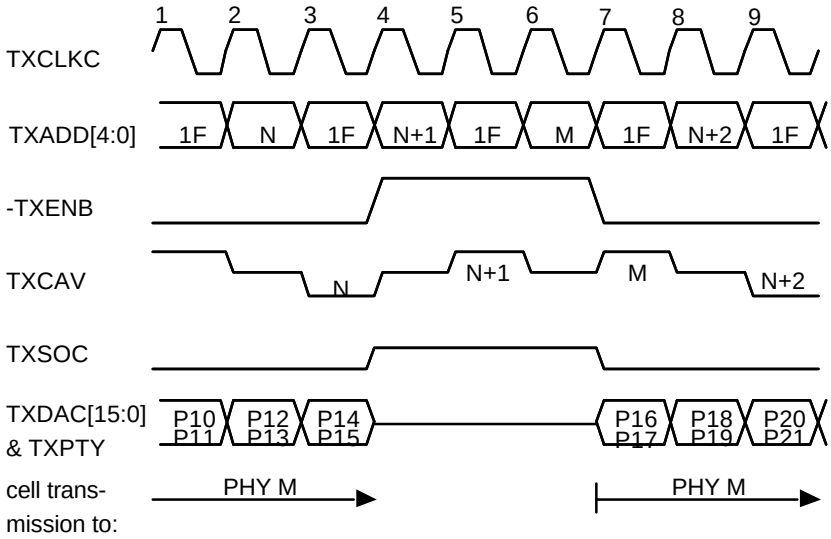


Figure 2.4.11 Cell Transmission to PHY Paused for Three Cycles

(4) Receive Cell Interface In Multi-PHY Mode

The receive cell interface operates basically in cell mode instead of byte mode, that is, the PLC2 starts cell transmission when it has a complete cell in the receive cell FIFO. But the ATM layer can halt the cell transmission by deasserting -RXENB.

RXCLKC

Receive cell interface operation clock.

RXCAV

Active high, cell available signal asserted by the PLC2 to indicate it can transmit a complete cell. When PLC2 is polled, PLC2 drives RXCAV high or low in the following cycle, depending on the condition of the receive cell FIFO of the port. When the FIFO contains a complete cell to transmission, RXCAV is driven high, otherwise RXCAV is driven low. RXCAV is always driven by PLC2 when TRIEN is tied low.

-RXENB

-RXENB indicates that RXDAC[15:0] contain valid data in the following cycle when asserted low. It is also used to select a port to transmission cell data. For port selection, -RXENB is deasserted and at the same time, RXADD[4:0] indicates which port is selected. In the following cycle, -RXENB is asserted and RXDAC[15:0] is sampled from the following cycle.

RXSOC

Active high, start of cell signal asserted by the PLC2 when the first byte of the cell appears on RXDAC[15:0].

RXADD[4:0]

Receive polling address driven by the ATM layer.

RXDAC[15:0]

Receive cell data bus driven by the PLC. RXDAC[15:0] is tri-state type. When TRIEN is set low, RXDAC is always driven by the PLC2. When TRIEN is set high, RXDAC[15:0] is driven by the PLC2 only in cycles following those with -RXENB asserted.

RXPTY

The parity bit for RXDAC[7:0]. Both odd parity and even parity are selectable. When TRIEN is set low, RXPTY is always driven by the PLC2. When TRIEN is set high, RXPTY is driven by the PLC2 only in cycles following those with -RXENB asserted.

Fig. 2.4.12 shows polling at receive interface. The polling takes two steps. For instance, at clock edge #2, ATM layer indicates that port "N" is to be polled. Then at clock edge #3, ATM layer does not change the level of -RXENB and PLC2 drives or not drive RXCAV depending on the condition in PLC2. The PLC2 drives RXCAV high if port "N" exists in PLC2 and it is ready to transmit a cell to ATM layer. It drives RXCAV low if port "N" exists in PLC2 and the port is not ready to transmit a cell to ATM layer. It does not drive RXCAV at clock edge #3 if port address "N" does not match the port address in PLC2. The port address is stored in CIADR register. ATM layer should not change the level of -RXENB from high to low during polling phase because such a move is considered by PLC2 as "selection" and PLC2 starts to transmit cell. Care should be taken that when ATM layer receives a cell from port N, it should not poll the port N. Such polling behavior is not assumed.

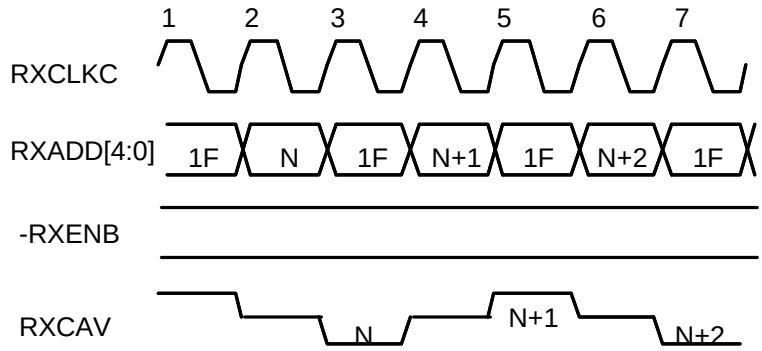


Figure 2.4.12 Polling at Receive Interface

Figure 2.4.13 shows selection at receive interface. At clock edge #3 ATM layer indicates the port address to be selected on TXADD[4:0] and at clock edge #4 asserts -RXENB to indicate that selection is being done. At clock edge #5, PLC2 starts cell transmission to ATM layer. This figure shows a case of the minimum interval between adjacent cell transmission of different port.

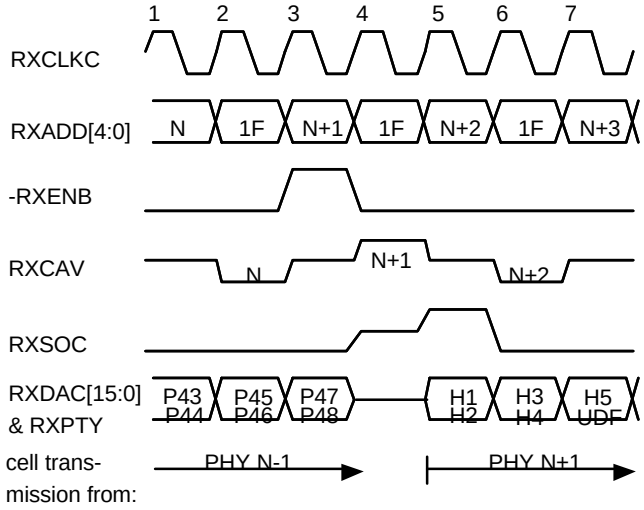


Figure 2.4.13 Selection at Receive Interface

Figure 2.4.14 shows a case where polling is done before restart of cell transmission. At clock edge #4, ATM layer finds no port other than port N-1is ready to transmit a cell to ATM layer and let -RXENB asserted to see if port N-1 is ready to transmit a cell. At clock edge #5, ATM layer finds that port N-1 has no more cell because PLC2 leaves RXSOC low. Then ATM layer deasserts -RXENB to indicate that cell transmission is over. During the cycle of clock edge #5, PLC2 continues driving RXSOC, RXPTY and RXDAC[15:0] because -RXENB was asserted during the cycle of clock edge #4. Polling continues during such transaction. At clock edge #8, ATM layer find that port N+2 is ready to transmit a cell. Then port N+2 is selected at clock edge #9. Port N+2 starts cell transmission at clock edge #10.

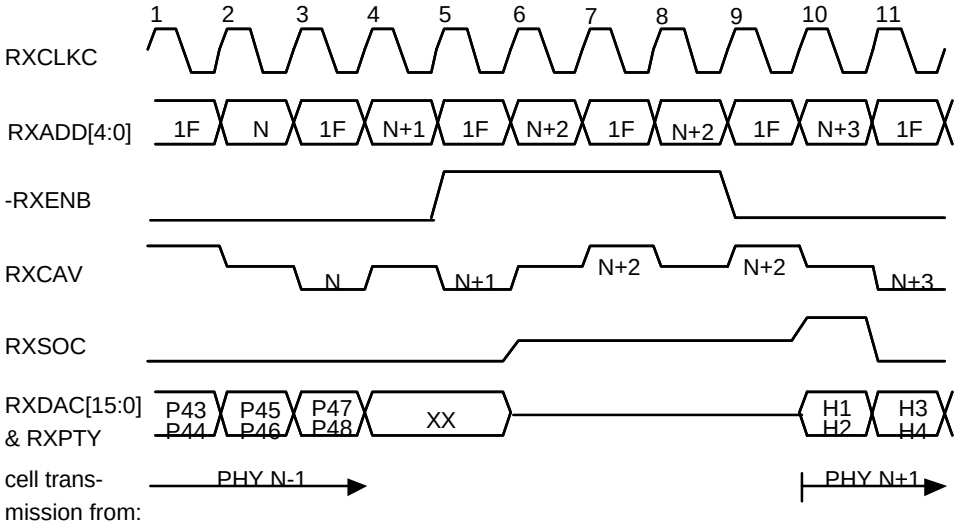


Figure 2.4.14 End and Restart of Rell Transmission at Receive Interface

Figure 2.4.15 shows a case of back to back cell transmission. At clock edge #5, ATM layer leaves -RXENB asserted because no other port than PHY N is ready to transmit a cell. At clock edge #6, port N finds that it is invited to transmit one more cell and the port happens to have a cell to transmit, then it starts to transmit a cell.

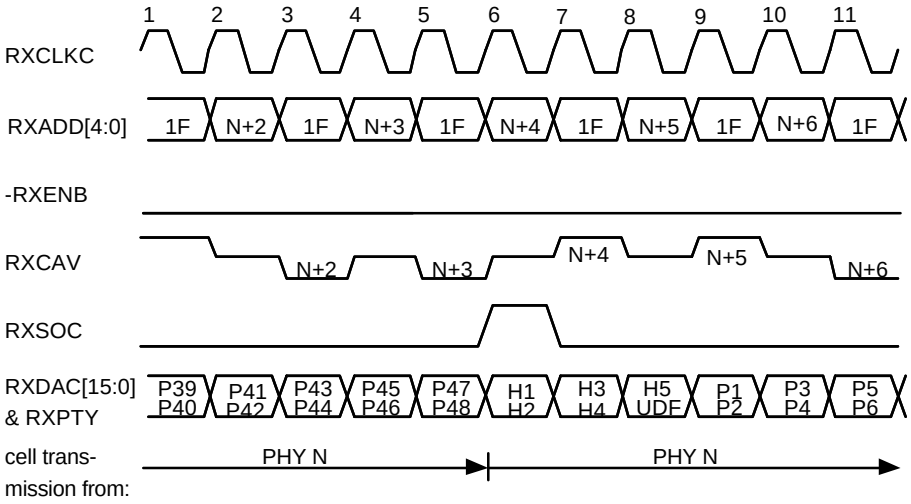


Figure 2.4.15 Two Consecutive Cells from Same PHY

Figure 2.4.16 shows ATM layer stops cell transmission halfway by deasserting -RXENB for three cycles. ATM layer should select the port (in this case port "M") again before restarting cell transmission. ATM layer can continue polling when it suspends cell transmission.

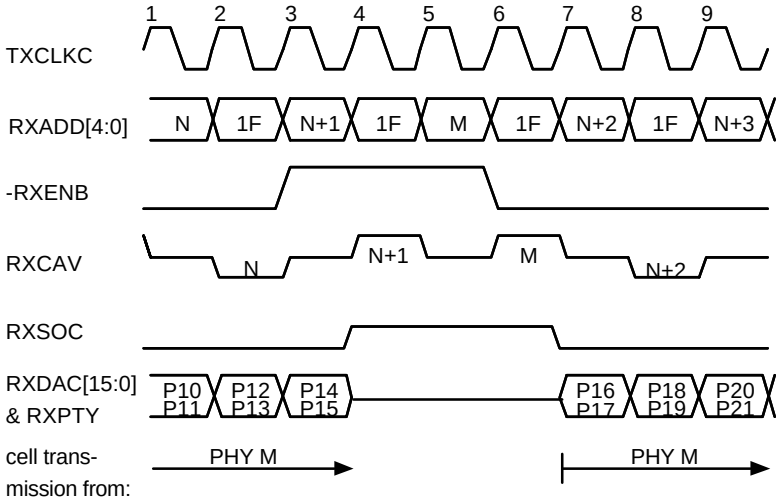


Figure 2.4.16 Cell Transmission From PHY Paused for Three Cycles

2.5 CPU Interface

The host CPU can read/write registers and memories in PLC2 following the procedures described below. The registers can be accessed directly while the internal memories should be accessed indirectly via MEMAL/H and MEMD registers.

(1) Read Access

[With Active ALE]

The CPU puts the read address on address bus A[6:0] and asserts ALE. The valid address on A[6:0] must have setup time (ts_A) and hold time (th_A) to the falling edge of ALE. The data bus D[7:0] is driven by PLC2 when (-CE + -RD) is low. The valid data access time from (-CE + -RD) is defined as td_D. -READY turns valid td_READY after (-CE + -RD) goes low. Then -READY immediately goes low when read access is made to invalid address. Otherwise -READY goes low when the valid data appears on D[7:0].

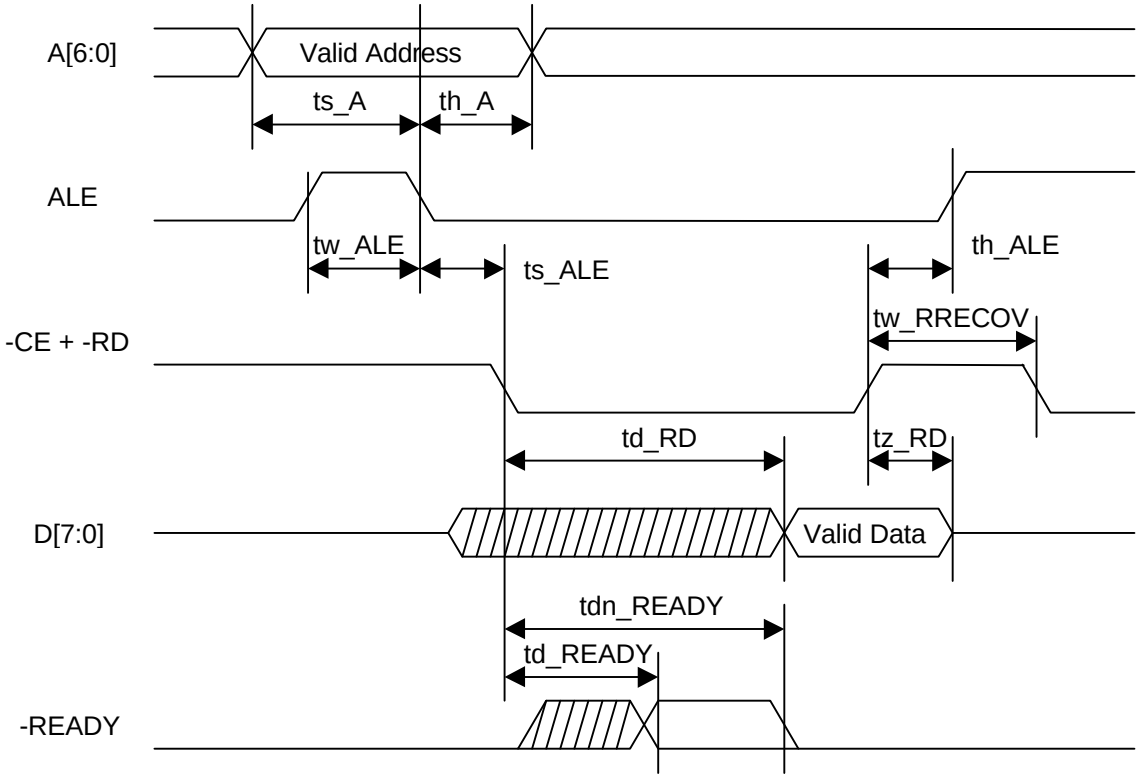


Figure 2.5.1 Host CPU Read Access Timing with Active ALE

[With ALE fixed to High]

The CPU puts the read address on address bus A[6:0]. The valid address on A[6:0] must have setup time (ts_A) to the falling edge of (-CE + -RD) and hold time (th_A) to the rising edge of (-CE + -RD). The data bus D[7:0] is driven by PLC2 when (-CE + -RD) is low. The valid data access time from (-CE + -RD) is defined as td_D. -READY turns valid within td_READY after (-CE + -RD) goes low. Then -READY immediately goes low when read access is made to invalid address. Otherwise -READY goes low when the valid data appears on D[7:0].

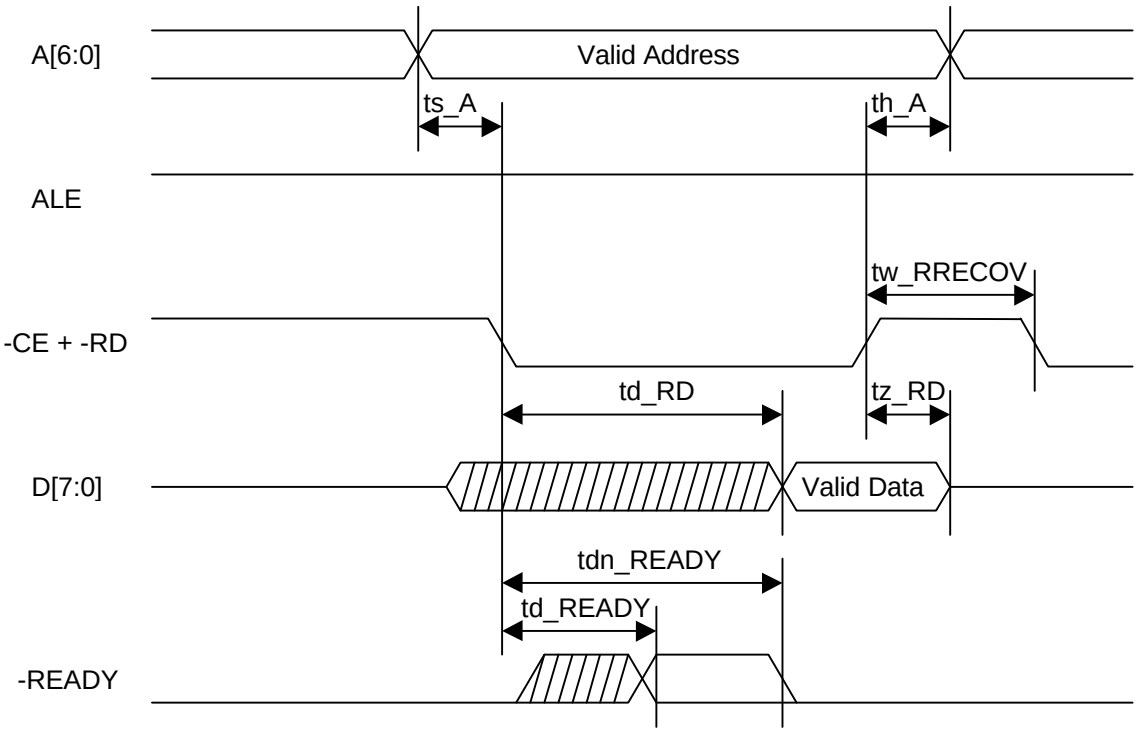


Figure 2.5.2 Host CPU Read Access Timing with Fixed ALE

(2) Write Access

[With Active ALE]

The CPU puts the write address on address bus A[6:0] and deasserts ALE. The valid address on A[6:0] must have setup time (ts_A) and hold time (th_A) to the falling edge of ALE. The valid write data must have setup time ts_D to the falling edge of (-CE + -WR) and hold time th_D from the rising edge of (-CE + -WR). -READY turns valid within td_READY after (-CE + -WR) goes low. Then -READY immediately goes low when write access is made to invalid address. Otherwise -READY goes low when the write access is finished in PLC2. The (-CE + -WR) low pulse must have minimum width tw_CEWR to ensure successful write access.

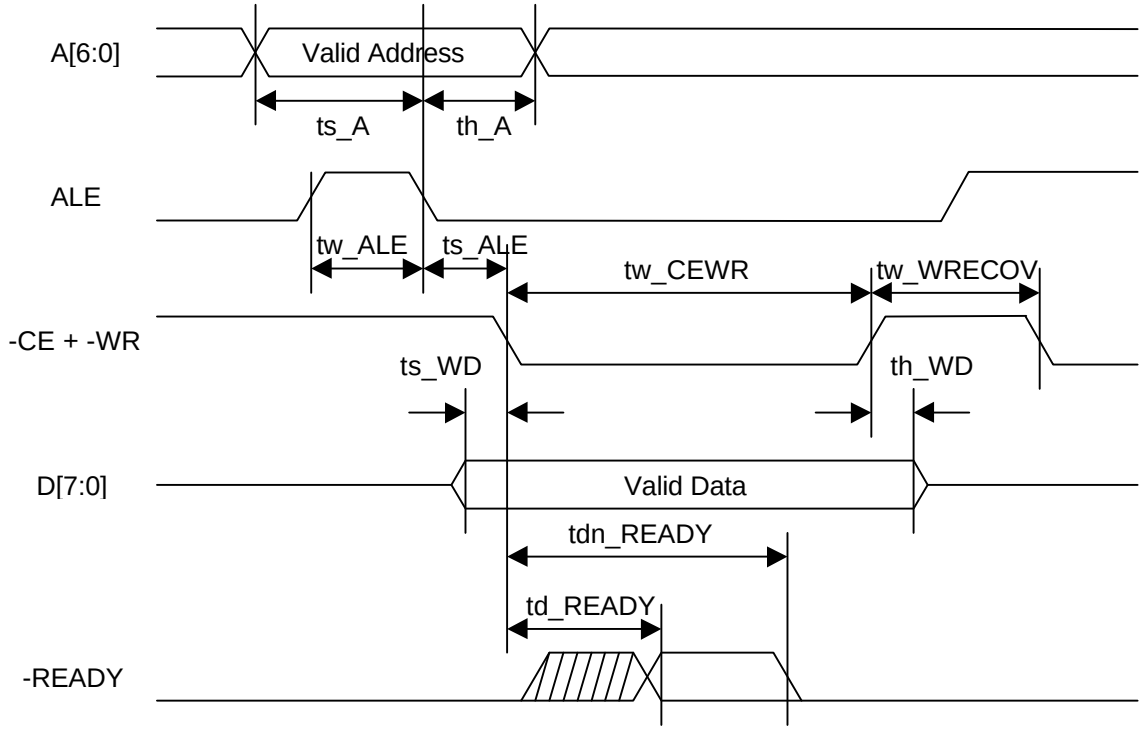


Figure 2.5.3 Host CPU Write Access Timing with Active ALE

[With ALE fixed to High]

The CPU puts the write address on address bus A[6:0]. The valid address on A[6:0] must have setup time (ts_A) to falling edge of (-CE + -WR) and hold time (th_A) to the rising edge of (-CE + -WR). The valid write data must have setup time ts_D to the falling edge of (-CE + -WR) and hold time th_D to the rising edge of (-CE + -WR). -READY turns valid within td_READY after (-CE + -WR) goes low. Then -READY immediately goes low when write access is made to invalid address. Otherwise -READY goes low when the write access is finished in PLC2. The (-CE + -WR) low pulse must have minimum width tw_CEWR to ensure successful write access.

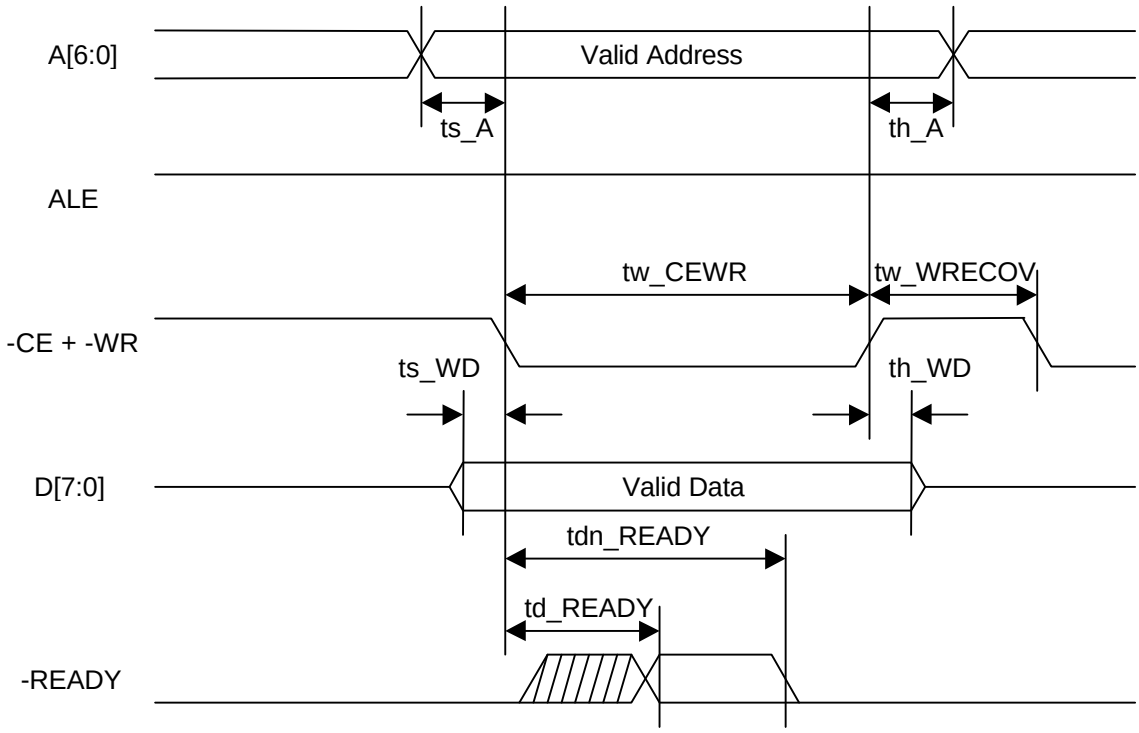


Figure 2.5.4 Host CPU Write Access Timing with Fixed ALE

3 REGISTERS

3.1 Register Map

Following registers can be accessed from the host CPU.

Configuration Registers

Address	Name	Type	Function
00H	CONT	R/W	Reset/Stop of PLC2
01H	FRMS	R/W	Frame Management Register
02H	CMS1	R/W	Cell Management Register 1
03H	CMS2	R/W	Cell Management Register 2
04H	LOOP	R/W	Loop Mode Select
05H	FSYNC	R/W	Frame Synchronization Mode
06H	CSYNC	R/W	Cell Synchronization Mode
07H	LOSCT	R/W	LOS Control Register
08H			Reserved
09H	J1POSH	R/W	Position of J1 Byte in TX Frame (Horizontal)
0AH	J1POSV	R/W	Position of J1 Byte in TX Frame (Vertical)
0BH	CIADR	R/W	Port Address in UTOPIA level 2 Mode
0CH	TXALM1	R/W	Alarm Signal Control 1
0DH	TXALM2	R/W	Alarm Signal Control 2
0EH			Reserved
0FH	CMS3	R/W	Cell Management Register 3

Status Registers

Address	Name	Type	Function
10H	INTSEL1	R/W	Interrupt Control Register 1
11H	INTSEL2	R/W	Interrupt Control Register 2
12H	INTSEL3	R/W	Interrupt Control Register 3
13H			Reserved
14H			Reserved
15H	INTIND1	R/W	Interrupt Status Register 1
16H	INTIND2	R/W	Interrupt Status Register 2
17H	INTIND3	R/W	Interrupt Status Register 3
18H			Reserved
19H			Reserved
1AH	STATUS1	R	Status Register 1
1BH	STATUS2	R	Status Register 2
1CH	STATUS3	R	Status Register 3
1DH			Reserved
1EH			Reserved
1FH	RGFC	R	Receive GFC Status

Error Counters

Address	Name	Type	Function
20H	B1ERRL	R	B1-SBIP8 Error Counter [7:0]
21H	B1ERRH	R	B1-SBIP8 Error Counter [15:8]
22H	B2ERRL	R	B2-LBIP24 Error Counter [7:0]
23H	B2ERRM	R	B2-LBIP24 Error Counter [15:8]
24H	B2ERRH	R	B2-LBIP24 Error Counter [19:16]
25H	B3ERRL	R	B3-PBIP8 Error Counter [7:0]
26H	B3ERRH	R	B3-PBIP8 Error Counter [15:8]
27H	LFEBEL	R	R-LFEBE Counter [7:0]
28H	LFEBEM	R	R-LFEBE Counter [15:8]
29H	LFEBEH	R	R-LFEBE Counter [19:16]
2AH	PFEBEL	R	R-PFEBE Counter[7:0]
2BH	PFEBEH	R	R-PFEBE Counter [15:8]
2FH	FCUPD	R/W	Error Counter Update Flag

Cell Counters

Address	Name	Type	Function
30H	COHER	R	Corrected Cell Header Error Counter
31H	UCHER	R	Uncollected Cell Header Error Counter
32H	RXCCL	R	Receive Valid Cell Counter [7:0]
33H	RXCCM	R	Receive Valid Cell Counter [15:8]
34H	RXCCH	R	Receive Valid Cell Counter [19:16]
35H	TXCCL	R	Transmit Valid Cell Counter [7:0]
36H	TXCCM	R	Transmit Valid Cell Counter [15:8]
37H	TXCCH	R	Transmit Valid Cell Counter [19:16]
3FH	CCUPD	R/W	Cell Counter Update Flag

Memory Access Registers

Address	Name	Type	Function
40H	MEMAL	R/W	Address Register [7:0]
41H	MEMAH	R/W	Address Register [12:8]
42H	MEMD	R/W	Data Register

Test Registers

Address	Name	Type	Function
50H	TSMOD1	R/W	PLC2 Test Mode Register 1
51H	TSMOD2	R/W	PLC2 Test Mode Register 2
52H	TSGEN	R/W	PLC2 Test Mode Register 3
53H	LFEBEI	R/W	PLC2 Test Mode Register 4
54H	PFEBEI	R/W	PLC2 Test Mode Register 5

Hereafter, each register is described in detail. A register field table shows:

Bit Number
Field Name
Default Value on Reset

In register table, "rsvd" means reserved bit.

Address : 00H
Name : CONT
Type : R/W
Function : Reset/Stop of PLC

7	6	5	4	3	2	1	0
AUTOCSE	LOOCDE	PLLINI	OOLDE	TXFRES	RXFRES	STOP	RESET
0	0	0	0	0	0	1	1

RESET

Software reset bit. When this bit is set to one, all the registers and counters are initialized. A hardware reset clears the RESET bit. The RESET bit should be set for at least 10 cycles of the slowest clock provided to PLC2.

0: PLC2 is not held in reset.
1: PLC2 is held in reset.

STOP

Software stop bit. When this bit is set to one, PLC2 stops operation, but does not change the state in PLC2. The host CPU can set value to registers and counters for diagnostic or initialize purpose. The default value of the STOP bit on a hardware reset is 1.

0: PLC2 is not held in stop mode.
1: PLC2 is held in stop mode.

RXFRES

The RXFRES bit controls the state of the receive FIFO. Setting this bit does not corrupt ongoing receive cell transfer. That is, after the last byte of cell has been transferred, the receive FIFO stops operation. The RXFRES bit should be asserted at least 2.7μs for Single-PHY mode and 10.8μs for Multi-PHY mode.

0: The receive FIFO operates normally.
1: All cells in the receive FIFO is discarded. The receive FIFO stops operation.

TXFRES

The TXFRES bit controls the state of the transmit FIFO. Setting this bit affects ongoing transmit cell transfer. That is, after the last byte of the cell has been transferred, the cell is discarded. The TXFRES bit should be asserted at least 2.7μs for Single-PHY mode and 10.8μs for Multi-PHY mode.

0: The transmit FIFO operates normally.
1: All cells in the transmit FIFO is discarded. The transmit FIFO stops operation.

OOLDE

The OOLDE bit controls the out of lock detector.

0: The out of lock detector is disabled.
1: The out of lock detector is enabled.

PLLINI

The PLLINI bit controls the receive PLL.

0: The receive PLL operates normally.
1: The receive PLL locks to reference clock REFCK regardless of other conditions.

LOOCDE

The LOOCDE bit controls the internal loss of optical carrier detector.

0: The loss of optical carrier detector is disabled.
1: The loss of optical carrier detector is enabled.

AUTOCSE

The AUTOCSE controls receive PLL.

0: Receive PLL recovers clock from receive data or generates x8 clock from REFCK depending on the state of REFSEL.

1: Receive PLL usually recovers clock from receive data. When LOOC input is tied high or no signal transition is detected for 80 bit period or recovered clock deviates more than 244 ppm from reference clock, the receive PLL automatically switches reference source from receive data to reference clock, as far as REFSEL is tied low. The receive PLL locks to REFCK when REFSEL is tied high regardless of AUTOCSE bit.

Address : 01H
Type : R/W
Name : FRMS
Function : Frame management

7	6	5	4	3	2	1	0
rsvd	SDH	J1	NODSBF	NOSCBF	NOSTF	TC1	TC0
–	0	0	0	0	0	0	0

TC1, TC0

The TC1 and TC0 define the transmission frame.

TC1	TC0	Frame
0	Don't care	STS-3c/STM-1
1	0	STS-1
1	1	STS-1/2

NOSTF

The NOSTF bit selects stuff byte mode in STS-1 operation.
0: Columns 30 and 59 are treated as fixed bytes in STS-1 operation.
1: Columns 30 and 59 are treated as data bytes in STS-1 operation.

NOSCBF

The NOSCBF bit controls the scramble of transmit frame.
0: Enable the scramble of transmit frame.
1: Disable the scramble of transmit frame.

NODSBF

The NODSBF bit controls the descramble of receive frame.
0: Enable the descramble.
1: Disable the descramble.

J1

The J1 bit controls the J1 byte insertion of transmit frame.
0: The J1 byte of transmit frame is fixed to 00H.
1: 64 bytes character code stored in the transmit overhead memory is inserted to J1 bytes cyclically.

SDH

The SDH bit controls PLC2 operation in terms of the difference between SONET and SDH.
0: PLC2 operates in SONET mode.
1: PLC2 operates in SDH mode.

The difference of operation by PLC2 between SONET/SDH is summarized below.

	SONET mode	SDH mode
C1 bytes in transmit frame	01H/02H/03H	01H/AAH/AAH
SS bits of H1 byte in transmit frame	'00'	'10'
L-RDI detection	5 consecutive frames	3 consecutive frames
L-AIS detection	5 consecutive frames	3 consecutive frames
P-RDI detection	10 consecutive frames	3 consecutive frames

(Notice: P-AIS detection criteria is 3 consecutive frames both for SONET and SDH.)

Address : 02H
Type : R/W
Name : CMS1
Function : Cell Management Register 1

7	6	5	4	3	2	1	0
UAC	TXF2	TXF1	UDF	PARITY	DIRECT	WIDTH	UTOPIA
0	0	0	0	0	0	0	0

UTOPIA

The UTOPIA bit selects UTOPIA mode.

0: Single-PHY
1: Multi-PHY

WIDTH

The WIDTH bit selects UTOPIA I/F data bus width.

0: 8 bit Data Bus (for Single-PHY or Multi-PHY mode)
1: 16 bit Data Bus (for Multi-PHY mode only)

DIRECT

The DIRECT bit enables direct status mode in Multi-PHY mode.

0: Normal mode
1: Direct Status mode

PARITY

The PARITY bit selects parity mode.

0: Odd Parity
1: Even Parity

UDF

The UDF bit controls HEC insertion in 16 bit cell format.

0: UDF1 for HEC
1: UDF2 for HEC

TXF2/TXF1

The TXF2/TXF1 bits control the transmit FIFO depth.

TXF2	TXF1	FIFO Depth
0	0	4 cell deep
0	1	1 cell deep
1	0	2 cell deep
1	1	3 cell deep

UAC

The UAC bit controls idle/unassigned cell insertion.

0: When there is no cell in transmit FIFO, idle cells are inserted into transmit frame.
1: When there is no cell in transmit FIFO, unassigned cells with GFC field set to ‘0001’ are inserted into transmit frame.

Address : 03H
Type : R/W
Name : CMS2
Function : Cell Management Register 2

7	6	5	4	3	2	1	0
GFCEN	NOTC	NOSCBC	NOHEC	NORC	NODSBC	PASS	DROP
0	0	0	0	0	0	0	0

DROP

The DROP bit controls the cell delineation.

0: Normal cell delineation as specified in ITU-T I.432.
1: All received cells with header error are discarded.

PASS

The PASS bit controls the cell delineation.

0: Normal cell delineation as specified in ITU-T I.432.
1: All cells are passed, regardless of header error, toward ATM layer. The cell delineation state transition is treated as specified in ITU-T I.432.

NODSBC

The NODSBC bit controls descramble of received cell.

0: Enable the payload descramble of received cell.
1: Disable the payload descramble of received cell.

NORC

The NORC bit controls HEC calculation option of received cell.

0: The coset polynomial, $X^6+X^4+X^2+1$, is added(modulo 2) in HEC calculation of received cell.
1: No polynomial is added

NOHEC

The NOHEC bit controls HEC calculation of transmit cell.

0: Enable calculation and insertion of HEC of transmit cell and.
1: Disable calculation and insertion of HEC of transmit cell. The HEC field of transmit cell is as received from ATM layer.

NOSCBC

The NOSCBC bit controls payload scramble of transmit cell.

0: Enable the payload scramble of transmit cell.
1: Disable the payload scramble of transmit cell.

NOTC

The NOTC bit controls HEC calculation option of transmit cell.

0: The coset polynomial, $X^6+X^4+X^2+1$('55H'), is added(modulo 2) in HEC calculation of transmit cell.
1: No polynomial is added

GFCEN

The GFCEN bit controls limited GFC function. When GFC field of received cell indicates 'HALT' ("1xxx"), PLC2 can withhold the transmission of valid cells. When valid cells are withheld, IDLE cells are transmitted instead.

0: Disable GFC control
1: Enable GFC control

Address : 04H
Type : R/W
Name : LOOP
Function : Loop mode select

7	6	5	4	3	2	1	0
rsvd	rsvd	LOOP2EN	LOOPL	LOOPT	LOOPU	LOOP2	LOOP1
–	–	0	0	0	0	0	0

LOOP1

The LOOP1 bit controls diagnostic loop back mode in LSI side. When this bit is set to one, TXDOP/M is connected to RXDIP/M internally so that the transmit serial data is just returned as the receive serial data.

0: Disable diagnostic loop back.
1: Enable diagnostic loop back.

LOOP2

The LOOP2 bit controls deep line loop back mode. When this bit is set to one, receive data input to RXDIP/M is put through RX serial to parallel converter and then to TX parallel to serial converter and output on TXDOP/M.

0: Disable deep line loop back.
1: Enable deep line loop back.

LOOPU

The LOOPU bit controls UTOPIA loop back mode. When this bit is set to one, transmit parallel data is looped back to the receive parallel input.

0 Disable UTOPIA loop back mode.
1: Enable UTOPIA loop back mode.

LOOPT

When the LOOPT bit is set to one, transmit clock of PLC2 is synchronized with a clock extracted from received data. (Loop Timing Mode)

0 Disable Loop Timing Mode. The transmit clock is synchronized with the reference clock, REFCK.
1: Enable Loop Timing Mode

LOOPL

The LOOPL bit controls the shallow line loop back mode. When this bit is set to one, RXDIP/M input is directly looped back to TXDOP/M.

0: Disable shallow line loop back.
1: Enable shallow line loop back.

LOOP2EN

The LOOP2EN bit determines whether the internal receive processor can set LOOP2 bit.

0: The internal receive processor cannot set or reset LOOP2 bit of LOOP register.
1: The internal receive processor can set and reset LOOP2 bit of LOOP register.

Address : 05H
Type : R/W
Name : FSYNC
Function : Frame Synchronization control

7	6	5	4	3	2	1	0
rsvd	FRWDF[2:0]			rsvd	BKWDF[2:0]		
–	1	0	0	–	0	1	0

FRWDF[2:0]

The FRWD [2:0] field is set to the number ‘N’ of forward protection of frame synchronization. When PLC2 loses ‘N’ times of frame synchronization in ‘SYNC’ mode, PLC2 moves to ‘HUNT’ mode.

BKWDF[2:0]

The BKWD [2:0] field is set to the number ‘M’ of backward protection of frame synchronization. When PLC2 catches ‘M’ times of frame synchronization in ‘HUNT’ mode, PLC2 moves to ‘SYNC’ mode.

Address : 06H
Type : R/W
Name : CSYNC
Function : Cell Synchronization Mode

7	6	5	4	3	2	1	0
rsvd	FRWDC[2:0]			rsvd	BKWDC[2:0]		
–	1	1	1	–	1	1	1

FRWDC[2:0]

This field are set to the number ‘N’ of forward protection of cell synchronization. When PLC2 loses ‘N’ times of cell synchronization in ‘SYNC’ mode, PLC2 moves to ‘HUNT’ mode.

BKWDC[2:0]

This field are set to the number ‘M’ of backward protection of cell synchronization. When PLC2 catches ‘M’ times of cell synchronization in ‘HUNT’ mode, PLC2 moves to ‘SYNC’ mode.

Address : 07H
Type : R/W
Name : LOSCT
Function : LOS control register

7	6	5	4	3	2	1	0
rsvd	rsvd	rsvd	rsvd	rsvd	rsvd	rsvd	EXTLOS
–	–	–	–	–	–	–	0

EXTLOS

The EXTLOS bit controls whether LOOCP/M input affects LOS status.

0: When LOOCP/M input is high, RXDIP/M input is fixed to low.
1: LOOCP/M input has no effect on PLC2 LOS detection.

Address : 09H
Type : R/W
Name : J1POSH
Function : Horizontal position of J1 byte in transmit frame

7	6	5	4	3	2	1	0
rsvd	J1H[6:0]						
–	0	0	0	0	0	1	1

Address : 0AH
Type : R/W
Name : J1POSV
Function : Vertical position of J1 byte of transmit frame

7	6	5	4	3	2	1	0
rsvd	rsvd	rsvd	rsvd	J1V[3:0]			
–	–	–	–	0	0	1	1

J1H[6:0]
This register is used only for diagnostic purpose.

J1V[3:0]
This register is used only for diagnostic purpose.

NOTE: The default values of J1H and J1V correspond to pointer 0 on H1 and H2 bytes.

Address : 0BH
Type : R/W
Name : CIADR
Function : Port Address in Multi-PHY mode

7	6	5	4	3	2	1	0
rsvd	rsvd	rsvd	ADDR[4:0]				
–	–	–	1	1	1	1	1

ADDR[4:0]

When PLC2 operates in Multi-PHY mode, ADDR [4:0] is used as physical port address of this device.

Address : 0CH
Type : R/W
Name : TXALM1
Function : Alarm signal control 1

7	6	5	4	3	2	1	0
rsvd	rsvd	rsvd	rsvd	PAIS	PRDI	LAIS	LRDI
–	–	–	–	0	1	0	1

PLC2 can send following alarm status automatically by setting this field.

LRDI

The LRDI bit controls automatic transmission of Line RDI.
0: Disable the automatic transmission
1: Enable automatic transmission, when PLC2 detects LOS, LOF or LAIS.

LAIS

The LAIS bit controls automatic transmission of Line AIS.
0: Disable the automatic transmission
1: Enable automatic transmission, when PLC2 detects LOS or LOF.

PRDI

The PRDI bit controls automatic transmission of Path RDI.
0: Disable the automatic transmission
1: Enable automatic transmission, when PLC2 detects LOS, LOF, LOP, LOC, LAIS or PAIS.

PAIS

The PAIS bit controls automatic transmission of Path AIS.
0: Disable the automatic transmission
1: Enable automatic transmission, when PLC2 detects LOS, LOF, LOP, LOC or LAIS.

NOTE: When automatic alarm transmission is used by setting this register, corresponding bit of TXALM2 register must be set to zero.

Address : 0DH
Type : R/W
Name : TXALM2
Function : Alarm signal control 2

7	6	5	4	3	2	1	0
rsvd	rsvd	rsvd	rsvd	PAIS	PRDI	LAIS	LRDI
–	–	–	–	0	0	0	0

PLC2 can be forced to send following alarm signals by using this field. While each bit is set to one, PLC2 continues to send corresponding alarm signal.

LRDI

The LRDI bit controls forced transmission of Line RDI.

0: Stop sending L-RDI
1: Start Sending L-RDI

LAIS

The LAIS bit controls forced transmission of Line AIS.

0: Stop sending L-AIS
1: Start sending L-AIS

PRDI

The PRDI bit controls forced transmission of Path RDI.

0: Stop sending P-RDI
1: Start sending P-RDI

PAIS

The PAIS bit controls forced transmission of Path AIS.

0: Stop sending P-AIS
1: Start sending P-AIS

NOTE: When the forced alarm transmission is used by setting this register, corresponding bit of TXALM1 register must be set to zero.

Address : 0FH
Type : R/W
Name : CMS3
Function : Cell Management Register 3

7	6	5	4	3	2	1	0
TGFC[3:0]				OPT	rsvd	rsvd	TGFCEN
0	0	0	0	0	–	–	0

TGFCEN

The TGFCEN controls whether to insert TGFC[3:0] to GFC field of every assigned cell to transmit.

0: GFC field of assigned cell to transmit is not changed.
1: TGFC [3:0] is inserted to GFC field of every assigned cell to transmit.

OPT

The OPT bit controls GFC field of unassigned cell generated in PLC2.

0: Pattern ‘0001’ is inserted to GFC field of unassigned cell generated in PLC2.
1: TGFC [3:0] is inserted to GFC field of unassigned cell generated in PLC2.

TGFC [3:0]

When TGFCEN is set, TGFC [3:0] is inserted to GFC field of every assigned cell to transmit.

Address : 10H
Type : R/W
Name : INTSEL1
Function : Interrupt Control Register of STATUS1

7	6	5	4	3	2	1	0
B3	B2	B1	LOC	LOP	LOF	OOF	LOS
0	0	0	0	0	0	0	0

Each bit of INTSEL1 register controls interrupt generation of corresponding bit of STATUS1 register.

LOS

The LOS bit controls LOS interrupt.
0: Disable an interrupt generation
1: Enable an interrupt generation, when Loss of Signal status change is detected

OOF

The OOF bit controls OOF interrupt.
0: Disable an interrupt generation
1: Enable an interrupt generation, when Out of Frame status change is detected

LOF

The LOF bit controls LOF interrupt.
0: Disable an interrupt generation
1: Enable an interrupt generation, when Loss of Frame status change is detected

LOP

The LOP bit controls LOP interrupt.
0: Disable an interrupt generation
1: Enable an interrupt generation, when Loss of Pointer status change is detected

LOC

The LOC bit controls LOC interrupt.
0: Disable an interrupt generation
1: Enable an interrupt generation, when Loss of Cell delineation status change is detected

B1

The B1 bit controls B1 interrupt.
0: Disable an interrupt generation
1: Enable an interrupt generation, when B1-SBIP8 error is detected

B2

The B2 bit controls B2 interrupt.
0: Disable an interrupt generation
1: Enable an interrupt generation, when B2-LBIP24 error is detected

B3

The B3 bit controls B3 interrupt.
0: Disable an interrupt generation
1: Enable an interrupt generation, when B3-PBIP8 error is detected

Address : 11H
Type : R/W
Name : INTSEL2
Function : Interrupt Control Register 2

7	6	5	4	3	2	1	0
C2	PFEBE	LFEBE	rsvd	PAIS	PRDI	LAIS	LRDI
0	0	0	–	0	0	0	0

Each bit of INTSEL2 register controls interrupt generation of corresponding bit of STATUS2 register.

LRDI

The LRDI bit controls LRDI interrupt.
0: Disable an interrupt generation
1: Enable an interrupt generation, when Line-RDI status changes

LAIS

The LAIS bit controls LAIS interrupt.
0: Disable an interrupt generation
1: Enable an interrupt generation, when Line-AIS status changes

PRDI

The PRDI bit controls PRDI interrupt.
0: Disable an interrupt generation
1: Enable an interrupt generation, when Path-RDI status changes

PAIS

The PAIS bit controls Path AIS interrupt.
0: Disable an interrupt generation
1: Enable an interrupt generation, when Path-AIS status changes

LFEBE

The LFEBE bit controls Line FEBE interrupt.
0: Disable an interrupt generation
1: Enable an interrupt generation, when Line-FEBE is detected

PFEBE

The PFEBE bit controls Path FEBE interrupt.
0: Disable an interrupt generation
1: Enable an interrupt generation, when Path-FEBE is detected

C2

The C2 bit controls C2 interrupt.
0: Disable an interrupt generation
1: Enable an interrupt generation, when C2 error is detected

Address : 12H
Type : R/W
Name : INTSEL3
Function : Interrupt Control Register 3

7	6	5	4	3	2	1	0
LOOC	GFC	TXOOL	RXOOL	UCH	COH	PTY	RFOV
0	0	0	0	0	0	0	0

Each bit of INTSEL3 register controls interrupt generation of corresponding bit of STATUS3 register.

RFOV
0: Disable an interrupt generation.
1: Enable an interrupt generation, when receive FIFO overflow is detected.

PTY
0: Disable an interrupt generation.
1: Enable an interrupt generation, when parity error is detected.

COH
0: Disable an interrupt generation.
1: Enable an interrupt generation, when PLC2 corrected a single bit header error.

UCH
0: Disable an interrupt generation.
1: Enable an interrupt generation, when PLC2 detects uncorrectable header error.

RXOOL
0: Disable an interrupt generation.
1: Enable an interrupt generation, when the receive PLL gets out of lock.

TXOOL
0: Disable an interrupt generation.
1: Enable an interrupt generation, when the transmit PLL gets out of lock.

GFC
0: Disable an interrupt generation.
1: Enable an interrupt generation, when PLC2 detects a command in GFC field of received cell.

LOOC
0: Disable an interrupt generation.
1: Enable an interrupt generation, when PLC2 detects logical high level at LOOCP/M input.

Address : 15H
Type : R/W
Name : INTIND1
Function : Interrupt Status Register 1

7	6	5	4	3	2	1	0
B3	B2	B1	LOC	LOP	LOF	OOF	LOS
0	0	0	0	0	0	0	0

INTIND1 register indicates interrupt status, when PLC2 generates an interrupt. Each bit of this register is one, when corresponding status of STATUS1 register has any transition or transition to 1. The host CPU can find interrupt cause by reading this register, when interrupt is occurred. Each bit is cleared when 0 is written by the host CPU.

LOS
0: Indicates no transition in LOS status.
1: Indicates transition in LOS status.

OOF
0: Indicates no transition in OOF status.
1: Indicates transition in OOF status.

LOF
0: Indicates no transition in LOF status.
1: Indicates transition in LOF status.

LOP
0: Indicates no transition in LOP status.
1: Indicates transition in LOP status.

LOC
0: Indicates no transition in LOC status.
1: Indicates transition in LOC status.

B1
0: Indicates no transition to 1 in B1 status.
1: Indicates transition to 1 in B1 status.

B2
0: Indicates no transition to 1 in B2 status.
1: Indicates transition to 1 in B2 status.

B3
0: Indicates no transition to 1 in B3 status.
1: Indicates transition to 1 in B3 status.

Address : 16H
Type : R/W
Name : INTIND2
Function : Interrupt Status Register 2

7	6	5	4	3	2	1	0
C2	PFEBE	LFEBE	rsvd	PAIS	PRDI	LAIS	LRDI
0	0	0	–	0	0	0	0

INTIND2 register indicates interrupt status, when PLC2 generates an interrupt. Each bit of this register is one, when corresponding status of STATUS2 register has any transition or transition to 1. The host CPU can find interrupt cause by reading this register, when interrupt is occurred. Each bit is cleared when 0 is written by the host CPU.

LRDI
0: Indicates no transition in LRDI status.
1: Indicates transition in LRDI status.

LAIS
0: Indicates no transition in LAIS status.
1: Indicates transition in LAIS status.

PRDI
0: Indicates no transition in PRDI status.
1: Indicates transition in PRDI status.

PAIS
0: Indicates no transition in PAIS status.
1: Indicates transition in PAIS status.

LFEBE
0: Indicates no transition to 1 in LFEBE status.
1: Indicates transition to 1 in LFEBE status.

PFEBE
0: Indicates no transition to 1 in PFEBE status.
1: Indicates transition to 1 in PFEBE status.

C2
0: Indicates no transition to 1 in C2 status.
1: Indicates transition to 1 in C2 status.

Address : 17H
Type : R/W
Name : INTIND3
Function : Interrupt Status Register 3

7	6	5	4	3	2	1	0
LOOC	GFC	TXOOL	RXOOL	UCH	COH	PTY	RFOV
0	0	0	0	0	0	0	0

INTIND3 register indicates interrupt status, when PLC2 generates an interrupt. Each bit of this register is one, when corresponding status of STATUS3 register has any transition or transition to 1. The host CPU can find interrupt cause by reading this register, when interrupt is occurred. Each bit is cleared when 0 is written by the host CPU.

RFOV
0: Indicates no transition to 1 in RFOV status.
1: Indicates transition to 1 in RFOV status.

COH
0: Indicates no transition to 1 in COH status.
1: Indicates transition to 1 in COH status.

UCH
0: Indicates no transition to 1 in UCH status.
1: Indicates transition to 1 in UCH status.

RXOOL
0: Indicates no transition in RXOOL status.
1: Indicates transition in RXOOL status.

TXOOL
0: Indicates no transition in TXOOL status.
1: Indicates transition in TXOOL status.

GFC
0: Indicates no transition to 1 in GFC status.
1: Indicates transition to 1 in GFC status.

LOOC
0: Indicates no transition to 1 in LOOC status.
1: Indicates transition to 1 in LOOC status.

Address : 1AH
Type : R
Name : STATUS1
Function : Receive Status Register

7	6	5	4	3	2	1	0
B3	B2	B1	LOC	LOP	LOF	OOF	LOS
0	0	0	0	0	0	0	0

LOS

This bit indicates status of Loss of Signal. When LOS is detected, PLC2 sets this field to one. When LOS condition disappears, this bit is cleared.

OOF

This bit indicates status of Out of Frame. When OOF is detected, PLC2 sets this bit to one. When OOF condition disappears, this bit is cleared.

LOF

This bit indicates status of Loss of Frame. When LOF is detected, PLC2 sets this bit to one. When LOF condition disappears, this bit is cleared.

LOP

This bit indicates status of Loss of Pointer. When LOP is detected, PLC2 sets this bit to one. When LOP condition disappears, this bit is cleared.

LOC

This bit indicates status of Loss of Cell delineation. When LOC is detected, PLC2 sets this bit to one. When LOC condition disappears, this bit is cleared.

B1

This bit indicates B1-SBIP8 error of receiving frame. When B1-SBIP8 error is detected, PLC2 sets this bit to one. When B1-SBIP8 error is not detected in next frame, this bit is cleared.

B2

This bit indicates B2-LBIP24 error of receiving frame. When B2-LBIP24 error is detected, PLC2 sets this bit to one. When B2-LBIP24 error is not detected in next frame, this bit is cleared.

B3

This bit indicates B3-PBIP8 error of receiving frame. When B3-PBIP8 error is detected, PLC2 sets this bit to one. When B3-PBIP8 error is not detected in next frame, this bit is cleared.

NOTE: This register indicates current status. It is not cleared when accessed by host CPU.

Address : 1BH
Type : R
Name : STATUS2
Function : Alarm Status Register

7	6	5	4	3	2	1	0
C2	PFEBE	LFEBE	rsvd	PAIS	PRDI	LAIS	LRDI
0	0	0	–	0	0	0	0

LRDI

This bit indicates L-RDI state of receiving frame. When L-RDI is judged to be set, PLC2 sets this bit to one. When L-RDI is judged to be reset, this bit is cleared.

LAIS

This bit indicates L-AIS state of receiving frame. When L-AIS is judged to be set , PLC2 sets this bit to one. When L-AIS is judged to be reset, this bit is cleared.

PRDI

This bit indicates P-RDI state of receiving frame. When P-RDI is judged to be set, PLC2 sets this bit to one. When P-RDI is judged to be reset, this bit is cleared.

PAIS

This bit indicates P-AIS state of receiving frame. When P-AIS is judged to be set, PLC2 sets this bit to one. When P-AIS is judged to be reset, this bit is cleared.

LFEBE

This bit indicates L-FEBE state of receiving frame. When received L-FEBE is non-zero, PLC2 sets this bit to one. When received L-FEBE is zero, this bit is cleared.

PFEBE

This bit indicates P-FEBE state of receiving frame. When received P-FEBE is non-zero, PLC2 sets this bit to one. When received P-FEBE is zero, this bit is cleared.

C2

This bit indicates C2 error of receiving frame. When C2 error is detected, PLC2 sets this bit to one. When C2 error is not detected in next frame or later, this bit is cleared.

NOTE: This register indicates current status. It is not cleared when accessed by host CPU.

Address : 1CH
Type : R
Name : STATUS3
Function : PLC2 Internal Status

7	6	5	4	3	2	1	0
LOOC	GFC	TXOOL	RXOOL	UCH	COH	PTY	RFOV
0	0	0	0	0	0	0	0

RFOV

When the receive FIFO overflow is detected, PLC2 sets this bit to one. When the receive FIFO overflow is cleared, PLC2 sets this bit to zero.

PTY

When PLC2 detects parity error in received cell at transmit side cell interface, this bit is set to one. When PLC2 detects normal parity, this bit is cleared.

COH

When PLC2 corrected a single bit header error in a receiving cell, this bit is set to one. When the following cell has normal header or uncorrectable header, this bit is set to zero.

UCH

When PLC2 detects uncorrectable header error in receiving cell, this bit is set to one. When the allowing cell has normal header or correctable single bit error, this bit is set to zero.

RXOOL

When the receive PLL is out of lock, this bit is set to one. When the receive PLL is in lock, this bit is set to zero.

TXOOL

When the transmit PLL is out of lock, this bit is set to one. When the transmit PLL is in lock, this bit is set to zero.

GFC

When PLC2 detects GFC commands (1xxx, x1xx or xx1x) in GFC field of received cell, PLC2 sets this bit to one. When PLC2 detects "000x" in GFC field of received cell, PLC2 sets this bit to zero.

LOOC

When PLC2 detects logical high level at LOOCP/M input, PLC2 sets this bit to one. When PLC2 detects logical low level at LOOCP/M input, PLC2 sets this bit to zero.

NOTE: This register indicates current status. It is not cleared when accessed by host CPU.

Address : 1FH
Type : R
Name : RGFC
Function : Receive GFC Status

7	6	5	4	3	2	1	0
rsvd	rsvd	rsvd	rsvd	RGFC[3:0]			
–	–	–	–	0	0	0	0

RGFC[3:0]

RGFC[3:0] indicates GFC field of received cell. It is updated when GFC field of the current cell is different from the preceding one.

Address : 20H
Type : R
Name : B1ERRL
Function : B1-SBIP8 error counter [7:0]

7	6	5	4	3	2	1	0
B1ERR[7:0]							
0	0	0	0	0	0	0	0

Address : 21H
Type : R
Name : B1ERRH
Function : B1-SBIP8 error counter [15:8]

7	6	5	4	3	2	1	0
B1ERR[15:8]							
0	0	0	0	0	0	0	0

This register indicates B1-SBIP8 error count. When B1 bit of FCUPD register is set to one, this counter is updated within 150μs and B1 bit is automatically cleared. The value of this counter is kept until next update request. The B1-SBIP8 count stops when 4 MSB bits reach '1111'.

Address : 22H
Type : R
Name : B2ERRL
Function : B2-LBIP24 error counter[7:0]

7	6	5	4	3	2	1	0
B2ERR[7:0]							
0	0	0	0	0	0	0	0

Address : 23H
Type : R
Name : B2ERRM
Function : B2-LBIP24 error counter[15:8]

7	6	5	4	3	2	1	0
B2ERR[15:8]							
0	0	0	0	0	0	0	0

Address : 24H
Type : R
Name : B2ERRH
Function : B2-LBIP24 error counter[19:16]

7	6	5	4	3	2	1	0
rsvd	rsvd	rsvd	rsvd	B2ERR[19:16]			
–	–	–	–	0	0	0	0

This register indicates B2-LBIP24 error count. When B2 bit of FCUPD register is set to one, this counter is updated within 150μs and B2 bit is automatically cleared. The value of this counter is kept until next update request. The B2-LBIP24 count stops when 4 MSB bits reach '1111'.

Address : 25H
Type : R
Name : B3ERRL
Function : B3-PBIP8 error counter[7:0]

7	6	5	4	3	2	1	0
B3ERR[7:0]							
0	0	0	0	0	0	0	0

Address : 26H
Type : R
Name : B3ERRH
Function : B3-PBIP8 error counter[15:8]

7	6	5	4	3	2	1	0
B3ERR[15:8]							
0	0	0	0	0	0	0	0

This register indicates B3-PBIP8 error count. When B3 bit of FCUPD register is set to one, this counter is updated within 150μs and B3 bit is automatically cleared. The value of this counter is kept until next update request. The B3-PBIP8 count stops when 4 MSB bits reach '1111'.

Address : 27H
Type : R
Name : LFEBEL
Function : Receive LFEBE counter[7:0]

7	6	5	4	3	2	1	0
LFEBE[7:0]							
0	0	0	0	0	0	0	0

Address : 28H
Type : R
Name : LFEBEM
Function : Receive LFEBE counter[15:8]

7	6	5	4	3	2	1	0
LFEBE[15:8]							
0	0	0	0	0	0	0	0

Address : 29H
Type : R
Name : LFEBEH
Function : Receive LFEBE counter[19:16]

7	6	5	4	3	2	1	0
rsvd	rsvd	rsvd	rsvd	LFEBE[19:16]			
–	–	–	–	0	0	0	0

This register indicates receive L-FEBE count. When LFEBE bit of FCUPD register is set to one, this counter is updated within 150μs and LFEBE bit is automatically cleared. The value of this counter is kept until next update request. The L-FEBE count stops when 4 MSB bits reach '1111'.

Address : 2AH
Type : R
Name : PFEBEL
Function : Receive PFEBE counter[7:0]

7	6	5	4	3	2	1	0
PFEBE[7:0]							
0	0	0	0	0	0	0	0

Address : 2BH
Type : R
Name : PFEBEH
Function : Receive PFEBE counter[15:8]

7	6	5	4	3	2	1	0
PFEBE[15:8]							
0	0	0	0	0	0	0	0

This register indicates received P-FEBE count. When PFEBE bit of FCUPD register is set to one, this counter is updated within 150μs and PFEBE bit is automatically cleared. The value of this counter is kept until next update request. The P-FEBE count stops when 4 MSB bits reach '1111'.

Address : 2FH
Type : R/W
Name : FCUPD
Function : Error Counter update flag

7	6	5	4	3	2	1	0
rsvd	rsvd	rsvd	PFEBE	LFEBE	B3	B2	B1
–	–	–	0	0	0	0	0

B1

Update control of B1ERRL/H registers

0: No operation

1: Internal B1-SBIP8 error count is loaded into B1ERRL/H registers within 150 μs and B1 bit is cleared automatically.

B2

Update control of B2ERRL/M/H registers

0: No operation

1: Internal B2-LBIP24 error count is loaded into B2ERRL/M/H registers within 150 μs and B2 bit is cleared automatically.

B3

Update control of B3ERRL/H registers

0: No operation

1: Internal B3-PBIP8 error count is loaded into B3ERRL/H registers within 150 μs and B3 bit is cleared automatically.

LFEBE

Update control of LFEBEL/M/H registers

0: No operation

1: Internal LFEBE count is loaded into LFEBEL/M/H registers within 150 μs and LFEBE bit is cleared automatically.

PFEBE

Update control of PFEBEL/H registers.

0: No operation

1: Internal PFEBE count is loaded into PFEBEL/H registers within 150 μs and PFEBE bit is cleared automatically.

Address : 30H
Type : R
Name : COHER
Function : Corrected Cell Header Error Counter

7	6	5	4	3	2	1	0
COHER[7:0]							
0	0	0	0	0	0	0	0

The COHER register indicates count of corrected header error. This register is cleared automatically on read. The error count stops when the count reach $255_{(10)}$. When header error correction is disabled, COHER register has no meaning.

Address : 31H
Type : R
Name : UCHER
Function : Uncorrected Cell Header Error counter

7	6	5	4	3	2	1	0
UCHER[7:0]							
0	0	0	0	0	0	0	0

The UCHER register indicates count of uncorrected header error. This register is cleared automatically on read. The error count stops when the count reach 255(10).

Address : 32H
Type : R
Name : RXCCL
Function : Receive valid cell counter[7:0]

7	6	5	4	3	2	1	0
RXCC[7:0]							
0	0	0	0	0	0	0	0

Address : 33H
Type : R
Name : RXCCM
Function : Receive valid cell counter[15:8]

7	6	5	4	3	2	1	0
RXCC[15:8]							
0	0	0	0	0	0	0	0

Address : 34H
Type : R
Name : RXCCH
Function : Receive valid cell counter[19:16]

7	6	5	4	3	2	1	0
rsvd	rsvd	rsvd	rsvd	RXCC[19:16]			
–	–	–	–	0	0	0	0

This register indicates received valid cell count. When RXCC bit of CCUPD register is set to one, this counter is updated within 1μs. The value of this counter is kept until next update. The receive valid cell count stops when 4 MSB bits reach '1111'.

Address : 35H
Type : R
Name : TXCCL
Function : Transmit valid cell counter[7:0]

7	6	5	4	3	2	1	0
TXCC[7:0]							
0	0	0	0	0	0	0	0

Address : 36H
Type : R
Name : TXCCM
Function : Transmit valid cell counter[15:8]

7	6	5	4	3	2	1	0
TXCC[15:8]							
0	0	0	0	0	0	0	0

Address : 37H
Type : R
Name : TXCCH
Function : Transmit valid cell counter[19:16]

7	6	5	4	3	2	1	0
rsvd	rsvd	rsvd	rsvd	TXCC[19:16]			
–	–	–	–	0	0	0	0

This register indicates transmit valid cell count. When TXCC bit of CCUPD register is set to one, this counter is updated within 1μs. The value of this register is kept until next update request by setting TXCC bit to one. The transmit valid cell count stops when 4 MSB bits reach '1111'.

Address : 3FH
Type : R/W
Name : CCUPD
Function : Cell counter update flag

7	6	5	4	3	2	1	0
rsvd	rsvd	rsvd	rsvd	rsvd	rsvd	TXCC	RXCC
–	–	–	–	–	–	0	0

RXCC

Update control of RXCCL/M/H registers

0: No operation

1: Internal received valid cell count is loaded into RXCCL/M/H registers within 1 μs and RXCC bit is cleared automatically.

TXCC

Update control of TXCCL/M/H registers

0: No operation

1: Internal transmit valid cell count is loaded into TXCCL/M/H registers within 1 μs and TXCC bit is cleared automatically.

Address : 40H
Type : R/W
Name : MEMAL
Function : Memory address register [7:0]

7	6	5	4	3	2	1	0
MEMAL[7:0]							
0	0	0	0	0	0	0	0

Address : 41H
Type : R/W
Name : MEMAH
Function : Memory address register [3:0]

7	6	5	4	3	2	1	0
MEMWR	rsvd	rsvd	MEMAH[4:0]				
0	–	–	0	0	0	0	0

Address : 42H
Type : R/W
Name : MEMD
Function : Data control register

7	6	5	4	3	2	1	0
MEMD[7:0]							
0	0	0	0	0	0	0	0

These registers is used to access the PLC2 internal memory. For access, follow the steps below.

Read Operation

(1) Set address to MEMAH register.
(2) Set address to MEMAL register.
(3) Wait for TBD nsec.
(4) Read MEMD register.
For read access to consecutive addresses, follow steps (2) to (4).

Write Operation

(1) Set address to MEMAH register with MEMWR set high.
(2) Set address to MEMAL.
(3) Write the value to MEMD register.
For write access to consecutive addresses, follow steps (2) to (3).

Address mapping is as follows.

0x0000-0x07ff	RX firmware
0x0800-0x0bff	TX firmware
0x0c00-0x0cff	RX overhead memory
0x0d00-0x0dff	TX overhead memory
0x0e00-0x0eff	RX cell FIFO
0x0f00-0x0fff	TX cell FIFO
0x1000-0x10ff	RX internal registers
0x1100-0x11ff	TX internal registers

Field assignment in RX/TX overhead memory is shown below. Address is increased from upper left corner to rightward and then downward. For instance, the address of G1 byte in RX overhead memory is 0x0c39.

The SOH/POH bytes are extracted from received data and stored in RX overhead memory every frame. Other area in RX overhead memory is used as working storage by internal processor.

In TX overhead memory, A1, A2, B1, B3, C1, H1, H2, H3, B2, K2, H4, Z2, J1, B3, C2, G1 and H4 bytes are automatically updated by internal processor while other bytes are filled with zero automatically.

A1	A1	A1	A2	A2	A2	C1	C1	C1	J1						
B1	-	-	E1	-	-	F1	-	-	B3						
D1	-	-	D2	-	-	D3	-	-	C2						
H1	H1	H1	H2	H2	H2	H3	H3	H3	G1						
B2	B2	B2	K1	-	-	K2	-	-	F2						
D4	-	-	D5	-	-	D6	-	-	H4						
D7	-	-	D8	-	-	D9	-	-	Z3						
D10	-	-	D11	-	-	D12	-	-	Z4						
Z1	Z1	Z1	Z2	Z2	Z2	E2	-	-	Z5						

Field assignment of RX/TX overhead memory

Address : 50H
Type : R/W
Name : TSMOD1
Function : Test mode register 1

7	6	5	4	3	2	1	0
RFHLT	DATE	CLKE	LOOCE	TXCOE	NOTP	NORP	REG
0	0	0	0	0	0	0	0

This register is used for diagnostic or LSI internal testing purpose. Usually this register should be set to zero.

REG

Register operation mode
0: Write to read only register is not allowed.
1: Write to read only registers is allowed.

NORP

Receive processor operation mode
0: Normal operation
1: Stop receive processor

NOTP

Transmit processor operation mode
0: Normal operation
1: Stop transmit processor

TXCOE

The TXCOE bit controls PECL buffer of TXCOP/M.
0: Enables PECL output buffer of TXCOP/M
1: Disables PECL output buffer of TXCOP/M

LOOCE

The LOOCE bit controls PECL buffer of LOOCP/M.
0: Enables PECL input buffer of LOOCP/M
1: Disables PECL input buffer of LOOCP/M

CLKE

The CLKE bit controls PECL buffer of RXCIP/M and TXCIP/M.
0: Enables PECL input buffer of RXCIP/M and TXCIP/M
1: Disables PECL input buffer of RXCIP/M and TXCIP/M

DATE

The DATE bit controls PECL buffer of RXDIP/M and TXDOP/M.
0: Enables PECL input buffer of RXDIP/M and TXDOP/M.
1: Disables PECL input buffer of RXDIP/M and TXDOP/M.

RFHLT

The RFHLT controls receive cell FIFO. This bit is used for evaluation only.
0: Receive cell FIFO is in normal operation.
1: When RFHLT bit is set high, receive cell FIFO stops immediately.

Address : 51H
Type : R/W
Name : TSMOD2
Function : Test mode register 2

7	6	5	4	3	2	1	0
RCT	DWLD	VC	rsvd	OOLTST	TSTCK	CLKSEL	MONSEL
0	0	0	–	0	0	0	0

This register is used for diagnostic or LSI internal testing purpose. Usually this register should be set to zero.

MONSEL

MONSEL is used for production test only.

CLKSEL

The CLKSEL determines the output on RXCK pin..
0: The receive parallel clock is output from RXCK pin.
1: The transmit parallel clock is output from RXCK pin.

TSTCK

The TSTCK bit is used for evaluation only.
0: REFCK is divided and distributed to PLC2 digital part when LOOPU bit is set high.
1: REFCK is always directly distributed to PLC2 digital part when LOOPU bit is set high.

OOLTST

The OOLTST bit is used for evaluation only.
0: The out of lock detector is enabled only when RCKSEL is tied high.
1: The out of lock detector is enabled regardless of RCKSEL.

VC

C The VC bit controls frame format. This bit can be ignored in normal operation.
0: VC4 is assumed in STS-3c/STM-1 frame.
1: VC3 is assumed in STS-3c/STM-1 frame.

DWLD

The DWLD bit is used for evaluation only.
0: Normal operation
1: The download mode is activated.

RCT

The RCT bit is used for evaluation only.
0: The cell delineation is enabled when OOF is cleared.
1: The cell delineation is always enabled.

Address : 52H
Type : R/W
Name : TSGEN
Function : Test mode register 3

7	6	5	4	3	2	1	0
rsvd	rsvd	HECI	LOCI	BIPI	LOPI	OOFI	LOSI
–	–	0	0	0	0	0	0

This register is used for diagnostic or LSI internal testing purpose. Usually this register should be set to zero.

LOSI

Transmit frame option 1
0: Normal operation
1: Transmit all '00H' data

OOFI

Transmit frame option 2
0: Normal operation
1: A1/A2 bytes of transmit frame are set to '00H'

LOPI

Transmit frame option 3
0: Normal operation
1: H1/H2 pointer of transmit data is set to invalid value

BIPI

Transmit frame option 4
0: Normal operation
1: B1/B2/B3 bytes of transmit frame are bit-reversed.

LOCI

Transmit frame option 5
0: Normal operation
1: HEC byte of transmit cells are bit-reversed.

HECI

Transmit frame option 6
0: Normal operation
1: The LSB of HEC byte of transmit cells are bit-reversed.

Address : 53H
Type : R/W
Name : LFEBEI
Function : Test mode register 4

7	6	5	4	3	2	1	0
rsvd	rsvd	LFEBEE	LFEBEI[4:0]				
–	–	0	0	0	0	0	0

This register is used for diagnostic or LSI internal testing purpose. Usually this register should be set to zero.

LFEBEI[4:0]

Set this field with the value to send as LFEBE

LFEBEE

Transmit frame option 7

0: Normal operation

1: Transmit the value of LFEBEI[4:0] instead of calculated LFEBE

Address : 54H
Type : R/W
Name : PFEBEI
Function : Test mode register 5

7	6	5	4	3	2	1	0
rsvd	rsvd	rsvd	PFEBEE	PFEBEI[3:0]			
–	–	–	0	0	0	0	0

This register is used for diagnostic or LSI internal testing purpose. Usually this register should be set to zero.

PFEBEI[3:0]

Set this field with the value to send as PFEBE

PFEBEE

Transmit frame option 8

0: Normal operation

1: Transmit the value of PFEBEI[3:0] instead of calculated PFEBE

4. RECEIVE FUNCTIONS

4.1 Receive Clock

4.1.1 External Clock Mode

When RCKSEL pin is tied low, externally provided clock, RXCIP/M is and the clock recovery PLL is deactivated. **Usually RXDIP/M is sampled at the rising edge of RXCIP/M. Optionally RXDIP/M can be sampled at the falling edge of RXCIP/M by tying DLYSEL pin to high.**

4.1.2 On-chip Clock Recovery Mode

When RCKSEL pin is tied high, the receive side of PLC2 operates on internally recovered clock. The recovered clock is divided by 8 and compared with the reference clock REFCK. When the recovered clock frequency is out of ±244ppm range of REFCK, the clock recovery PLL is judged to be out of lock and RXOOL bit of STATUS1 register is set. The clock recovery PLL automatically switches to REFCK for reference source to keep oscillation in the vicinity of 155.52MHz (for STS-3/STM-1) , 51.84MHz (for STS-1) or 25.92MHz (for STS-1/2) when the recovered clock is out of ±244ppm range of REFCK or 80 bits period of no transition in receive data is detected or LOOCP/M input is tied high and AUTOCSE bit in CONT register is set high. During the period when the clock recovery PLL locks to REFCK, the data transition detector keeps sampling the receive data. When the data transition detector detects at least one data transition in 80 bits period and LOOCP/M input is tied low and the clock recovery PLL generates clock at frequency in ±244ppm range of REFCK , the clock recovery PLL switches back to receive data for reference. Above is typical case. There are many options available.

(1)80bit transition detector can be masked by setting zero to LOOCDE bit of CONT register (address: 00H).
(2)External LOOCP/M input can be masked by setting one to LOOCE bit of TSMOD1 register (address: 50H).
(3)Automatic switching between clock recovery mode in which RX PLL locks to receive data and reference mode in which RX PLL locks to REFCK can be cancelled by setting zero to AUTOCSE bit of CONT register (address:00H).
(4)244 ppm detector can be masked by setting zero to OOLDE bit of CONT register (address: 00H).
(5)When AUTOCSE bit is zero, RX PLL operation mode can be controlled by external pin REFSEL and PLLINI bit of CONT register. The operation is as follows.

REFSEL=1 or PLLINI=1 : RX PLL locks to REFCK.
Otherwise: RX PLL locks to receive data.

(6) Even when AUTOCSE is set to one, RX PLL can be forced into reference mode by making REFSEL=1 or PLLINI=1.
(Notice: STOP bit in PCONT register must be cleared to let AUTOCSE effective.)

4.2 Frame Synchronization

(1) STS-3c(STM-1)

HUNT

The framing pattern of 3 consecutive A1's followed by 3 consecutive A2's is searched. When the framing pattern is found, framing operation enters PRESYNC mode.

PRESYNC

When one more expected framing pattern is with 2430 byte interval, the framing operation enters SYNC mode.

SYNC

The framing pattern is checked every frame. If invalid framing patterns are found in 4 consecutive frames, OOF is set in STATUS1 register and the framing operation enters HUNT mode.

(2)STS-1, STS-1/2

HUNT

The framing pattern of one A1 followed by one A2 is searched. When the framing pattern is found, framing operation enters PRESYNC mode.

PRESYNC

When one more framing pattern is found with 810 byte interval, the framing operation enters SYNC mode.

SYNC

The framing pattern is checked every frame. If invalid framing patterns are found in 4 consecutive frames, OOF is set in STATUS1 register and the framing operation enters HUNT mode.

4.3 Frame Descrambling

The received frame data is descrambled by quasi random pattern generated by the polynomial $1+ x^6+x^7$. The first line of SOH (i.e. A1, A2, C1 bytes) is excluded from the descramble operation. The descramble operation starts from the byte following the last C1 byte with initial data for the generating polynomial '1111111.' The descramble operation can optionally be disabled by setting 1 to NODSBF bit in FRMSEL register.

4.4 BIP/FEBE Count

(1) Section BIP-8

Section BIP-8 is calculated over the entire area of each received frame before descrambling based on 8 bits interleaved parity calculation using even parity. The calculated BIP-8 code is compared with the B1 byte of the following frame bit by bit. The differences indicates the section level bit errors. The bit errors are counted and accumulated in a internal counter frame by frame. This counter value can be accessed via B1ERRL/H register. The host CPU is required to read them every one second for performance monitoring. Before reading them, host CPU should set 1 to B1 bit in FCUPD register. In about one frame time, B1ERRL/H are updated and B1 bit in FCUPD register is automatically cleared. Section BIP-8 counter stops counting when 4 MSB bits become '1111'.

(2) Line BIP-24

Line BIP-24 is calculated over the entire area of each frame after descrambling except for the first to third rows of SOH based on 24 bits interleaved parity calculation using even parity. The calculated BIP-24 code is compared with the three B2 bytes of the following frame bit by bit. The differences indicates the line level bit errors. The bit errors are counted and the count is inserted to the Z2 byte of the transmit SOH as Line FEBE, as well as accumulated in a internal counter frame by frame. This counter value can be accessed via B2ERRL/M/H register. The host CPU is required to read them every one second for performance monitoring. Before reading them, host CPU should set 1 to B2 bit in FCUPD register. In about one frame time, B2ERRL/M/H are updated and B2 bit in FCUPD register is automatically cleared. Line BIP-24 counter stops counting when 4 MSB bits become '1111'.

(3) Path BIP-8

Path BIP-8 is calculated over the entire area of each VC4 (or SPE for STS-1) after descrambling based on 8 bits interleaved parity calculation using even parity. The calculated BIP-8 code is compared with the B3 byte of the following frame bit by bit. The differences indicates the path level bit errors. The bit errors are counted and inserted to the G1 byte of the transmit POH as Path FEBE, as well as accumulated in a internal counter frame by frame. This counter value can be accessed via B3ERRL/H register. The host CPU is required to read them every one second for performance monitoring. Before reading them, host CPU should set 1 to B3 bit in FCUPD register. In about one frame time, B3ERRL/H are updated and B3 bit in FCUPD register is automatically cleared. Path BIP-8 counter stops counting when 4 MSB bits become '1111'.

(4) Line FEBE

Line FEBE value of every received frame is accumulated in Line FEBE counter. This counter value can be accessed via LFEBEL/M/H registers. The host CPU is required to read them every one second for performance monitoring. Before reading them, host CPU should set 1 to LFEBE bit in FCUPD register. In about one frame time, LFEBEL/M/H are updated and FEBE bit in FCUPD register is automatically cleared. Line FEBE counter stops counting when 4 MSB bits become '1111'.

(5) Path FEBE

Path FEBE value of every received frame is accumulated in Path FEBE counter. This counter value can be accessed via PFEBEL/H registers. The host CPU is required to read them every one second for performance monitoring. Before reading them, host CPU should set 1 to PFEBE bit in FCUPD register. In about one frame time, PFEBEL/H are updated and FEBE bit in FCUPD register is automatically cleared. Path FEBE counter stops counting when 4 MSB bits become '1111'.

4.5 Pointer Operation

The first H1 and the first H2 in SOH are used to locate J1 byte of VC4 (or SPE for STS-1). The second and third H1 bytes have fixed value of 93H. The second and third H2 bytes have fixed value of FFH. The second and third H1/H2 bytes are not used for pointer operation. Figure 4.1 shows the field assignment of the first H1/H2 bytes.

H1								H2							
NDF				FIXED		POINTER									
N	N	N	N	s	s	I	D	I	D	I	D	I	D	I	D

Figure 4.1 Field Assignment of H1/H2 Bytes.

NDF has two values; NNNN=0110 indicates no change in the pointer value while NNNN=1001 indicates change in pointer value.

FIXED field is usually ignored. The normal value depends on whether the receive data is SONET type or SDH type. When the receive data is SONET type, ss=00. When the receive data is SDH type, ss=10. When H1 and H2 bytes should carry PAIS, ss=11.

POINTER usually locates J1 byte. The pointer value is a binary number with a range from 0 to 782, which indicates the offset between the third H3 and the J1 byte of VC4. SOH bytes are not counted in the offset. For example, a pointer value of 0 indicates the J1 byte immediately follows the third H3 byte, whereas an offset of 522 indicates that the J1 byte immediately follows the third C1 byte. POINTER field is also used to indicate stuff operation. If the POINTER value of the current frame equals the POINTER value of the previous frame with 3 or more I bits inverted, it is the positive stuff indication. If the POINTER value of the current frame equals the POINTER value of the previous frame with 3 or more D bits inverted, it is the negative stuff indication.

There are 6 cases for the pointer operation.

(1) New Data Flag Active

Normally NDF has value of 0110. If NDF=1001 or 0001 or 1101 or 1011 or 1000, New Data Flag indication is considered active. The coincident POINTER value replaces the previous pointer value as far as the POINTER value is normal, that is in the range from 0 to 782. The updated pointer value takes effect from the first J1 byte

following H1, H2. When New Data Flag is considered active, the positive stuff indication and the negative stuff indication are ignored.

(2) Positive Stuff Operation

When following conditions are met, positive stuff operation is executed.

1) three or more I bits are inverted.
2) 2 or less D bits, if at all, are inverted.
3) New Data Flag indication is not active.
4) The pointer is not updated in preceding three frames.

In positive stuff operation, three bytes (one byte in STS-1) following the third H3 byte is ignored as payload only in the current frame . The pointer value is incremented by one.

(3) Negative Stuff Operation

When following conditions are met, negative stuff operation is executed.

1) three or more D bits are inverted.
2) 2 or less I bits, if at all, are inverted.
3) New Data Flag indication is not active.
4) The pointer is not updated in preceding three frames.

In negative stuff operation, three H3 bytes (one H3 byte for STS-1) are included as part of VC4 (or SPE in STS-1) only in the current frame. The pointer value is reduced by one.

(4) 3 Consecutive, Consistent New Value

When consistent, normal (in the range of 0 to 782) new pointer value is received for three consecutive frames, the pointer value replaces the previous value.

(5) Detection of Path AIS

If all ones pattern is detected in H1 and H2 for three consecutive frames, PAIS bit is set in STATUS1 register. PAIS bit is reset when valid pointers are detected for three consecutive frames. In SDH mode, PAIS is also reset when LOP is detected.

(6) LOP Detection

The LOP bit in STATUS1 register is set when a valid pointer is not found for 8 consecutive frames or when 8 consecutive NDF with the value of 1001 are detected. The LOP bit is reset when a valid pointer with normal NDF is detected for three consecutive frames or all ones pattern (that is PAIS) is detected in H1 and H2 for three consecutive frames.

4.6 Detection of Irregular State

(1) LOS : Loss of Signal

The receive data is sampled by REFCK clock and compared with the data sampled one cycle before. The LOS is declared and LOS bit in STATUS1 register is set when one of following two conditions is met for 20 μsec:

1. No data transition is observed at RXDIP/M input.
2. EXTLOS bit in LOSCT register is set high and LOOCP/M input is logical high.

LOS bit is cleared when two consecutive valid frame alignment patterns (A1, A2) have been received without no LOS set condition (20 μsec of no data transition or LOOCP/M input high) in between.

(2) OOF : Out of Frame

Framing operation set OOF bit in STATUS1 register when four consecutive invalid frame alignment patterns (A1, A2) have been received and reset OOF bit when two consecutive valid frame alignment pattern have been detected.

(3) LOF : Loss of Frame

The receive processor checks OOF status every frame. When OOF is set for 24 consecutive frames (i.e. for 3 msec), LOF bit in STATUS1 register is set. If OOF is found reset for 24 consecutive frames, the LOF bit is cleared.

(4) LOP : Loss of Pointer

The LOP bit in STATUS1 register is set when a valid pointer is not found for 8 consecutive frames or when 8 consecutive NDF with the value of 1001 are detected. The LOP bit is reset when a valid pointer with normal NDF is detected for three consecutive frames or all ones pattern (that is PAIS) is detected in H1 and H2 for three consecutive frames.

(5) LOC : Loss of Cell Delineation

The LOC bit in STATUS1 register is set when the cell delineation is in HUNT STATE. The LOC bit is reset when the cell delineation enters SYNC STATE. For the cell delineation, refer to Section 4.8.

4.7 Detection of Alarm Signals

The receive processor checks the K2 and G1 bytes to detect Line AIS, Line RDI, Path RDI along with H1/H2 bytes to detect Path AIS. When one of these alarms are detected, a corresponding bit in STATUS2 register is set. The alarm detection criteria is different for SONET and SDH. For SDH mode operation, SDH bit of FRMS register (address:01H) should be set to one.

(1) LAIS : Line Alarm Indication Signal

When a 111 binary pattern is detected in bits 6,7,8 of K2 byte for five consecutive frames (SONET mode) or three consecutive frames (SDH mode), LAIS is declared and LAIS bit of STATUS2 register is set high. LAIS is removed when any pattern other than 111 is detected in bits 6,7,8 of K2 bytes for five consecutive frames (SONET mode) or three consecutive frames (SDH mode).

(2) LRDI : Line Remote Defect Indication

When a 110 binary pattern is detected in bits 6,7,8 of K2 byte for five consecutive frames (SONET mode) or three consecutive frames (SDH mode), LRDI is declared and LRDI bit of STATUS2 register is set high. LRDI is removed when any pattern other than 110 is detected in bits 6,7,8 of K2 bytes for five consecutive frames (SONET mode) or three consecutive frames (SDH mode).

(3) PAIS : Path Alarm Indication Signal

When all 1 binary pattern is detected in H1/H2 bytes for three consecutive frames, PAIS is declared and PAIS bit of STATUS2 register is set high. PAIS is removed when a valid pointer with NDF set to '1001' is detected or when the same valid pointer with normal NDF is detected in three consecutive frames. In SDH mode, PAIS is also removed when LOP is detected.

(4) PRDI : Path Remote Defect Indication

When bit 5 of G1 byte is detected to be 1 for ten consecutive frames (SONET mode) or three consecutive frames (SDH mode), PRDI is declared and PRDI bit of STATUS2 register is set high. PRDI is removed when bit 5 of G1 byte is detected to be 0 for ten consecutive frames (SONET mode) or three consecutive frames (SDH mode).

4.8 Cell Processing

The payload is extracted from STS-3c(STM-1)/STS-1 frame in framing operation and provided to the cell delineation operation.

(1) Cell Delineation

HUNT

The cell delineation operation searches the cell header with correct HEC. When a correct HEC is found, the cell delineation operation enters PRESYNC state.

PRESYNC

With 53 byte interval, the cell header is checked for HEC. If correct HEC's are found for 6 cells, the cell delineation enters SYNC state. If an incorrect HEC is found before that, the cell delineation operation returns to HUNT state.

SYNC

The HEC pattern is check cell by cell. If 7 consecutive incorrect HEC's are found, the cell delineation returns to HUNT state. The SYNC state has two mode; CORRECTION mode and DETECTION mode. The cell delineation enters CORRECTION mode from PRESYNC state at first. When one bit HEC error is found in CORRECTION mode, it is corrected and the cell delineation enters DETECTION mode. If multiple bit HEC error is found in CORRECTION mode, the cell is dropped and the operation enters DETECTION mode. When a correct HEC is found in

DETECTION mode, the operation returns to CORRECTION mode.

(2) Cell Payload Descramble

The 48 byte cell payload is descrambled by the sequence generated by the polynomial ' $x^{43}+1$.' The descramble operation can optionally be disabled by setting 1 to NODSBC in CMS2 register.

(3) FIFO Control

Receive cell data is stored in the 4 cell deep receive FIFO. The receive FIFO is controlled on cell basis. When the FIFO is full of cell and there is more cells to be stored, these additional cells are discarded and RFOV bit in STATUS2 register is set high. The receive FIFO can be reset independently by setting RXFRES bit of PCONT register. In reset state, the receive FIFO discards cells stored in it and ignores writes. The RXFRES bit should be set for at least 10.8 μs.

(4) Receive Cell Interface

Receive cell interface operates according to UTOPIA level-2 defined in ATM forum. The single-PHY mode defined in UTOPIA level-2 is compatible with UTOPIA level-1.

In single PHY operation, data bus width is 8 bit. The maximum operation frequency is 33 MHz.

In multi PHY operation, data bus width can be 8 bit or 16 bit. Optional direct status indication is also supported. The maximum operation frequency is 40 MHz.

For parity bit, odd parity and even parity are selectable.

When 16 bit data bus operation is selected and HEC field is calculated in ATM layer, HEC can be inserted in UDF1 or UDF2. The parity selection and HEC selection are set in CMS1 register. Details of the receive cell interface operation is described in section 2.4.

(5) Performance Monitoring

The number of cells which have been passed with HEC error corrected are counted in 8 bit COHER counter while the number of cells which have been dropped due to HEC error are counted in 8 bit UCHER counter. COHER counter and UCHER counter stop counting when the count value reaches FFH. The number of normal or corrected cells which have been stored into receive cell FIFO is counted in 20 bit internal counter. The count value can be read via RXCCL/M/H register. The RXCCL/M/H are updated by setting 1 to RXCC bit in CCUPD register. The receive cell counter stops counting when 4 MSB bits reach ‘1111’.

(6) Optional Mode

When DROP bit in CMS2 register is set high, every cell with at least one HEC error is dropped in SYNC mode. No HEC correction is made.

When PASS bit in CMS2 register is set high, every cell is passed to the receive cell FIFO regardless of HEC error in SYNC mode.

When NORC bit in CMS2 register is set high, the coset polynomial $X^6+X^4+X^2+1$, is not added(modulo 2) in HEC calculation of received cell

In these optional mode, cell delineation state transition is made as normal mode.

(7) GFC Handling

GFC field is checked every cell. When PLC2 finds any command (1xxx, x1xx or xx1x) in GFC field of received cell, it sets GFC bit of STATUS2 register. When the command is HALT(1xxx) and GFCEN bit is set in CMS2 register, transmit of cells is stopped. GFC field of received cell is stored in RGFC register.

5. TRANSMIT FUNCTIONS

5.1 Transmit Clock Generation

(1) Loop Timing Mode

PLC2 transmit side operates in loop timing mode when LOOPT bit of LOOP register is set high. In the loop timing mode, transmit clock is the same as the receive side clock. Even when the clock recovery PLL fails to lock with the receive data, the transmit clock frequency is kept because in such situation, the clock recovery PLL switches the reference source to externally provided REFCK when AUTOCSE bit in CONT register is set high.

(2) Internal Clock Generation Mode

PLC2 generates transmit serial clock (155.52MHz/51.84MHz/25.92MHz) from REFCK when LOOPT bit of LOOP register is set low and TCKSEL pin is tied high.

(3) External Clock Mode

PLC2 transmit part operates on externally provided serial clock, TXCIP/M when LOOPT bit of LOOP register is set low and TCKSEL pin is tied low.

5.2 Frame Scrambling

The transmit data is scrambled by quasi random pattern generated by polynomial $1+x^6+x^7$. The first line of SOH (A1, A2, C1) is excluded from the scramble operation. The scramble operation start from the byte data following C1 with initial data for the polynomial '1111111.' This scramble operation can optionally be disabled by setting 1 to NODSBF bit in FRMS register.

5.3 BIP Calculation

(1) Section BIP-8

The section BIP-8 is calculated over the entire area of each frame after scramble based on 8 bits interleaved parity calculation using even parity. The calculated BIP-8 code is inserted to B1 byte in the following frame before scrambling.

(2) Line BIP-24

The line BIP-24 is calculated over the entire area of each frame before scrambling except for the first to third rows of SOH based on 24 bits interleaved parity calculation using even parity. The calculated BIP-24 code is inserted into B2 bytes in the following frame before scrambling.

(3) Path BIP-8

The path BIP-8 is calculated over the entire area of each VC4 (or SPE for STS-1)

before scrambling based on 8 bits interleaved parity calculation using even parity. The calculated BIP-8 code is inserted into B3 byte in the following frame before scrambling.

5.4 SOH Bytes Insertion

(1) A1, A2

The value should be F6H for A1's and 28H for A2's. These values are automatically inserted to transmit SOH in PLC2.

(2) C1

The value should be 01H/02H/03H for SONET and 01H/AAH/AAH for SDH. These values are automatically inserted to transmit SOH in PLC2.

(3) B1

The section BIP-8 is calculated automatically and inserted to the B1 byte in the transmit SOH.

(4) H1, H2

The H1 and H2 bytes are automatically set to value shown in Fig. 5.1 by internal processor. The pointer value is 0. The value of SS is 00 for SONET and 10 for SDH. For SDH mode operation, SDH bit of FRMS register (address:01H) should be set to 1. For diagnostic purpose, H1 and H2 bytes in transmit frame can be written from outside. In this case internal transmit processor should be stopped by setting 1 in NOTP bit of TSMOD1 register. The pointer value in H1 and H2 bytes must be consistent with the value set to the J1POSH/J1POSV registers. Table 5.1 shows some examples.

POINTER	J1V	J1H
0	3	3
86	3	89
521	8	89
522	0	3
782	2	89

Table 5.1 Correspondence Between POINTER and J1V/J1H

H1			H1	H1	H2	H2	H2
0110	SS		93H	93H	POINTER[7:0]	FFH	FFH
		↑ POINTER[9:8]					

POINTER[9:0]=0H by default.
SS=00 for SONET and 10 for SDH.

Figure 5.1 Values for Three H1's and Three H2's in Transmit SOH.

(5) H3

The H3 bytes are set automatically in transmit SOH. The value is usually 00H and, when PLC2 generates PAIS, FFH.

(6) B2

The line BIP-24 is calculated automatically and inserted to the B2 bytes of transmit SOH.

(7) K2

The Line AIS and Line RDI are set into the K2 byte automatically in PLC2 according to the condition tabulated in Section 1.4.

(8) Z2

The Line FEBE is calculated automatically and inserted to the Z2 byte.

(9) Others

The other SOH bytes are automatically filled with zero.

5.5 POH Bytes Insertion

(1) B3

The Path BIP-8 is calculated automatically and inserted into the B3 byte.

(2) C2

The value should be 13H because payload type is always ATM for PLC2. This value is automatically inserted to transmit POH in PLC2.

(3) G1

The Path RDI are inserted automatically to the G1 byte according to the condition tabulated in Section 1.4. The Path FEBE is calculated and inserted to the G1 byte, too.

(4) H4

The cell offset is counted automatically and set into the H4 byte.

(5) Others

The other POH bytes are automatically filled with zero.

5.6 Alarm Signal Insertion

(1) LAIS: Line Alarm Indication Signal

When LOS or LOF is detected in the receive side, Line AIS is automatically inserted by transmitting the code 111 in bit 6, 7, 8 of the K2 byte of transmitting frame

if LAIS bit is set in TXALM1 register. LAIS is inserted without any condition when LAIS bit is set high in TXALM2 register.

(2) LRDI: Line Remote Defect Indication

When LOS or LOF is detected or LAIS is declared in the receive side, Line RDI is automatically inserted by transmitting the code 110 in bit 6, 7, 8 of the K2 byte of transmitting frame if LRDI bit is set in TXALM1 register. LRDI is inserted without condition when LRDI bit is set high in TXALM2 register.

(3) PAIS: Path Alarm Indication Signal

When LOS, LOF, LOP, LOC is detected or LAIS is declared in the receive side, Path AIS is automatically inserted by setting all-ones in H1/H2/H3 bytes and the entire payload field if PAIS bit is set in TXALM1 register. PAIS is also inserted without condition when PAIS bit is set high in TXALM2 register.

(4) PRDI: Path Remote Defect Indication

When LOS, LOF, LOP, LOC is detected or LAIS or PAIS is declared in the receive side, Path RDI is automatically inserted by setting 1 in bit 5 of the G1 byte of transmitting frame if PRDI bit is set in TXALM1 register. PRDI is inserted without condition when PRDI bit is set high in TXALM2 register.

5.7 Transmit Cell Processing

(1) Transmit Cell Interface

Transmit cell interface operates according to UTOPIA level-2 defined in ATM forum. The single-PHY mode defined in UTOPIA level-2 is compatible with UTOPIA level-1.

In single PHY operation, data bus width is 8 bit. The maximum operation frequency is 33 MHz.

In multi PHY operation, data bus width can be 8 bit or 16 bit. Optional direct status indication is also supported. The maximum operation frequency is 40 MHz.

For parity bit, odd parity and even parity are selectable.

When 16 bit data bus operation is selected, HEC can be inserted in UDF1 or UDF2. The parity selection and HEC selection are set in CMS1 register. Details of the transmit cell interface operation is described in section 2.4.

(2) FIFO Control

Transmit cell data received from ATM layer is stored in the transmit FIFO. The transmit FIFO is controlled in cell level. The FIFO is programmable to be 1, 2, 3 or 4 cell deep. When the FIFO is full of cell data, PLC2 rejects receiving more cells from ATM layer by deasserting TXCAV when it is polled. The transmit FIFO can be reset independently by setting TXFRES bit of CONT register. In reset state, the transmit FIFO discards cells stored in it and ignores writes. The TXFRES bit should be set for at least 10.8 μsec.

(3) Cell Header Calculation

A CRC-8 calculation is performed over the first four header bytes. A parallel implementation of the polynomial, x^8+x^2+x+1 is used. The coset polynomial, $x^6+x^4+x^2+1$ is added by modulo 2 to the residue. The result is inserted to the fifth byte of the ATM cell. The coset polynomial addition can optionally be disabled by setting 1 to NOTC in CMS2 register. The cell header calculation can optionally disabled by setting 1 to NOHEC bit in CMS2 register. In this case, the 5th byte of the cell data goes through unchanged.

(4) Cell Payload Scrambling

The 48 bytes of cell payload is scrambled with the sequence generated by the polynomial ' $x^{43}+1$.' The scramble operation can optionally be disabled by setting high to NOSCBC in CMS2 register.

(5) Performance Monitoring

The number of assigned or unassigned cells which have been read from transmit cell FIFO and inserted in the transmit frames are counted in internal 20 bit counter. The count value can be read via TXCCL/M/H register. The TXCCL/M/H are updated by setting 1 to TXCC bit in CCUPD register. The transmit cell counter stops counting when 4 MSB bits become ‘1111’.

(6) GFC Handling

Transmit of cells is stopped when GFCHLT bit is set in GFC register and HALT bits are set in GFC field of received cells. When TGFCEN bit is set in CMS3 register, TGFC[3:0] in CMS3 register is inserted in the GFC field of assigned/unassigned cells transmitted from ATM layer. Additionally, When OPT bit in GFC register is set high, TGFC[3:0] in CMS3 register is also inserted in unassigned cells generated in PLC2.

(7) Idle/Unassigned Cell Insertion

When there is no cell in the transmit FIFO, PLC2 inserts idle/unassigned cell to transmit frame dependent on register control. If UAC bit is set high in CMS1 register, PLC2 inserts unassigned cells with GFC field set to ‘0001’ or TGFC[3:0] depending on OPT bit in CMS3 register. If UAC bit is set low, PLC2 inserts idle cells.

6. OPERATION AND TEST

6.1 Startup Procedure

For startup, follow the procedure below.

Step 1: Hardware Reset
-RESET pin should be tied low for 10 cycles of CLK to reset the configuration registers. These configuration registers have default values after reset.

Step 2: Software Reset
Set RESET bits of CONT registers to high for at least *20* cycles of REFCK to reset internal registers and then clear these RESET bits.

Step 3: Operation Mode Set
Set configuration registers according to the usage. If default values are sufficient, skip this step.

Step 4: Clear Stop
Clear stop bit of CONT register of each port to start normal operation.

Setting STOP bit high during normal operation is not recommended because it results in loss of frames and cells.

6.2 Loop Back

Loop back mode is controlled by LOOP register and TSDSEL pin.

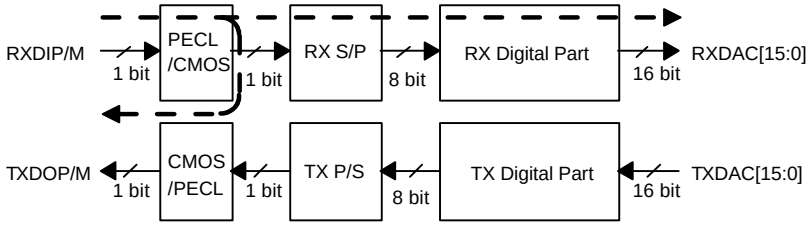
(1) Serial Line Loop Back
Setting one to LOOPL bit of LOOP register or tying TSDSEL pin to high forces PLC2 into serial line loop back mode. In this mode, receive serial data RXDIP/M is directly output from transmit serial port TXDOP/M and at the same time fed to receive part.

(2) Parallel Line Loop Back
Setting one to LOOP2 bit of LOOP register forces PLC2 into parallel line loop back mode. In this mode, receive serial data RXDIP/M is serial/parallel converted and fed to receive parallel part and at the same time parallel/serial converted in transmit section and output from transmit serial port TXDOP/M.

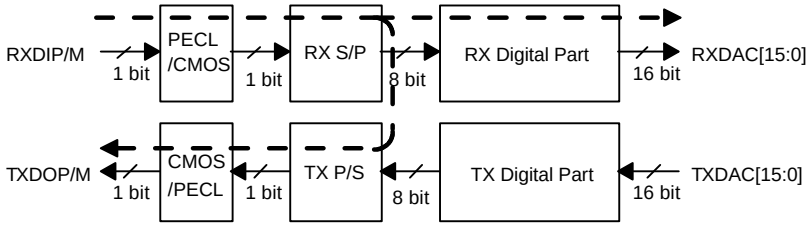
(3) Serial UTOPIA Loop Back
Setting one to LOOP1 bit of LOOP register forces PLC2 into serial UTOPIA loop back mode. In this mode, transmit serial data is looped back to receive serial input internally and at the same time output from transmit serial port TXDOP/M.

(4) Parallel UTOPIA Loop Back

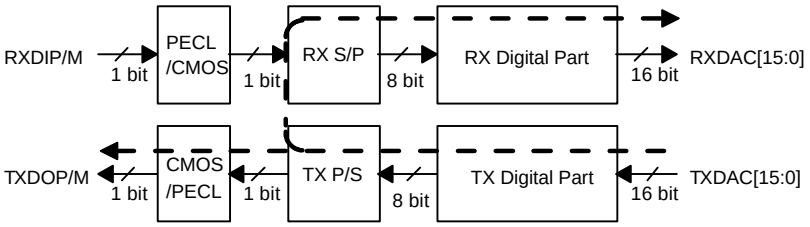
Setting one to LOOPU bit of LOOP register forces PLC2 into parallel UTOPIA loop back mode. In this mode, transmit parallel data is looped back to receive parallel part and at the same time parallel/serial converted and output from transmit serial port TXDOP/M.



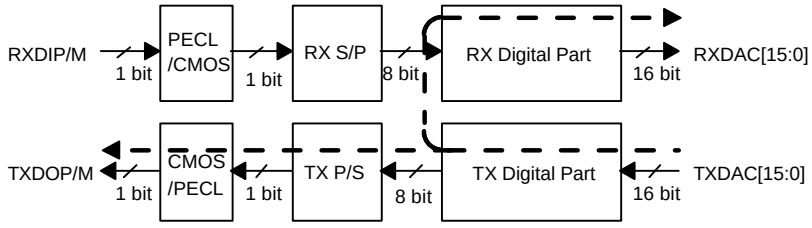
Serial Line Loop Back



Parallel Line Loop Back



Serial UTOPIA Loop Back



Parallel UTOPIA Loop Back

6.3 Diagnostic Test

Receive state detection capability can be tested in loop back mode using TSGEN register. LOS, OOF, LOP, BIP error, LOC detection test can be made setting corresponding bit in TSGEN register.

7. ABSOLUTE MAXIMUM RATINGS

Parameter	Ratings
Ambient Temperature Under Bias	0 °C to 70 °C
Storage Temperature	-65 °C to 150 °C
Supply Voltage	-0.5 V to 7.0 V
Input Voltage Applied	-0.5 V to VDD + 0.5 V
Soldering Temperature (10 sec)	240 °C

8. DC CHARACTERISTICS

(TA = 0 °C ~ 70 °C, VDD = 5 V +/- 5 %)

TTL level input and output

Symbol	Parameter	Min	Max	Units	Conditions
VOLtu	TTL UTOPIA I/F Output Low Voltage		0.4	Volts	IOL = +8 mA
VOHtu	TTL UTOPIA I/F Output High Voltage	2.4		Volts	IOH = -8 mA
VOLt	TTL Output Low Voltage		0.4	Volts	IOL = +4 mA
VOHt	TTL Output High Voltage	2.4		Volts	IOH = -4 mA
VILt	TTL Input Low Voltage		0.8	Volts	
VIHt	TTL Input High Voltage	2.0		Volts	
IILt	TTL Input Low Current		-10	μA	VIL = VSS
IIHt	TTL Input High Current		+10	μA	VIH = VDD

CMOS level input

Symbol	Parameter	Min	Max	Units	Conditions
VILc	CMOS Input Low Voltage		2.0	Volts	
VIHc	CMOS Input High Voltage	3.0		Volts	
IILc	CMOS Input Low Current		-10	μA	VIL = VSS
IIHc	CMOS Input High Current		+10	μA	VIH = VDD

PECL input and output

Symbol	Parameter	Min	Max	Units	Conditions
VOLp	PECL Output Low Voltage	VDD -1.9	VDD -1.5	Volts	Note 1
VOHp	PECL Output High Voltage	VDD -1.15	VDD -0.75	Volts	Note 1
VILp	PECL Input Low Voltage	VDD -1.9	VDD -1.5	Volts	Note 1
VIHp	PECL Input High Voltage	VDD -1.15	VDD -0.75	Volts	Note 1
IILp	PECL Input Low Current		-10	μA	VIL = VSS
IIHp	PECL Input High Current		+10	μA	VIH = VDD

Note 1: Ta = 25 °C, VDD = 5 V, terminated to 3.0 V via 50 Ω

Symbol	Parameter	Min	Max	Units	Conditions
IDDD	Operating Current		220	mA	Note 2
Cin	Input Capacitance		6	pF	
Cout	Output Capacitance		6	pF	
Cio	Bi-directional Capacitance		6	pF	

Note2: VDD = 5.25 V, Outputs loaded with 50 pF, TXDOP/M and RXDIP/M operating at 155.52 Mbit/s

9. TIMING CHARACTERISTICS

9.1 Line Interface

RX Line Interface

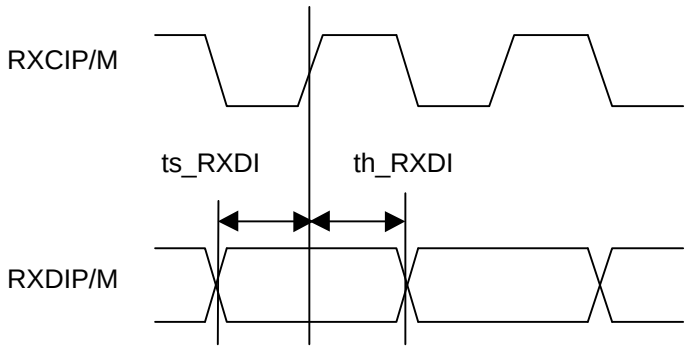


Figure 9.1.1 RX Line Interface Timing

Symbol	Description	Min	Max	Units
	RXCIP/M Duty Cycle	45	55	ns
	RXCIP/M Frequency Tolerance	-20	+20	ppm
ts_RXDI	RXDIP/M Setup Time to RXCIP/M High	2		ns
th_RXDI	RXDIP/M Hold Time to RXCIP/M High	2		ns

TX Line Interface

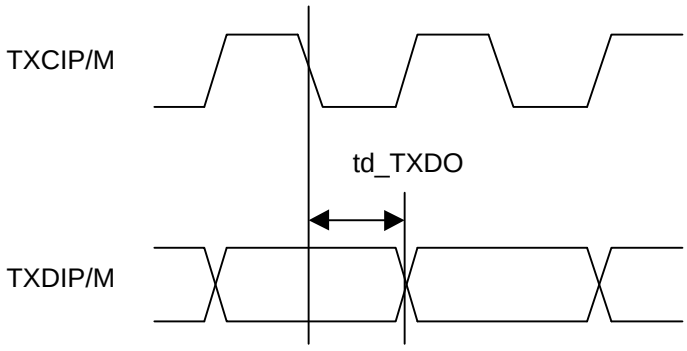


Figure 9.1.2 TX Line Interface Timing

Symbol	Description	Min	Max	Units
	TXCIP/M Duty Cycle	45	55	ns
	TXCIP/M Frequency Tolerance	-20	+20	ppm
ts_TXDOP	TXDOP/M Delay from TXCIP/M Low	-2	2	ns

9.2 Cell Interface

TX Cell Interface

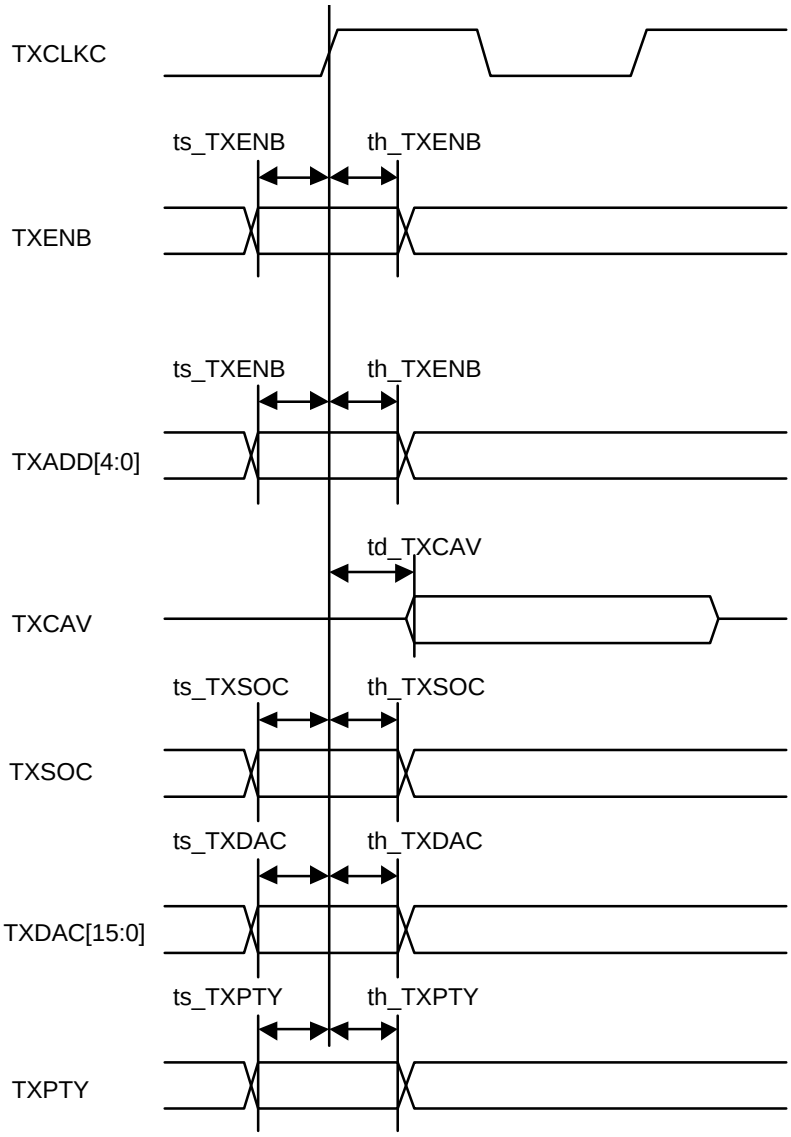


Fig. 9.2.1 TX Cell Interface Timing

Transmit UTOPIA Level-2 Single-PHY or Multi-PHY with 8 bits Data Bus

Symbol	Description	Min	Max	Units
	TXCLKC Frequency		33	MHz
	TXCLKC Duty Cycle	40	60	%
ts_TXENB	TXENB Setup Time to TXCLKC High	8		ns
th_TXENB	TXENB Hold Time to TXCLKC High	1		ns
ts_TXADD	TXADD[4:0] Setup Time to TXCLKC High	8		ns
th_TXADD	TXADD[4:0] Hold Time to TXCLKC High	1		ns
td_TXCAV	TXCAV Delay from TXCLKC High	1	22	ns
ts_TXSOC	TXSOC Setup Time to TXCLKC High	8		ns
th_TXSOC	TXSOC Hold Time to TXCLKC High	1		ns
ts_TXDAC	TXDAC[7:0] Setup Time to TXCLKC High	8		ns
th_TXDAC	TXDAC[7:0] Hold Time to TXCLKC High	1		ns
ts_TXPTY	TXPTY Setup Time to TXCLKC High	8		ns
th_TXPTY	TXPTY Hold Time to TXCLKC High	1		ns

Transmit UTOPIA Level-2 Multi-PHY with 16 bits Data Bus

Symbol	Description	Min	Max	Units
	TXCLKC Frequency		40	MHz
	TXCLKC Duty Cycle	40	60	%
ts_TXENB	TXENB Setup Time to TXCLKC High	6		ns
th_TXENB	TXENB Hold Time to TXCLKC High	1		ns
ts_TXADD	TXADD[4:0] Setup Time to TXCLKC High	6		ns
th_TXADD	TXADD[4:0] Hold Time to TXCLKC High	1		ns
td_TXCAV	TXCAV Delay from TXCLKC High	1	19	ns
ts_TXSOC	TXSOC Setup Time to TXCLKC High	4		ns
th_TXSOC	TXSOC Hold Time to TXCLKC High	1		ns
ts_TXDAC	TXDAC[15:0] Setup Time to TXCLKC High	4		ns
th_TXDAC	TXDAC[15:0] Hold Time to TXCLKC High	1		ns
ts_TXPTY	TXPTY Setup Time to TXCLKC High	4		ns
th_TXPTY	TXPTY Hold Time to TXCLKC High	1		ns

RX Cell Interface

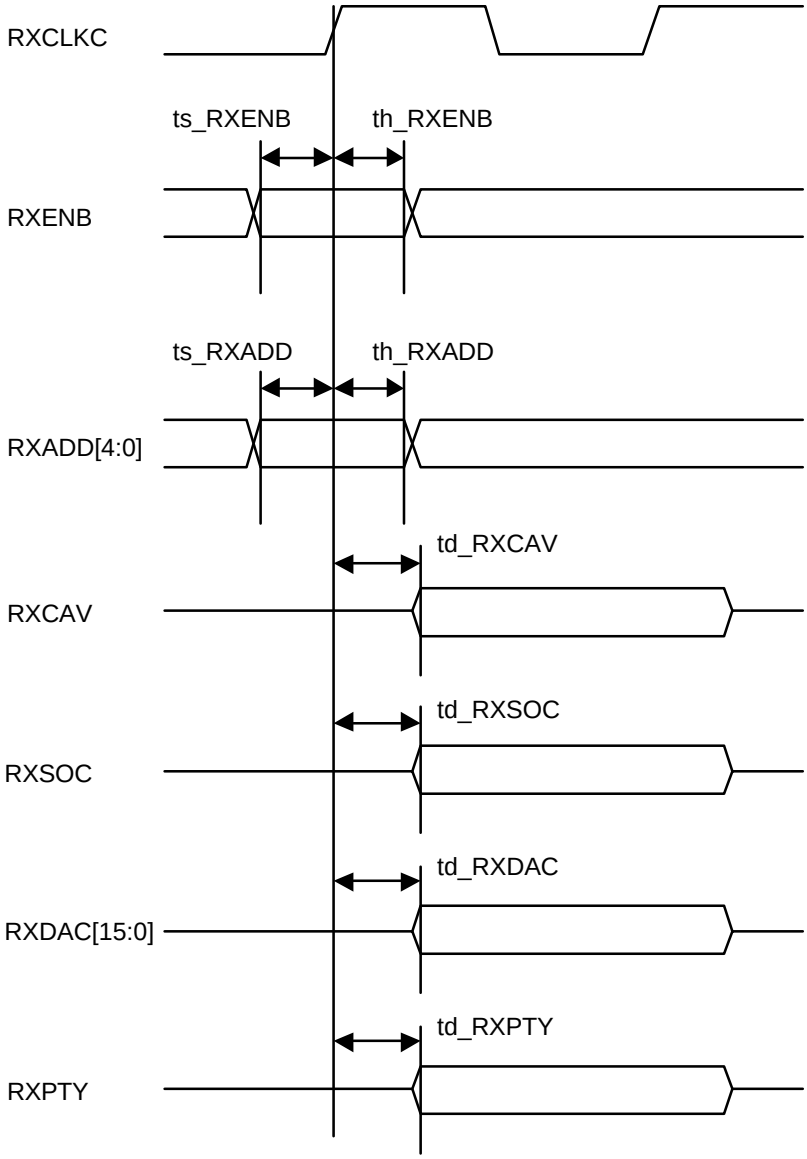


Fig. 9.2.2 RX Cell Interface Timing

Receive UTOPIA Level-2 Single-PHY or Multi-PHY with 8 bits Data Bus

Symbol	Description	Min	Max	Units
	RXCLKC Frequency		33	MHz
	RXCLKC Duty Cycle	40	60	%
ts_RXENB	RXENB Setup Time to RXCLKC High	8		ns
th_RXENB	RXENB Hold Time to RXCLKC High	1		ns
ts_RXADD	RXADD[4:0] Setup Time to RXCLKC High	8		ns
th_RXADD	RXADD[4:0] Hold Time to RXCLKC High	1		ns
td_RXCAV	RXCAV Delay from RXCLKC High	1	22	ns
td_RXSOC	RXSOC Delay from RXCLKC High	1	22	ns
td_RXDAC	RXDAC[7:0] Delay from RXCLKC High	1	22	ns
td_RXPTY	RXPTY Delay from RXCLKC High	1	22	ns

Receive UTOPIA Level-2 Multi-PHY with 16 bits Data Bus

Symbol	Description	Min	Max	Units
	RXCLKC Frequency		40	MHz
	RXCLKC Duty Cycle	40	60	%
ts_RXENB	RXENB Setup Time to RXCLKC High	6		ns
th_RXENB	RXENB Hold Time to RXCLKC High	1		ns
ts_RXADD	RXADD[4:0] Setup Time to RXCLKC High	6		ns
th_RXADD	RXADD[4:0] Hold Time to RXCLKC High	1		ns
td_RXCAV	RXCAV Delay from RXCLKC High	1	19	ns
td_RXSOC	RXSOC Delay from RXCLKC High	1	19	ns
td_RXDAC	RXDAC[15:0] Delay from RXCLKC High	1	19	ns
td_RXPTY	RXPTY Delay from RXCLKC High	1	19	ns

9.3 CPU Interface

CPU Interface Read Timing

[With Active ALE]

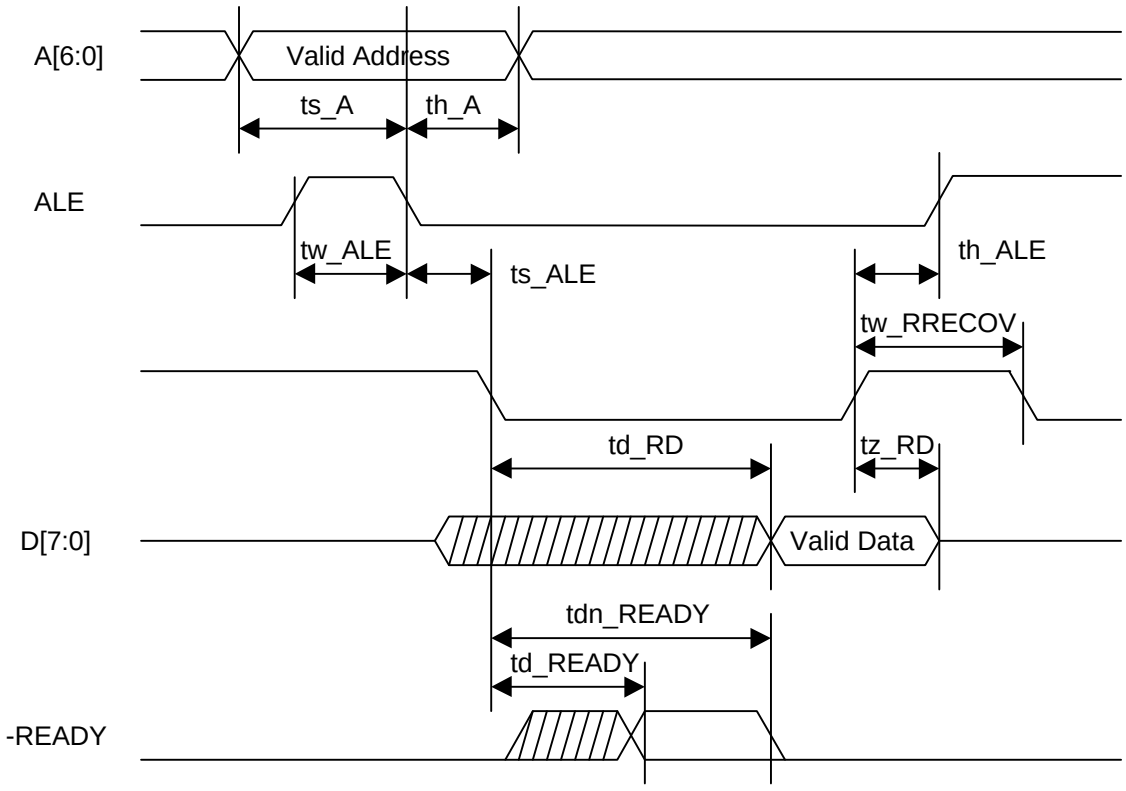


Figure 9.3.1 CPU Interface Read Access with Active ALE

Read access starts when (-RD + -CE) goes down and ends when (-RD + -CE) goes up.

Symbol	Description	Min	Max	Units
ts_A	Valid Address Setup Time to ALE	25		ns
th_A	Valid Address Hold Time from ALE	5		ns
tw_ALE	ALE High Pulse Width	20		ns
ts_ALE	ALE Low Setup Time to Read Start	0		ns
th_ALE	ALE Low Hold Time to Read End	(1)		ns
td_RD	Valid Data Delay from Read Start		(2)	ns
tz_RD	Data Output Hi-Z from Read End	1	20	ns
td_READY	READY Valid Delay from Read Start	TBD	TBD	ns
tdn_READY	READY Low Delay from Read Start		(3)	ns
tw_RRECOV	Read Recovery Time		(4)	ns

Table. 9.3.1 CPU Interface Read Timing with Active ALE

[With ALE Fixed to High]

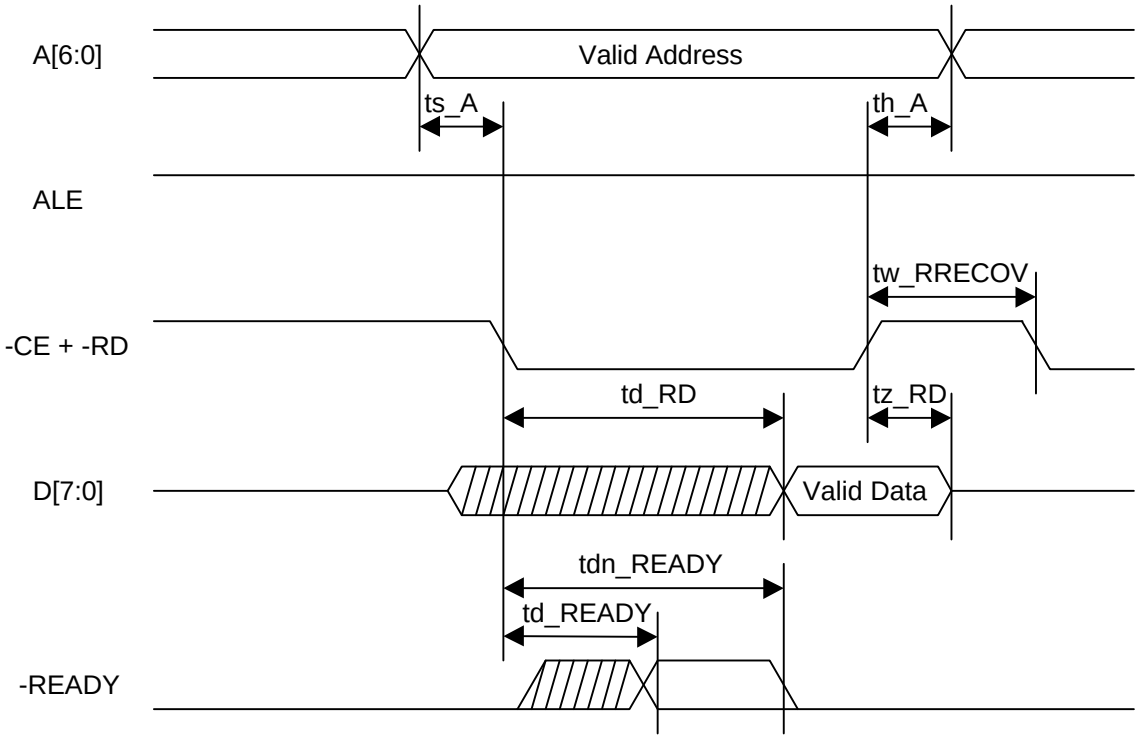


Figure 9.3.2 CPU Interface Read Access with Fixed ALE

Read access starts when (-RD + -CE) goes down and ends when (-RD + -CE) goes up.

Symbol	Description	Min	Max	Units
ts_A	Valid Address Setup Time to (-CE + -RD) low	25		ns
th_A	Valid Address Hold Time from (-CE + -RD) High	5		ns
td_RD	Valid Data Delay from Read Start		(2)	ns
tz_RD	Data Output Hi-Z from Read End	1	20	ns
td_READY	READY Valid Delay from Read Start	TBD	TBD	ns
tdn_READY	READY Low Delay from Read Start		(3)	ns
tw_RRECOV	Read Recovery Time		(4)	ns

Table. 9.3.2 CPU Interface Read Timing with ALE Fixed to High

In the formula below, Fmin is lower frequency of Byte clock and CLK (host interface clock). Byte clock is 19.44MHz for STS-3 (STM-1), 6.38MHz for STS-1 and 3.24MHz for STS-1/2. CLK is 19.44MHz.

(1) th_ALE(min) = (1 / Fmin) * 2 [ns]

(2)
For internal registers and internal memories except for TX/RX overhead memories:
td_RD (max) = (1 / Fmin) * 3 + 50 [ns]

For TX/RX overhead memories:
td_RD (max) = (1 / Fmin) * 3 + 50 [ns] when STOP bit in PCONT register is set.
td_RD (max) = (1 / Fmin) * 100 [ns] when STOP bit in PCONT register is not set.

(3)
For internal registers and internal memories except for TX/RX overhead memories:
td_READY (max) = (1 / Fmin) * 3 + 50 [ns]

For TX/RX overhead memories:
td_READY (max) = (1 / Fmin) * 3 + 50 [ns] when STOP bit in PCONT register is set.
td_READY (max) = (1 / Fmin) * 100 [ns] when STOP bit in PCONT register is not set.

In the formula above, Fmin is lower frequency of Byte clock and CLK (host interface clock). Byte clock is 19.44MHz for STS-3 (STM-1), 6.38MHz for STS-1 and 3.24MHz for STS-1/2. CLK is 19.44MHz.

(4) tw_RECOV(min) = (1 / Fmin) * 3 [ns]

CPU Interface Write Timing

[With Active ALE]

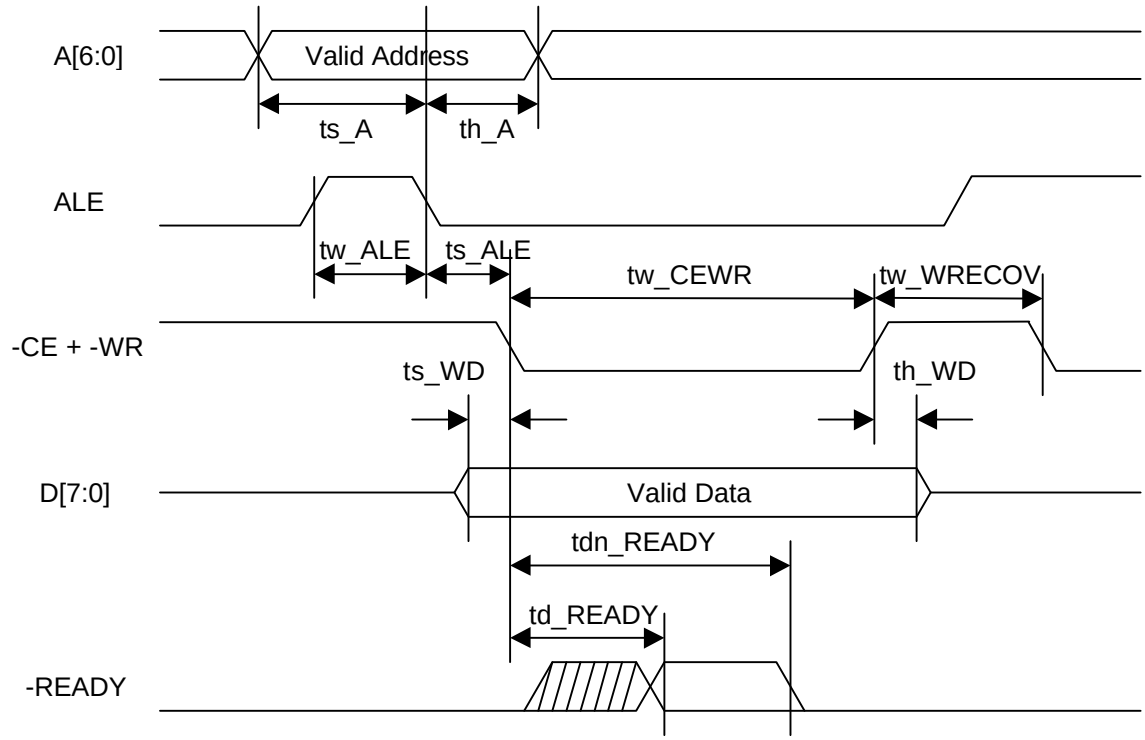


Figure 9.3.3 CPU Interface Write Access with Active ALE

Write access starts when (-WR + -CE) goes down and ends when (-WR + -CE) goes up.

Symbol	Description	Min	Max	Units
ts_A	Valid Address Setup Time to ALE	25	*	ns
th_A	Valid Address Hold Time to ALE	5	*	ns
tw_ALE	ALE High Pulse Width	20	*	ns
ts_ALE	ALE Low Setup Time to Write Start	0	*	ns
th_ALE	ALE Low Hold Time to Write End	(1)	*	ns
tw_CEWR	Write pulse width	(2)	*	ns
ts_WD	Write Data Setup Time to Write Start	0	*	ns
th_WD	Write Data Hold Time to Write End	0	*	ns
td_READY	READY Valid Delay from Write Start	TBD	TBD	ns
tdn_READY	READY Low Delay from Write Start	*	(3)	ns
tw_WRECOV	Write Recovery Time	*	(4)	ns

Table 9.3.3 CPU Interface Write Timing with Active ALE

[With ALE Fixed to High]

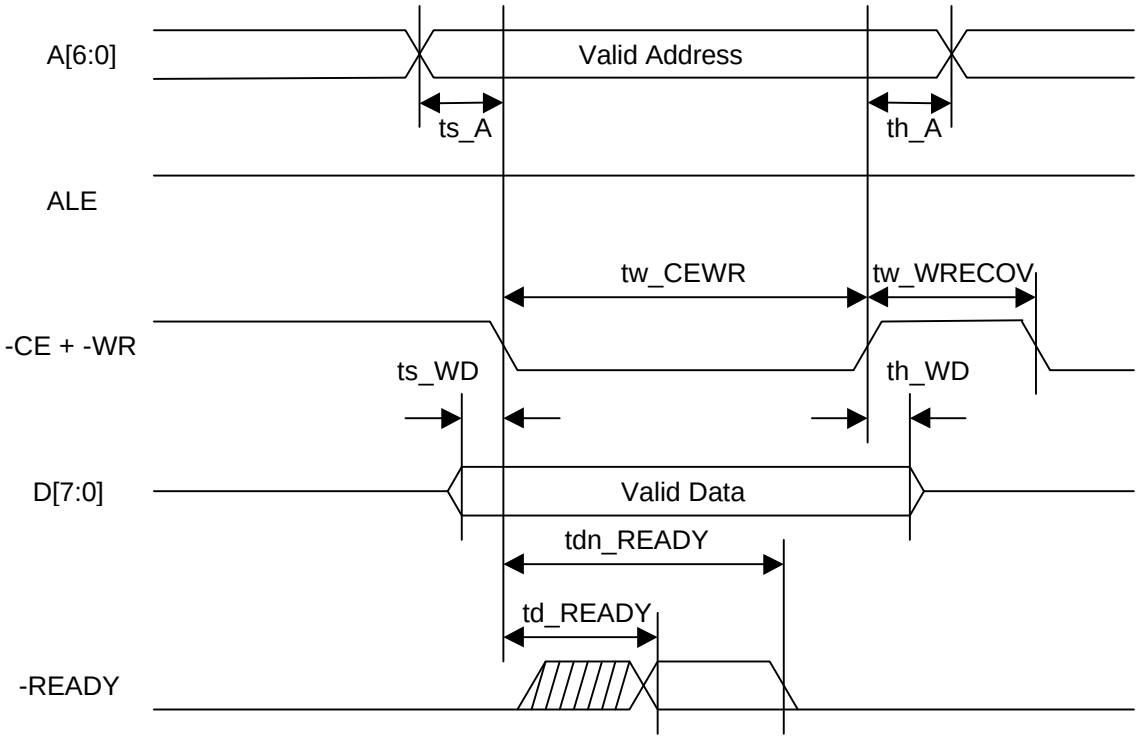


Figure 9.3.4 CPU Interface Write Access with Fixed ALE

Write access starts when (-WR + -CE) goes down and ends when (-WR + -CE) goes up.

Symbol	Description	Min	Max	Units
ts_A	Valid Address Setup Time to (-CE + -WR) low	25	*	ns
th_A	Valid Address Hold Time from (-CE + -WR) High	5	*	ns
tw_CEWR	Write pulse width	(2)	*	ns
ts_WD	Write Data Setup Time to Write Start	0	*	ns
th_WD	Write Data Hold Time to Write End	0	*	ns
td_READY	READY Valid Delay from Write Start	TBD	TBD	ns
tdn_READY	READY Low Delay from Write Start	*	(3)	ns
tw_WRECOV	Write Recovery Time	*	(4)	ns

Table 9.3.4 CPU Interface Write Timing with ALE Fixed to High

In the formula below, Fmin is lower frequency of Byte clock and CLK (host interface clock). Byte clock is 19.44MHz for STS-3 (STM-1), 6.38MHz for STS-1 and 3.24MHz for STS-1/2. CLK is 19.44MHz.

(1) th_ALE(min) = (1 / Fmin) * 2 [ns]

(2)
For internal registers and internal memories except for TX/RX overhead memories:
tw_CEWR (max) = (1 / Fmin) * 4 [ns]

For TX/RX overhead memories:
tw_CEWR (max) = (1 / Fmin) * 4 [ns] when STOP bit in PCONT register is set.
tw_CEWR (max) = (1 / Fmin) * 100 [ns] when STOP bit in PCONT register is not set.

(3)
For internal registers and internal memories except for TX/RX overhead memories:
td_READY (max) = (1 / Fmin) * 3 + 50 [ns]

For TX/RX overhead memories:
td_READY (max) = (1 / Fmin) * 3 + 50 [ns] when STOP bit in PCONT register is set.
td_READY (max) = (1 / Fmin) * 100 [ns] when STOP bit in PCONT register is not set.

(4) tw_RECOV(min) = (1 / Fmin) * 3 [ns]

A.1 PLC2 INTERNAL OPERATION

RX Clock Recovery Block

Recovers clock from NRZ signal of 155.52Mbps or 51.84Mbps. The clock recovery PLL switches to the reference clock REFCK when at least one of three conditions below are satisfied:
(1) LOOC is asserted
(2) 80 bit period of no signal transition is detected
(3) PLL frequency deviated more than 244ppm from the reference clock
The clock recovery PLL switches to the incoming data again when three conditions below are all satisfied:
(1) LOOC is not asserted.
(2) signal transition is detected in 80 bit period
(3) PLL frequency is within 244 ppm range of the reference clock

RX Serial to Parallel Converter

Received signal data is converted to 8 bits parallel form in this block. The operation clock can be selectable between internally recovered clock or externally provided clock.

Receive Frame Handler

(1) The frame structure is recognized and synchronization is done. When the frame synchronization is in hunt mode, OOF is declared. When OOF continues more than 3msec, LOF is declared.
(2) The point tracking is done in this block. When the pointer value in H1/H2 bytes are invalid, LOP (Loss of Pointer) is declared.
(3) The entire SOH/POH area of each incoming frame is stored in the Receive Overhead Memory. The payload area is transferred to the Receive Cell Handler.
(4) Section BIP-8, Line BIP-24 and Path BIP-8 are calculated for each incoming frame.

Receive Overhead Memory

The 256 bytes receive overhead memory stores SOH/POH of each incoming frame for processing by the receive processor. It is used as working area for the receive processor.

Receive Processor

The receive processor accesses the Receive Overhead Memory for SOH/POH handling. For each frame, the receive processor:
(1) Checks the K2 byte to declare Line AIS and Line RDI.
(2) Checks the H1/H2 byte to declare Path AIS.
(3) Checks the G1 byte to declare Path RDI.
(4) Checks the B1 byte to count Section BIP-8 errors and accumulates the error count.
(5) Checks the B2 byte to count Line BIP-24 errors and accumulates the error count.
(6) Checks the B3 byte to count Path BIP-8 errors and accumulates the error count.

(7) Checks the Z2 byte to accumulate Line FEBE count.
(8) Checks the G1 byte to accumulate Path FEBE count.

Receive Program Memory

The receive program memory stores up to 1024 steps of instruction codes for the receive processor.

Receive Cell Handler

The receive cell handler makes cell delineation. It checks the header of incoming cells. When a cell with 1bit header error is found while in sync correction mode, the receive cell handler corrects the error and send it to the receive cell FIFO. When a cell with 1 bit error is found in sync detection mode or when a cell with multiple bit error is found while in sync correction mode, the receive cell handler discards the cell. Cells with corrected header, cells which are discarded and cells which are normal or corrected and stored in the receive cell FIFO are counted respectively. In the hunt mode, the receive cell handler declares LOC (Loss of Cell delineation).

Receive Cell FIFO

The receive cell FIFO can store up to 4 cells. The FIFO depth is fixed to be 4 cell deep. When an entire cell is stored, the full flag is set and the receive cell interface begins to read the cell data and send it to ATM layer. The write port of the FIFO operates on the receive network clock while the read port operates on the cell interface clock provided from the ATM layer.

Receive Cell Interface

The receive cell interface reads cell data from the receive cell FIFO and send it to the ATM layer. The cell transfer begins when the entire cell data has been stored in the receive cell FIFO. UTOPIA Level1 and Level2 are both supported. The data bus width is selectable between 8 bits and 16 bits.

Transmit Clock Synthesis

The transmit clock synthesis PLL generates 155.52MHz/51.84MHz from reference clock of 19.44MHz/6.48MHz. If it fails to get within 244ppm range of the reference clock, TXOOL is declared.

TX Parallel to Serial Converter

The TX parallel to serial converter converts the transmit parallel data to serial one. The operation clock can be selectable between internally generated clock and externally provided clock.

Transmit Frame Handler

(1) B1, B2 and B3 value for the transmit frame are calculated.
(2) The transmit frame is assembled with SOH/POH read from the transmit overhead memory and payload received from the transmit cell handler.

Transmit Overhead Memory

The 256 byte transmit overhead memory stores SOH/POH to transmit. It is used as working area for the transmit processor.

Transmit Processor

For each transmit frame, the transmit processor:
(1) Checks STATUS1, STATUS2 and if conditions are satisfied, inserts Line AIS, Line RDI, Path AIS, Path RDI to SOH/POH in the transmit overhead memory.
(2) Copies B1, B2 and B3 value from the corresponding registers of the transmit frame handler to B1, B2 and B3 bytes of SOH/POH in the transmit overhead memory.
(3) Copies Line FEBE and Path FEBE value from the corresponding registers of the transmit frame handler to Z2 and G1 bytes of SOH/POH in the transmit overhead memory.

Transmit Program Memory

The transmit program memory stores up to 512 steps of instruction codes for the transmit processor.

Transmit Cell Handler

The transmit cell handler read cell data from the transmit cell FIFO and calculates and inserts HEC field and send the cell data to the transmit frame handler. Transmit of cell can be stopped by register control when HALT bit is set in the GFC field of received cells.

Transmit Cell FIFO

The transmit cell FIFO can store up to 4 cells. The FIFO depth can be programmed to be 1, 2, 3 and 4. When an entire cell is stored, the full flag is set and the transmit cell handler begins to read the cell data. The write port of the FIFO operates on the cell interface clock provided from the ATM layer while the read port operates on the network clock.

Transmit Cell Interface

The transmit cell interface receives transmit cells from ATM layer and stores them into the receive cell FIFO. The cell transfer begins when the cell FIFO has space for an entire cell. UTOPIA Level1 and Level2 are both supported. The data bus width is selectable between 8 bits and 16 bits.

Host Interface

PLC2 registers and internal memories can be accessed via the host interface. ALE (Address Latch Enable) signal and the address latch is included so as to allow address/data multiplexed bus. The registers are accessed directly while internal memories are accessed via MEMAH/L and MEMD port.

A.2 PLC2 CLOCKING DETAILS

1) RX Serial Clock

RX serial clock is used for the RX serial to parallel converter. The RX serial clock is divided by eight and usually delivered to the main part of RX block. The internally recovered clock or externally provided clock can be selected as the RX serial clock. The selection is made by RCKSEL pin.

< Internal Clock Recovery Mode>

The RX PLL recovers the serial clock from the serial data input RXDP/M. The recovered clock is divided by 8 and compared with reference clock REFCK in RXOOL detector. Initially RX PLL locks to the reference clock. When the frequency of the RX PLL enters within 244ppm of the reference clock, RX PLL tries to lock to the serial data input RXDP/M. Once data lock is successful, RX PLL reverts to the reference clock if the frequency of the recovered clock is not within 244ppm of the reference clock or LOOCP is high and LOOCM is low or no signal transition is detected for 80 bits period. When RCKSEL input is set high, the internally recovered clock is selected as RX serial clock.

< External Serial Clock Mode>

When RCKSEL input is set low, the external serial clock is selected as RX serial clock. The external serial clock is input to PECL input pins RXCIP/M.

(2) RX Main Clock (RXCLKN)

RX main clock is used in the RX main part of PLC2 where the SOH/POH processing, cell delineation and write of retrieved cell data to receive cell FIFO are executed. Basically RX main clock is divide by 8 of RX serial clock. RX serial clock is internally recovered clock or externally provided clock. When RCKSEL pin is set high, the internally recovered clock is selected. When RCKSEL is set low, the externally provided clock is selected. The selected clock is divided by 8 and is input to the RXOOL detector. When the divided by 8 clock is out of 244ppm of the reference clock, RXOOL is set high and the reference clock, REFCK is selected as RX main clock. REFCK is also selected when the diagnostic loop back mode is enabled.

(3) RX Cell Interface Clock (RXCLKC)

RX cell interface clock, RXCLKC is input from ATM layer. It is used to read cells from the receive cell FIFO and transfer them to ATM layer. The RXCLKC frequency is required to be from 20MHz to 33MHz for UTOPIA Level-1 operation and up to 40MHz for UTOPIA Level-2 operation.

(4) TX Serial Clock

< Loop Timing Mode>

PLC2 enters loop timing mode when LOOPT bit is set high in LOOP register. In loop timing mode, RX serial clock is used as TX serial clock. RX serial clock can be internally recovered clock or externally provided serial clock RXCIP/M dependent on

RCKSEL input. When the internally recovered clock is selected as RX serial clock and it can not lock to serial data input, RX PLL locks to REFCK and continues to provide serial clock to TX line I/F block.

< External Transmit Clock Mode>

When LOOPT bit is set low in LOOP register and TCKSEL is set low, external serial clock , TXCIP/M is selected as TX serial clock.

< Internal TX Serial Clock Synthesis Mode>

When LOOPT bit in LOOP register is set low and TCKSEL input is set high, TX PLL output is selected as TX serial clock. TX PLL generates 8 times frequency of the reference clock, REFCK. When REFCK is 19.44MHz, TX PLL generates 155.52MHz. When REFCK is 6.48MHz, TX PLL generates 51.84MHz. TX PLL output is divided by eight and compared with REFCK. When the divided clock is not within 244ppm of REFCK, TXOOL is set high.

< Line Loop Back Mode>

PLC2 enters line loop back mode when LOOP2 bit is set high in LOOP register. In loop timing mode, RX serial clock is used as TX serial clock. RX serial clock can be internally recovered clock or externally provided serial clock RXCIP/M dependent on RCKSEL input. When the internally recovered clock is selected as RX serial clock and it can not lock to serial data input, RX PLL locks to REFCK and continues to provide serial clock to TX line I/F block.

(5) TX Main Clock

TX main clock is used in TX main part where transmit data is processed in 8 bit parallel.

< Loop Timing Mode>

When LOOPT bit in LOOP register is set high, divided by eight of RX serial clock is selected as TX main clock. When RX serial clock is RX PLL output and RX PLL can not lock to the receive data, TX main clock is automatically changed to the reference clock, REFCK.

< External Transmit Clock Mode>

When LOOPT bit in LOOP register is set low and TCKSEL is set low, divided by eight of external serial clock input TXCIP/M is selected as TX main clock.

< Internal TX Serial Clock Synthesis Mode>

When LOOPT bit in LOOP register is set low and TCKSEL is set high, REFCK is selected as TX main clock.

< Line Loop Back Mode>

When LOOP2 bit in LOOP register is set high, PLC2 enters line loopback mode and the divided by eight of RX serial clock is selected as TX main clock. When RX serial clock is RX PLL output and RX PLL can not lock to the receive data, TX main clock is

automatically changed to the reference clock, REFCK.

(6) TX Cell Interface Clock (TXCLKC)

TX cell interface clock, TXCLKC is delivered from ATM layer. It is used to receive cells from ATM layer and write them to the transmit FIFO. The TXCLKC frequency is required to be within 20MHz to 33MHz for UTOPIA Level-1 operation and up to 40MHz for UTOPIA Level-2 operation.

(7) Host Interface Clock (CLK)

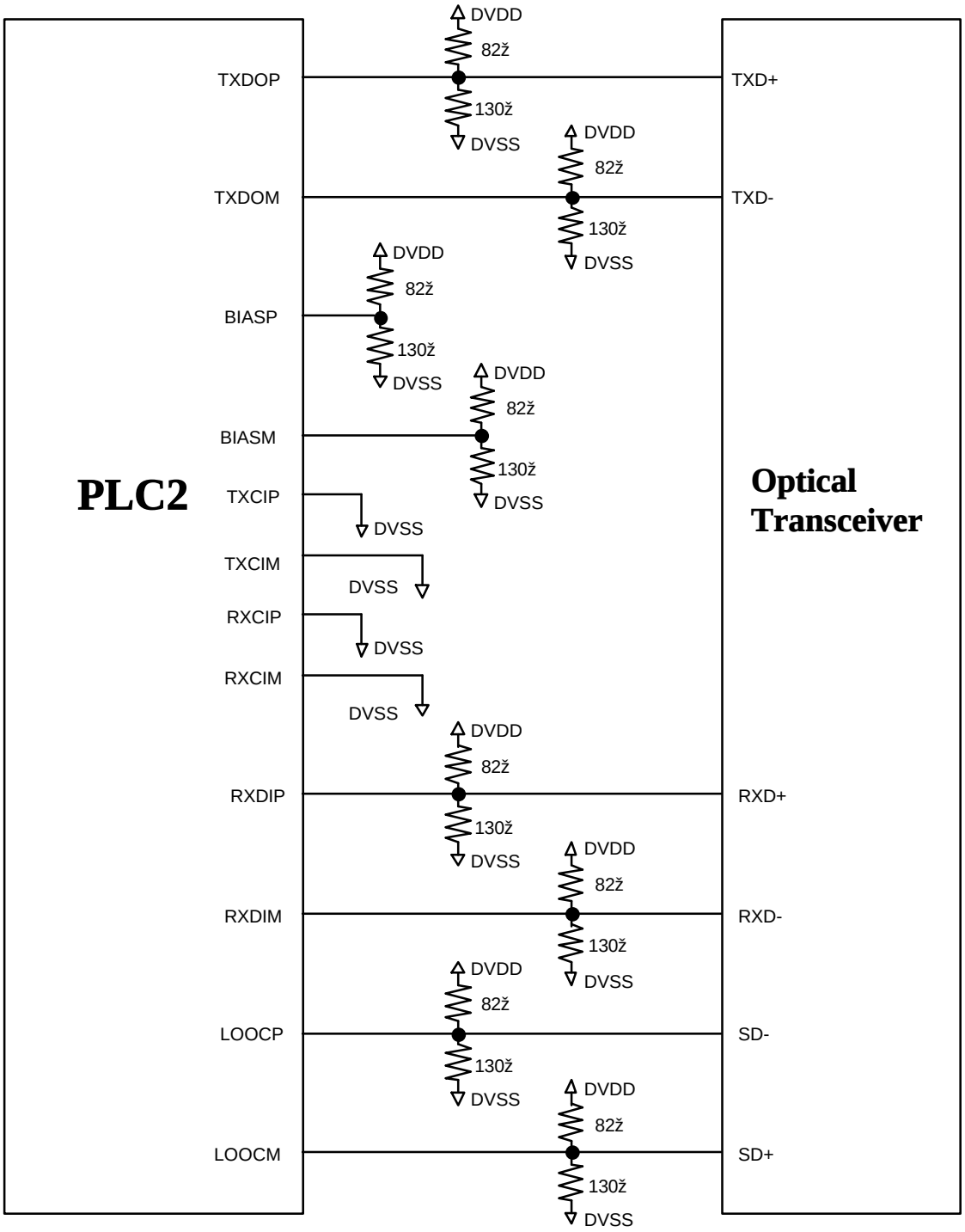
Host interface clock, CLK is used to the host register read/write operation. It is recommended to be around 20MHz. For instance, CLK input can be the same as REFCK input, i.e. 19.44MHz/6.48MHz.

A.3 PLC2 APPLICATION GUIDANCE

-Connection between PLC2 and an optical transceiver

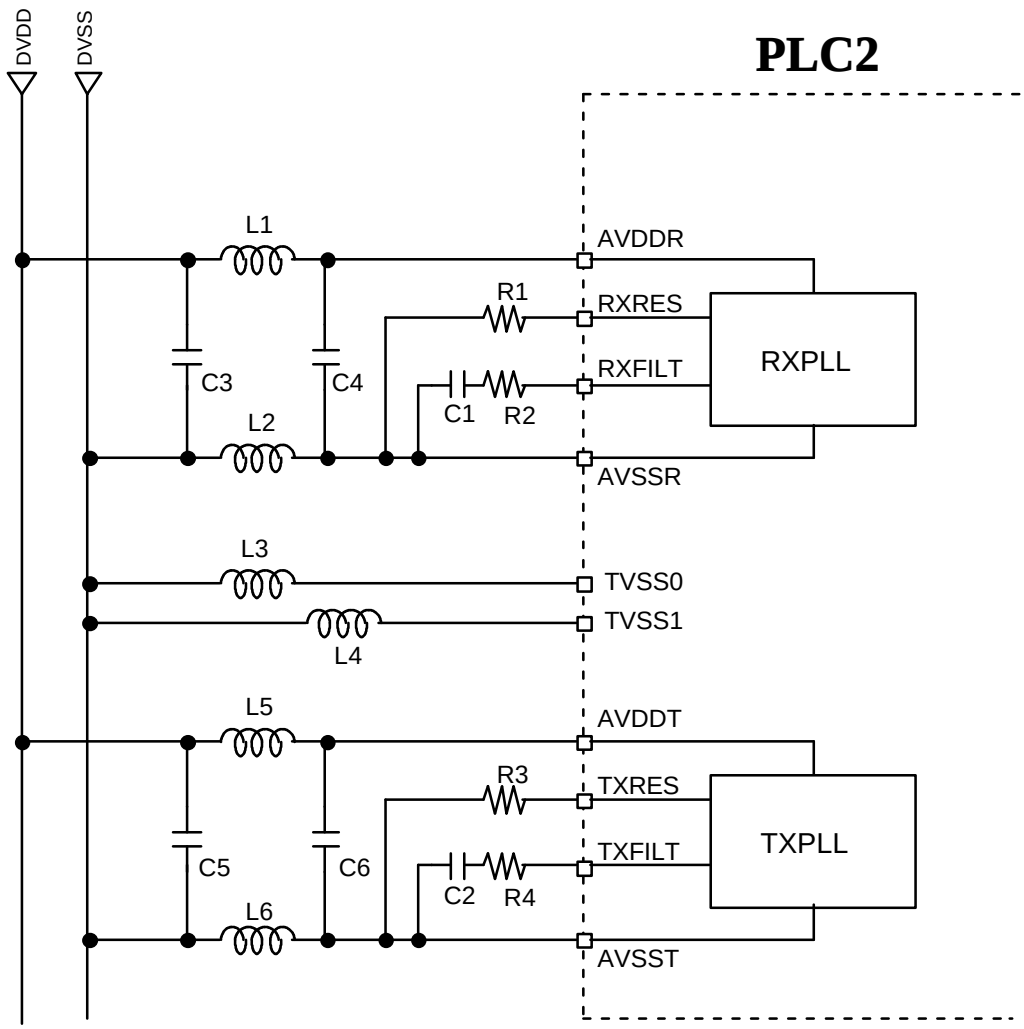
-PLC2 analog components connection

-Supplemental information about PLC2 application board design



It is assumed that SD is asserted high when certain level of optical signal is detected. If SD output of the optical transceiver has single ended, meaning that only SD+ is output, then LOOCP input should be tied to 3.7V. It is realized, for instance, by tying LOOCP to DVDD via1.3K ž and to DVSS via 3.7k ž.

Connection between PLC2 and an optical transceiver

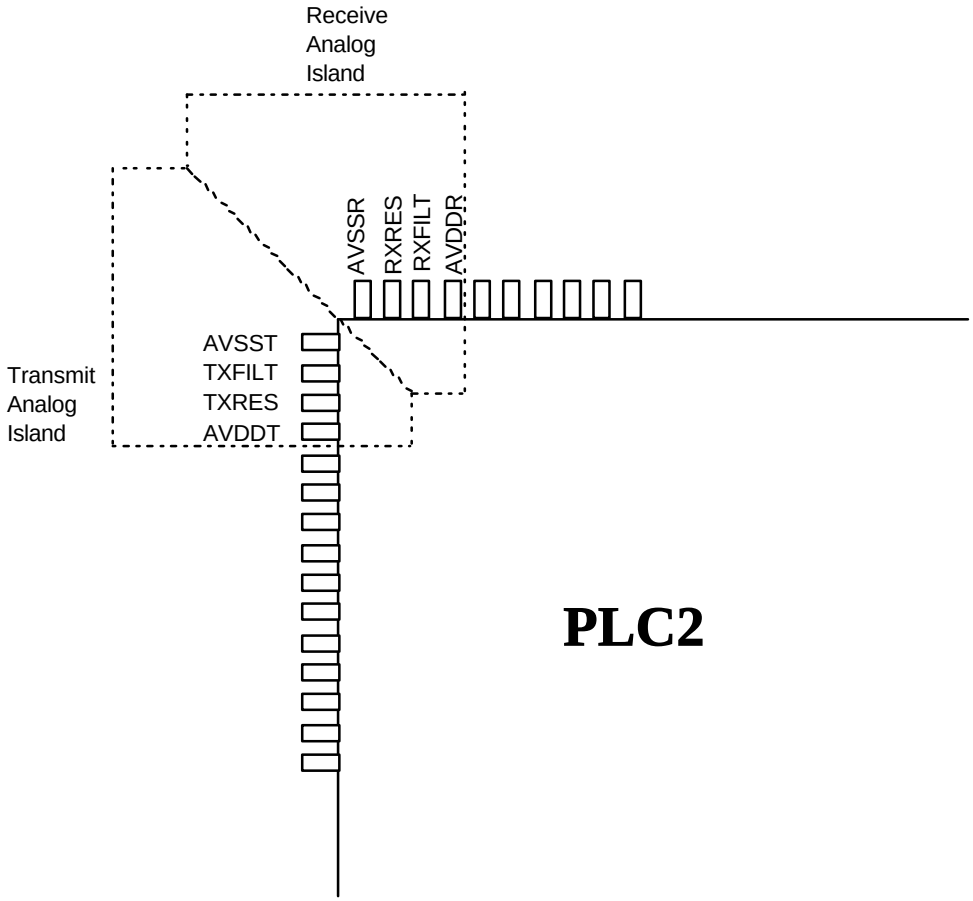


L1~L6: Ferrite bead

R1: TBD.
R2: TBD.
R3: TBD.
R4: TBD.

C1: TBD.
C2: TBD.
C3: 0.1µF & 1.0µF
C4: 0.1µF & 1.0µF
C5: 0.1µF & 1.0µF
C6: 0.1µF & 1.0µF

PLC2 Analog Components Connection



1. Resistors and capacitors connected to RXRES or RXFILT should be included in receive analog island.
2. Resistors and capacitors connected to TXRES or TXFILT should be included in transmit analog island.
3. These analog island should be as small as possible to reduce coupling with surrounding digital area.
3. Digital signal lines should not run over analog islands.
4. Ideally every power pins should have 0.1µF and 4,7 µF decoupling chip capacitors.
5. Ideally every PECL terminators should have 0.1 µF decoupling chip capacitors.

Supplemental information about PLC2 application board design