SC1480
DDR Memory Power Supply Controller

POWER MANAGEMENT

Description

The SC1480 is a single output, constant on-time synchronous-buck, pseudo-fixed frequency, PWM controller intended for use in notebook computers and other battery operated portable devices. Features include high efficiency and fast dynamic response with no minimum on time, a reference input and a buffered REFOUT pin capable of sourcing 3mA. The excellent transient response means that SC1480 based solutions will require less output capacitance than competing fixed frequency converters.

The frequency is constant until a step in load or line voltage occurs, at which time the pulse density and frequency will increase or decrease to counter the change in output or input voltage. After the transient event, the controller frequency will return to steady state operation.

The SC1480 incorporates two power-reducing states, standby and shutdown. In standby mode, the switcher output is shutdown but the buffered reference output stays up, reducing quiescent current to a low 125µA. This is particularly useful for reducing battery draw in systems which implement a suspend-to-RAM (S3) state. The SC1480 can be completely shut down, drawing less than 10µA.

The integrated gate drivers feature adaptive shoot-through protection and soft switching. Additional features include cycle-by-cycle current limit, digital soft-start, overvoltage and under-voltage protection, and a PGOOD output.

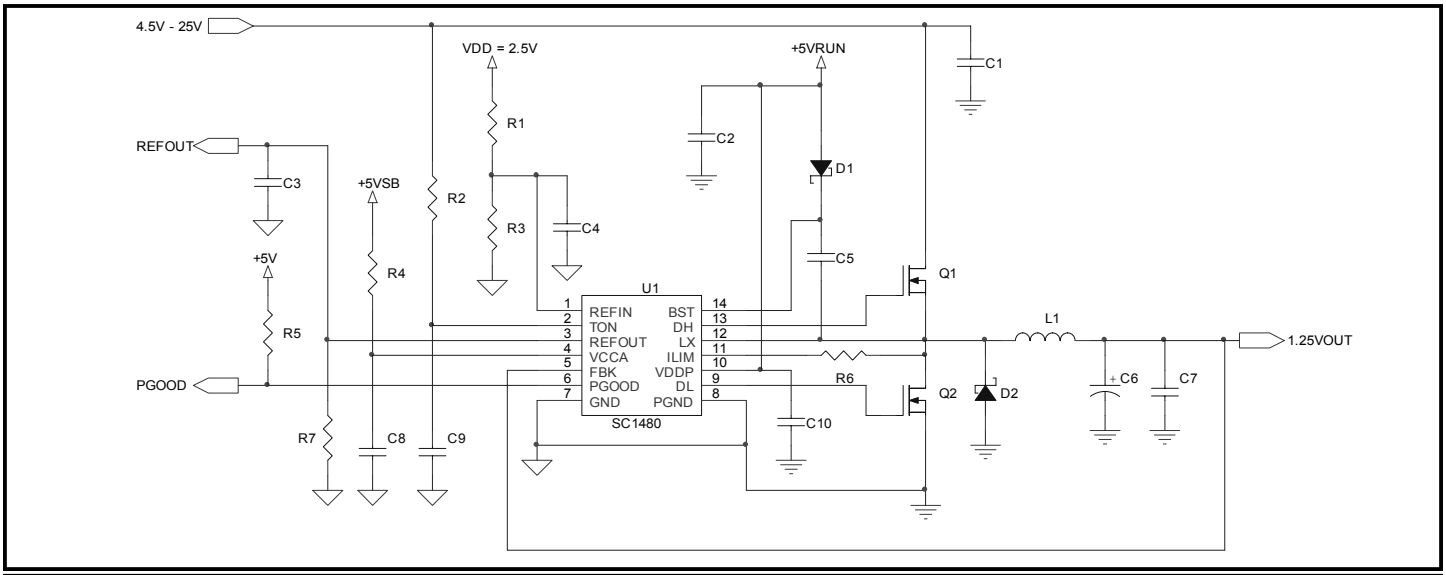
Features

- Constant on-time for fast dynamic response
- Programmable VOUT based on external reference
- VIN range = 1.8V – 25V
- DC current sense using low-side RDS(ON) sensing or sense resistor
- 3mA reference output buffer
- Low power S3 state
- Resistor programmable frequency
- Cycle-by-cycle current limit
- Digital soft start
- Output current source-sink capability
- Overvoltage/under-voltage fault protection and PGOOD output
- Under 10uA typical shutdown current
- Low quiescent power dissipation
- 14-Pin TSSOP package. Also available in Lead-free package which is fully WEEE and RoHS compliant
- Industrial temperature range
- Integrated gate drivers with soft switching
- Efficiency >90%

Applications

- Notebook computers
- CPU I/O supplies
- Handheld terminals and PDAs
- LCD monitors
- Network power supplies

Typical Application Circuit



Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied.

Pin Combination	Symbol	Maximum	Units
TON to AGND		-0.3 to +25.0	V
DH, BST to AGND		-0.3 to +30.0	V
LX to AGND		-2.0 to +25.0	V
AGND to PGND		-0.3 to +0.3	V
BST to LX		-0.3 to +6.0	V
VCCA, VDDP to AGND		-0.3 to +6.0	V
FB, PGOOD, REFIN, ILIM, REFOUT, DL to PGND		-0.3 to +6.0	V
Thermal Resistance, Junction to Ambient(4)	θ_{JA}	100	°C/W
Operating Junction Temperature Range	T_J	-40 to +125	°C
Storage Temperature Range	T_{STG}	-65 to +150	°C
Lead Temperature (Soldering) 10 Sec.	T_{LEAD}	300	°C

Electrical Characteristics

Test Conditions: V_{IN} = 2.5V, REFIN = 1.25, VCCA = VDDP = 5.0V, V_{OUT} = 1.25V, R_{TON} = 1M (300kHz), 0.1% Resistor Dividers

Parameter	Conditions	25°C			-40°C to 125°C		Units
		Min	Typ	Max	Min	Max	
Input Supplies							
VCCA Input Voltage			5.0		4.5	5.5	V
VDDP Input Voltage			5.0		4.5	5.5	V
VIN Input Voltage		2.0		25			V
VDDP Operating Current	FB > regulation point, I_{LOAD} = 0A		5			10	µA
VCCA Operating Current	FB > regulation point, I_{LOAD} = 0A		700			1100	µA
VCCA Standby Current	VDDP < VDDP UV Threshold No Load On REFOUT		125				µA
TON Operating Current	R_{TON} = 1M (300kHz)		15				µA
Shutdown Current							
(REFIN = 0V)	VCCA		5			10	µA
	VDDP + VIN		5			10	µA
Controller							
Error Comparator Threshold (FBK Turn-on Threshold) (1)	With Respect to REFOUT VCCA = 4.5V to 5.5V		REFOUT		REFOUT -10	REFOUT +10	mV

Electrical Characteristics Cont.

Test Conditions: V_{IN} = 2.5V, REFIN = 1.25, VCCA = VDDP = 5.0V, V_{OUT} = 1.25V, R_{TON} = 1M (300kHz), 0.1% Resistor Dividers

Parameter	Conditions	25°C			-40°C to 125°C		Units
		Min	Typ	Max	Min	Max	
On-Time	R_{TON} = 1M (300kHz) VIN = 2.5V		1660		1411	1909	ns
	R_{TON} = 500K (600kHz) VIN = 2.5V		913		776	1050	ns
Minimum Off Time			400			550	ns
Line Regulation Error	VCCA, VDDP = 4.5V to 5.5V Vin = 4.5V to 25V		0.04				%/V
Load Regulation Error	ILIM - PGND = 0V to 0°C Limit		0.3				%
FBK Input Resistance			500				kΩ
Over-Current Sensing							
ILIM Sink Current			10		9	11	µA
Current Comparator Offset	PGND - ILIM				-5	5	mV
Reference Buffer							
REFOUT Source Current					3		mA
REFIN Enable Threshold			0.8		0.55	1.0	V
REFIN Hysteresis			40				mV
Offset Voltage	REFOUT current = 0mA				-10	10	mV
	REFOUT current = 3mA				-12.5	12.5	mV
Fault Protection							
Current Limit (Positive) (2)	PGND-LX, R_{ILIM} = 5k		50		40	60	mV
	PGND-LX, R_{ILIM} = 10k		100		90	110	mV
	PGND-LX, R_{ILIM} = 20k		200		180	220	mV
Current Limit (Negative)	PGND-LX		-140		-200	-100	mV
Output Under-Voltage Fault	With respect to REFOUT		-20		-28	-15	%
Output Over-Voltage Fault	With respect to REFOUT		+10		+8	+12	%
Over-Voltage Fault Delay	FBK forced above OV Vth		2.0				µs
PGOOD Low Output Voltage	Sink 1mA					0.4	V
PGOOD Leakage Current	FBK in regulation, PGOOD = 5V					1	µA
PGOOD UV Threshold	With respect to REFOUT		-10		-12	-8	%

Electrical Characteristics Cont.

Test Conditions: V_{IN} = 2.5V, REFIN = 1.25, VCCA = VDDP = 5.0V, V_{OUT} = 1.25V, R_{TON} = 1M (300kHz), 0.1% Resistor Dividers

Parameter	Conditions	25°C			-40°C to 125°C		Units
		Min	Typ	Max	Min	Max	
PGOOD Fault Delay	FB forced outside PGOOD window.		2.0				µs
VCCA Under Voltage Threshold	Rising Edge Hysteresis 100mv		4.0		3.7	4.3	V
VDDP Under Voltage Threshold			3.3		3.0	3.75	V
VDDP Under Voltage Hysteresis			250				mV
Over Temperature Lockout	10°C Hysteresis		165				C
Soft Start							
Soft-Start Ramp Time	REFIN high to full current limit.		1.6				ms
Under-Voltage Blank Time	SMPS Turn-On		2				ms
Gate Drivers							
Dead Time	DH or DL rising		30				ns
DL Pull-Down Resistance	DL low		0.8			1.6	Ω
DL Pull-Up Resistance	DL high		2			4	Ω
DH Pull-Down Resistance	DH low, BST - LX = 5V		2			4	Ω
DH Pull-Up Resistance	DH high, BST - LX = 5V		2			4	Ω
DL Sink Current	DL - PGND = 2.5V		2				A
DL Source Current	VDDP - DL = 2.5V		1				A
DH Sink Current	DH - LX = 2.5V, BST - LX = 5V		1				A
DH Source Current	BST - DH = 2.5V, BST - LX = 5V		1				A

Notes:

(1) When the inductor is in continuous conduction mode, the output voltage will have a DC regulation level higher than the error-comparator threshold by 50% of the ripple voltage.

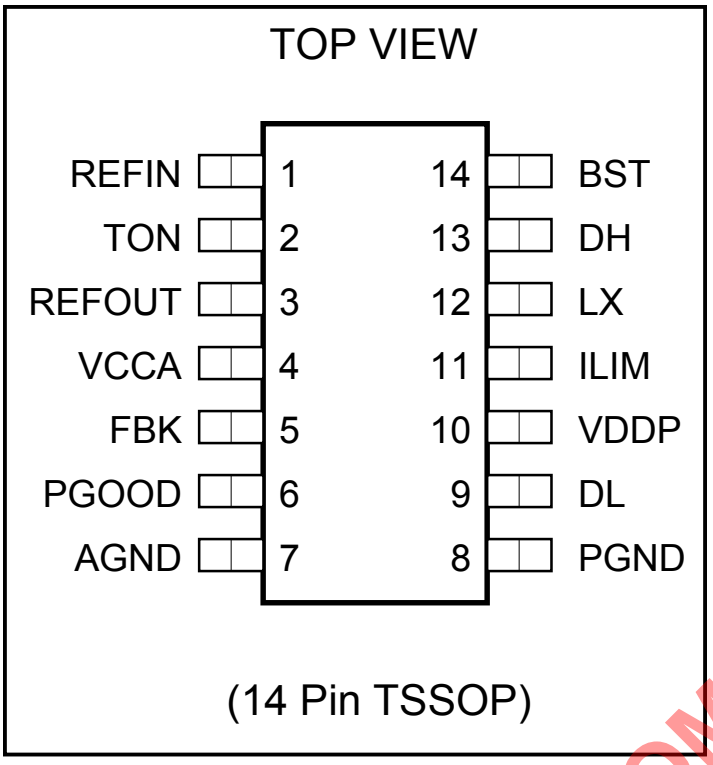
(2) Using a current sense resistor, this measurement relates to PGND minus the voltage of the source on the low-side MOSFET.

(3) This device is ESD sensitive. Use of ESD handling precautions is required.

(4) Measured in accordance with JESD51-1, JESD51-2 and JESD51-7.

POWER MANAGEMENT

Pin Configuration



Ordering Information

Device (1)	Package
SC1480ITSTR	TSSOP-14
SC1480ITSTRT(2)	TSSOP-14
SC1480EVB	Evaluation Board

Notes:
(1) Only available in tape and reel packaging. A reel contains 2500 devices.
(2) Lead free product. This product is fully WEEE and RoHS compliant.

Pin Descriptions

Pin #	Pin Name	Pin Function
1	REFIN	External Reference input. Tie to ground to disable SMPS and reference buffer.
2	TON	On-time set input. Sets on-time of upper MOSFET via series resistor to the input supply.
3	REFOUT	Reference output pin. Can source 3mA.
4	VCCA	Supply voltage input for the analog supply. Connect through a RC filter to +5V.
5	FBK	Feedback input. Connect from resistor divider at output of SMPS to select output voltage.
6	PGOOD	Power Good open drain NMOS output. Goes high after a fixed clock cycle delay following power up.
7	AGND	Analog ground.
8	PGND	Power ground.
9	DL	Gate drive output for the low side MOSFET switch.
10	VDDP	+5V supply voltage input for the gate drivers. Tie to ground to disable SMPS.
11	ILIM	Current limit input. Connect to drain of low-side MOSFET for RDS(on) sensing or the source for resistor sensing through a threshold sensing resistor. See applications section for more information.
12	LX	Switching node inductor connection.
13	DH	Gate drive output for the high side MOSFET switch.
14	BST	Boost capacitor connection for the high side gate drive.

Block Diagram

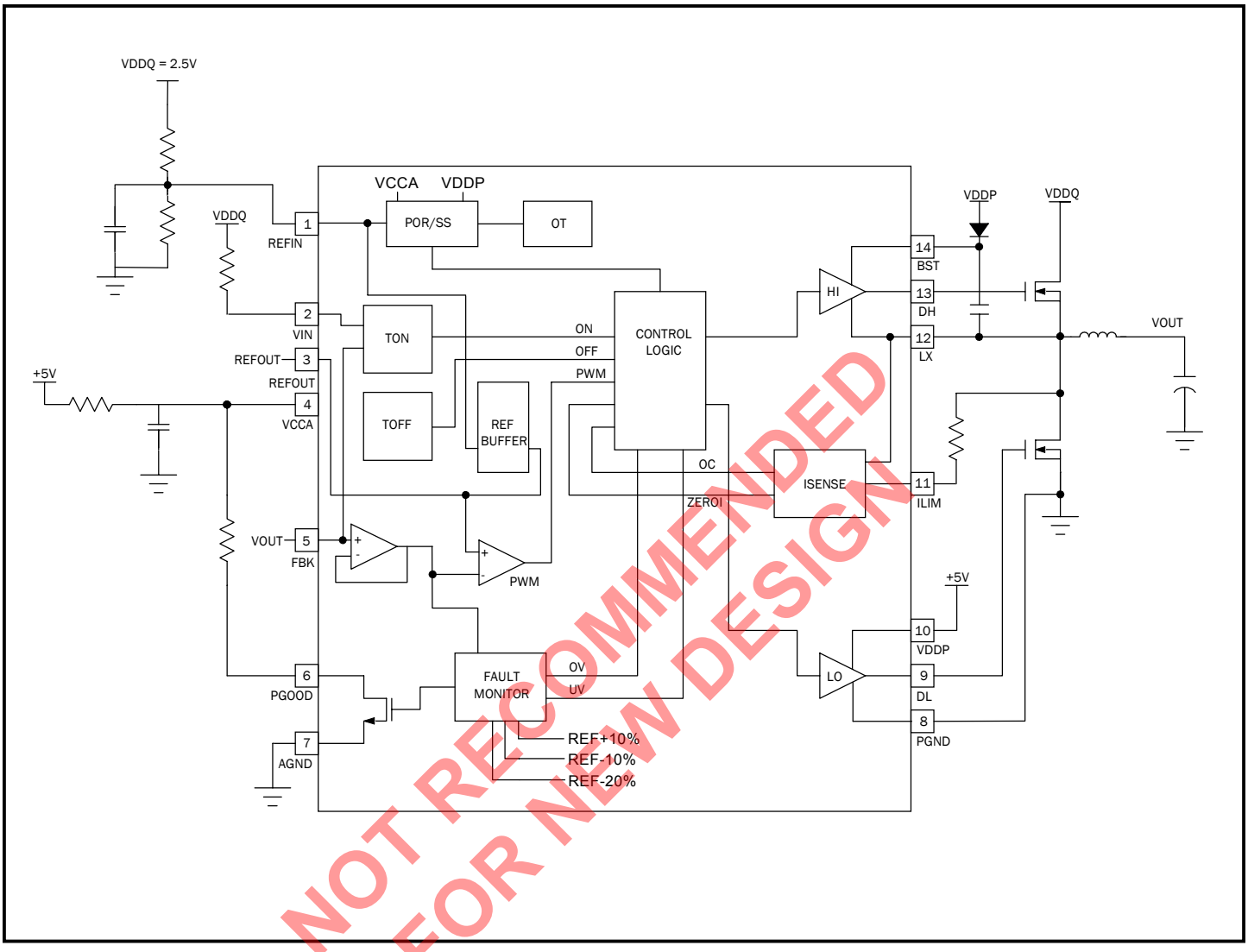


FIGURE 1

Applications Information

+5V Bias Supply

The SC1480 requires an external +5V bias supply in addition to the battery. If stand-alone capability is required, the +5V supply can be generated with an external linear regulator. There are two inputs for the external +5V bias supply, VCCA & VDDP. The VCCA input powers the analog section of the SC1480 while the VDDP input provides power to the upper and lower gate drivers. VCCA will need to be decoupled from the +5V supply through a 10 Ohm resistor and the addition of a filter capacitor from VCCA to ground. VCCA and VDDP must be separate in order to utilize the low power S3 state of the SC1480. The battery input VIN and the +5V input VCCA can be tied together if the input voltage is fixed from +4.5V to +5.5V; however, as before, VCCA will need to be decoupled from the +5V supply through a 10 Ohm resistor and the addition of a filter capacitor from VCCA to ground.

Pseudo-Fixed Frequency Constant On-Time PWM Controller

The PWM control architecture consists of a constant-on-time, pseudo fixed frequency PWM controller, (Figure 1). The output ripple voltage developed across the output filter capacitors ESR provides the PWM ramp signal eliminating the need for a current sense resistor. The high-side switch on-time is determined by a one-shot whose period is directly proportional to output voltage and inversely proportional to input voltage. A second one-shot sets the minimum off-time to 400ns typically.

On-Time One-Shot (T_{ON})

The on-time one-shot comparator has two inputs. One input looks at the output voltage, while the other input samples the input voltage and converts it to a current. This input proportional current is used to charge an internal on-time capacitor. The TON time is the time required for the voltage on the capacitor to charge from zero volts to VOUT, thereby making the on-time of the high-side switch directly proportional to output voltage and inversely proportional to input voltage. This implementation results in a nearly constant switching frequency without the need of a clock generator.

$$T_{ON} = 3.3x10^{-12} \bullet (R_{TON} + 37x10^{3}) \bullet \left(\frac{V_{OUT}}{V_{IN}} \right) + 50\eta S$$

R_{TON} is a resistor connected from the input supply to the TON pin. The graph on page 19 shows the relationship between R_{TON} and switching frequency.

Reference I/O

The reference input can be generated off of a 2.5V or VDDQ supply by a simple resistive divider. Resistors less than 100k Ohms should be used and a small filter capacitor from the reference input to ground of 0.1uF will remove any ripple voltage present on the input. The input has a common mode range of the REFIN threshold to 2.5V.

The voltage on the reference input passes through a unity gain buffer prior to being sent to REFOUT. This reference output has a class A output stage with 3mA of sourcing capacity. It has a pull-down impedance of 50k. The output will require a small RC filter of 10 Ohms and 1µF to maintain stability.

Shutdown, Suspend to RAM and Run Mode

The SC1480 has three modes of operation: shutdown, suspend to RAM, and run mode. All three modes must have VCCA connected at all times. Shutdown mode is controlled by REFIN. When REFIN is below 0.8V, the reference buffer will be off and the SMPS is disabled. In this mode the bias current of the device will be less than 10µA.

Suspend to RAM, or S3 State, is controlled by REFIN and VDDP. With REFIN is above 0.8V and VDDP is low (below 3V), the device will output the reference voltage onto REFOUT, but the SMPS is disabled. In this mode the bias current is approximately 125µA.

Run mode is activated by maintaining REFIN above 0.8V and VDDP above 3V. In this mode the reference and SMPS are active.

Current Limit Circuit

Current limiting of the SC1480 can be accomplished in two ways. First, the device can implement on-state resistance of the low-side MOSFET as the current sensing element (RDS_{ON} sensing). Second, the device can accept a resistive element in the low-side source ($R_{SENSE,}$ resistor sensing). The second method offers greater accuracy of the current limit threshold over RDS_{ON} sensing, at the added expense of a sense resistor and associated efficiency loss.

Whether RDS_{ON} sensing or R_{SENSE} resistor sensing is used,

Applications Information (Cont.)

a scaling resistor between LX and ILIM is required. This resistor, R_{ILIM}, is connected to a 10µA current source within the SC1480 through the ILIM pin. This sets a voltage drop equal to 10µA times R_{ILIM}. As the current increases through the lower MOSFET, the phase pin voltage will decrease until the offset voltage caused by R_{ILIM} is reached and ILIM < PGND. At this point an overcurrent trip signal is issued. Current limiting will prevent the firing of a DH on-pulse, thereby reducing the switching frequency. As the frequency decreases, the output voltage will drop until an under-voltage shutdown is reached.

The current sensing circuit actually limits the inductor valley current (see Figure 2). This means that if the current limit is set to 10A, the peak current through the inductor would be 10A plus the peak ripple current, and the average current through the inductor would be 10A plus 1/2 the peak-to-peak ripple current. The equations for setting the valley current and calculating the average current through the inductor are shown below:

$$IL_{OC}(Valley) = 10\mu A \bullet \frac{R_{ILIM}}{RDS_{ON}}$$

$$IL_{OC}(Average) = IL_{OC}(Valley) + \frac{\Delta I_L}{2}$$

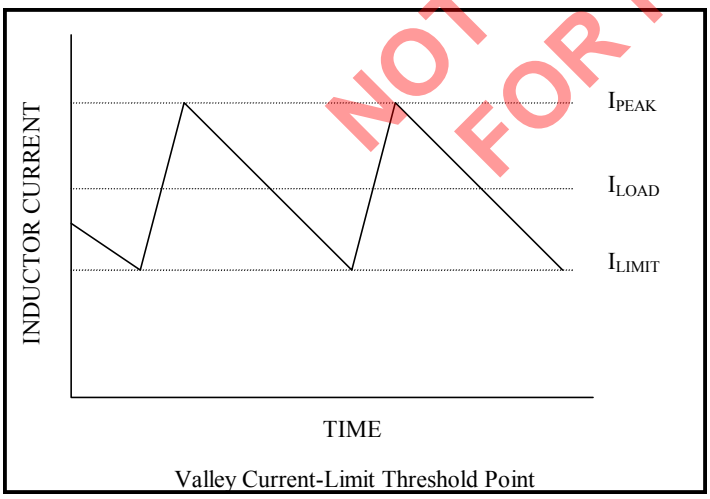


FIGURE 2

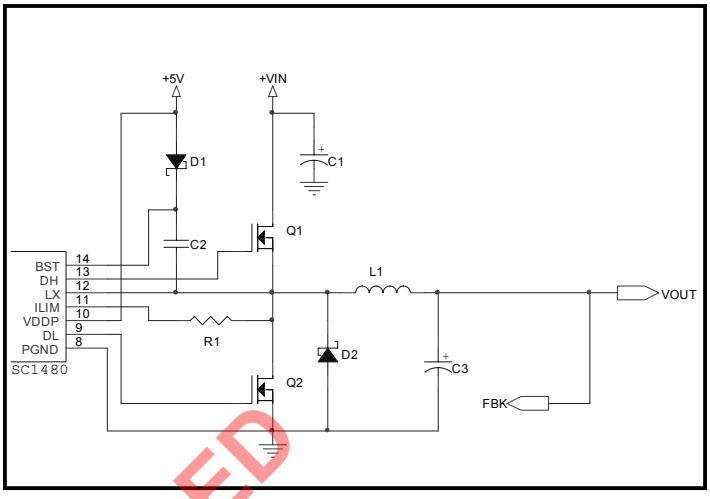


FIGURE 3

Schematic of RDS_{ON} sensing circuit is shown in Figure 3 with RDS_{ON} of Q2.

Similarly, for resistor sensing, the current through the lower MOSFET and the source sense resistor develops a voltage that opposes the voltage developed across R_{ILIM}. When the voltage developed across the R_{SENSE} resistor reaches voltage drop across $R_{ILIM,}$ an overcurrent will be issued. The overcurrent equation when using an external sense resistor is:

$$IL_{OC}(Valley) = 10\mu A \bullet \frac{R_{ILIM}}{R_{SENSE}}$$

Schematic of resistor sensing circuit is shown in Figure 4 with R_{ILIM} = R1 and R_{SENSE} = R2.

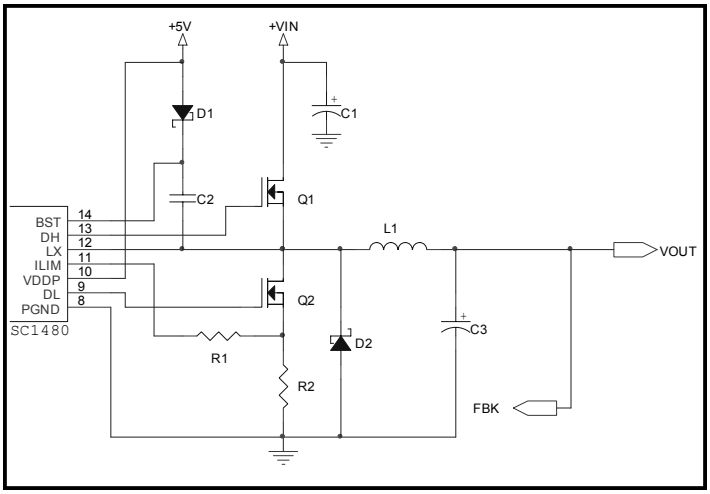


FIGURE 4

Power Good Output

Power good is an open-drain output and requires a pull-up resistor. When the output voltage is 10% above or below its set voltage, PGOOD gets pulled low. It is held low until the output voltage returns to within 10% of the output set voltage. PGOOD is also held low during start-up and will not be allowed to transition high until the output reaches 90% of its set voltage. There is a slight delay built into the PGOOD circuit to prevent false transitions.

Output Overvoltage Protection

When the output exceeds 10% of the its set voltage the low-side MOSFET is latched on. It stays latched and the SMPS is off until the enable input or POR is toggled. There is a slight delay built into the OV protection circuit to prevent false transitions.

Output Undervoltage Protection

When the output is 20% below its set voltage the output is latched in a tristated condition, and the SMPS is off until the enable input or POR is toggled. There is a slight delay built into the UV protection circuit to prevent false transitions.

POR, UVLO and Softstart

An internal power-on reset (POR) occurs when VCCA exceeds 3V, resetting the fault latch and soft-start counter, and preparing the PWM for switching. VCCA undervoltage lockout (UVLO) circuitry inhibits switching and forces the DL gate driver high until VCCA rises above 4.1V. At this time the circuit will come out of UVLO and begin switching, and the softstart circuit being enabled, will progressively limit the output current over a predetermined time period. The ramp occurs in four steps: 25%, 50%, 75% and 100%, thereby limiting the slew rate of the output voltage. There is 100mV of hysteresis built into the UVLO circuit and when the VCCA falls to 4.0V the output drivers are shutdown and tristated.

MOSFET Gate Drivers

The DH and DL drivers are optimized for driving moderate-sized high-side, and larger low-side power MOSFETs. An adaptive dead-time circuit monitors the DL output and prevents the high-side MOSFET from turning on, until DL is fully off, and conversely, monitors the DH output and prevents the low-side MOSFET from turning on until DH is fully off. Be sure there is low resistance and low inductance between the DH and DL outputs to the gate of each MOSFET.

The high-side gate driver is equipped with turn-on soft switching to reduce gate drive power dissipation. When a DH turn-on is initiated the pull-up resistance is 10 Ohms. This limits the peak high-side gate current before the MOSFET is conducting current. The peak gate current plays a large role in gate driver switching losses. When the high-side MOSFET begins conducting, and LX starts to rise, the pull-up resistance on DH changes to 2 Ohms.

Design Procedure

Prior to any design of a switch mode power supply (SMPS) for notebook computers, determination of input voltage, load current, switching frequency and inductor ripple current must be specified.

Input Voltage Range

The maximum input voltage (VIN_{MAX}) is determined by the highest AC adaptor voltage. The minimum input voltage (VIN_{MIN}) is determined by the lowest battery voltage after accounting for voltage drops due to connectors, fuses and battery selector switches.

Maximum Load Current

There are two values of load current to consider. Continuous load current and peak load current. Continuous load current has more to do with thermal stresses and therefore drives the selection of input capacitors, MOSFETs and commutation diodes. Whereas, peak load current determines instantaneous component stresses and filtering requirements such as, inductor saturation, output capacitors and design of the current limit circuit.

Switching Frequency

Switching frequency determines the trade-off between size and efficiency. Increased frequency increases the switching losses in the MOSFETs, since losses are a function of VIN^2. Knowing the maximum input voltage and budget for MOSFET switches usually dictates where the design ends up.

Inductor Ripple Current

Low inductor values create higher ripple current, resulting in smaller size, but are less efficient because of the high AC currents flowing through the inductor. Higher inductor values do reduce the ripple current and are more efficient, but are larger and more costly.

Applications Information (Cont.)

The selection of the ripple current is based on the maximum output current and tends to be between 20% to 50% of the maximum load current. Again, cost, size and efficiency all play a part in the selection process.

Design Example

The following design example is for the evaluation board schematic shown on page 16. While most DDR supplies have a maximum load of 3A, the following design was meant for applications beyond DDR memory. Therefore, this design will have an input voltage from 5V to 19V, with an output voltage of 1.25V at 5A of load current.

Inductor Selection

The switching frequency is set to 300kHz which yields a good trade-off of size and efficiency. RTON is chosen to be 1M Ohm for a switching frequency of 300kHz. Because ripple voltage is used as the feedback mechanism of this device, this leads to the choice of the ripple current being 10% of load current. This will give a nice ripple voltage waveform for ensuring proper PWM triggering for this type of controller.

$$\Delta IL = 0.1 \bullet 5 = 0.5A$$

$$L = \frac{V_{OUT} \bullet (V_{IN} - V_{OUT}) \bullet T}{V_{IN} \bullet \Delta I_L}$$

$$L = 4\mu H$$

Setting the Current Limit

The minimum current-limit threshold must be high enough to support the maximum load current. The valley of the inductor current occurs at:

$$ILoad(Max) - \frac{\Delta IL}{2}$$, (see Figure 2) therefore:

$$ILIM(Low) > ILoad(Max) - \frac{\Delta IL}{2}$$

The inductor must not saturate under all conditions of operation. If the current limit is set to 6.5A the maximum current through the inductor will be: $6.5 + \Delta IL = 7A$

Setting the over current to 6.5A is calculated as follows:

$$RILIM = \frac{RDS_{ON} \bullet ILOC}{10\mu A}$$

RDSON of the MOSFET is a nominal 0.013 Ohms, accounting for increased temperature effects use 0.015 Ohm.

$$RILIM = \frac{0.015 \bullet 6.5}{10\mu A} = 10k$$

The inductor chosen was a Panasonic 4µH, 11A inductor.

Similarly, using a Sense resistor to obtain a more accurate current limit would make use of the valley current equation. Thus, for a 0.015 Ohm resistor the RILIM would calculate to the same 10k Ohm ILIM resistor will be $6 \bullet 6 \bullet 0.015 = 0.54W$ effecting the efficiency budget.

Output Capacitor Selection

The output filter capacitor must have low effective series resistance (ESR) to meet the output ripple and load transient requirements, at the same time have high enough ESR to satisfy stability requirements. In addition, the value of output capacitance must be high enough to absorb the inductor energy going from full-load to no-load without tripping the overvoltage protection circuit. For CPU load transients, how much ESR is needed depends upon output voltage variation limits under a CPU load transient. The ESR for this condition is given:

$$ESR = \frac{\Delta V_{OUT}}{I_{LOAD(MAX)}}$$

In non CPU applications, the output capacitor size depends on how much ESR is needed to maintain an acceptable level of output voltage ripple. Under these conditions the ESR value is given:

$$ESR = \frac{\Delta V_{OUT(p-p)}}{I_{LOAD(MAX)}}$$

However, for most CPU applications the minimum capacitance required is limited by the energy absorption of the output capacitor. The equation for determining the minimum capacitance can be found by the following equation:

$$C_{MIN} = \frac{L_{OUT} \bullet I_{OUT}^2}{V_F^2 - V_I^2}$$

Applications Information (Cont.)

Where V_F is the final output voltage after release of the load and V_I is the initial voltage prior to the release of load. If no more than 100mV of output voltage variation is required between V_F and V_I , plugging in the numbers for the application circuit yields minimum output capacitance of 1000µF. As shown, a large amount of capacitance is required to absorb the energy of the inductor during a load release of 5A. In typical DDR memory applications a load release of this magnitude is not an issue and therefore the application circuit can get by with 300µF of output capacitance.

Stability Considerations:

Unstable operation shows up in two related but distinctly different ways: double pulsing and fast-feedback loop instability.

Double-pulsing occurs due to noise on the output or because the ESR is too low, causing not enough voltage ramp in the output signal. This causes the error amplifier to trigger prematurely after the 400ns minimum off-time has expired. Double-pulsing will result in higher ripple voltage at the output, but in most cases is harmless. However, in some cases double-pulsing can indicate the presence of loop instability, which is caused by insufficient ESR. One simple way to solve this problem is to add some trace resistance in the high current output path. A side effect of doing this is output voltage droop with load.

SC1480 ESR Requirements

The constant on-time control used in the SC1480 regulates the ripple voltage at the output capacitor. This signal consists of a term generated by the output ESR of the capacitor and a term based on the increase in voltage across the capacitor due to charging and discharging during the switching cycle. The minimum ESR is set to generate the required ripple voltage for regulation. For most applications the minimum ESR ripple voltage is dominated by PCB layout and the properties of SP or POSCAP type output capacitors. For applications using ceramic output capacitors the absolute minimum ESR must be considered. Existing literature describing the ESR requirements to prevent double pulsing does not accurately predict the performance of constant on-time controllers. A time domain model of the converter was developed to generate equations for the minimum ESR empirically. If the ESR is low enough the ripple voltage is dominated by the charging of the output capacitor. This ripple voltage lags the on-time due to the LC poles and can cause double pulsing if the phase delay exceeds the off-time of the converter. Referring to Figure 3, the equation for the minimum ESR as a function of output capacitance and switching frequency and duty cycle is;

$$ESR > \left(\frac{1+3 \bullet \left(\frac{Fs-200000}{Fs} \right)}{2 \bullet \pi \bullet Cout \bullet Fs \bullet (1-D)^2} \right)$$

Where D = Vout/Vin. Plugging in the numbers for this design ESR > 0.004 Ohms.

Input Capacitor Selection

Input capacitors are selected based upon the input ripple current demand of the converter. First determine the input ripple current expected and then choose a capacitor to meet that demand.

The input RMS ripple current can be calculated as follows:

$$I_{RMS} = \sqrt{V_{OUT} \bullet (V_{IN} - V_{OUT})} \bullet \frac{I_{OUT}}{V_{IN}}$$

Therefore, for a maximum load current of 6.0A , the input capacitors should be able to safely handle 3A of ripple current. For the EVAL board, we chose two 10µF, 25V ceramic capacitors. Each capacitor has a ripple current capability of 2A.

MOSFET Switch Selection

The current selection of MOSFETs are determined by the setting of the overcurrent limit circuit and the maximum input voltage. The next step is to determine their power handling capability. For the EVAL board the ISi4484 meet the voltage and current requirements. This is a 30V, 10A FET. Based on 85°C ambient temperature, 150°C junction temperature and thermal resistance, their power handling is calculated as follows:

Power Limit for Upper & Lower FET:

T_J = 150°C; T_A = 85°C; θ_{JA} = 50°C/W

$$P_T = \frac{T_J - T_A}{\theta_{JA}} = \frac{150 - 85}{50} = 1.3W$$

Each FET must not exceed 1.3W of power dissipation.

MOSFET Power Dissipation
Worst-case conduction losses occur at the duty factor extremes. For the high-side MOSFET, the worst-case conduction power dissipation occurs at minimum battery voltage:

$$P_{DUC} = \frac{V_{OUT}}{V_{IN(MIN)}} \bullet I_{LOAD}^2 \bullet R_{DS(ON)}$$

Typically, a small high-side MOSFET is selected to reduce switching losses at high input voltages. However, the RDS(ON) limits how small the MOSFET can be.
Another element of loss in the upper MOSFET is the switching loss, especially at high input voltages, those seen when the AC adaptor is applied. The upper MOSFET switching losses can be estimated as follows:

$$P_{DUS} = \frac{C_{RSS} \bullet V_{IN(MAX)}^2 \bullet f \bullet I_{LOAD}}{I_{GATE}}$$

Where CRSS is the reverse transfer capacitance of the upper MOSFET and IGATE is the peak gate-drive source/sink current which is approximately 1A for the SC1480.

For the low-side MOSFET the there are only conduction loses to be concerned about since the commutation diode is active while the lower MOSFET switches. The worst-case power dissipation occurs at maximum battery voltage:

$$P_{DLC} = \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right) \bullet I_{LOAD}^2 \bullet R_{DS(ON)}$$

Adding up the power dissipation for each MOSFET can now proceed and the total for each MOSFET should not exceed 1.3W which was calculated earlier to be the maximum power dissipation under worst-case conditions.

Dropout Performance
The output voltage adjust range for continuous-conduction operation is limited by the fixed 500nS (maximum) minimum off-time one-shot. For best dropout performance, use the slowest on-time setting of 200kHz. When working with low input voltages, the duty-factor limit must be calculated using worst-case values for on and off times. The IC duty-factor limitation is given by:

$$DUTY = \frac{T_{ON(MIN)}}{T_{ON(MIN)} + T_{OFF(MAX)}}$$

Be sure to include inductor resistance and MOSFET on-state voltage drops when performing worst-case dropout duty-factor calculations.

Layout Guidelines
As with any high frequency switching regulator, it is advisable to practice a careful layout strategy. This includes keeping loop area as small as possible. And properly decoupling lines that pull large currents in short periods of time. To keep loop area small always use a ground plane and if possible split the plane in two areas, signal GND and power GND, then tie the two together at one point. Be sure that high current paths have low inductance by making trace widths wide where possible. The SC1480 pin-outs contain digital signals on the right and analog signals on the left side of the device. This facilitates the isolation of digital and analog signals enabling effective layout of the device. In summary follow these guidelines for good PC board layout::

- Keep high-current paths short, especially at the ground terminals.
- Tie AGND and PGND together close to the IC.
- Keep the power traces and load connections short. This practice is essential for high efficiency. Using thick copper PC boards (2oz vs 1oz) can enhance full-load efficiency by 1% or more.
- Connect the ILIMIT resistor as close to the lower MOSFET drain as possible, and keep the resistance distance from the ILIM pin to the drain short. This will improve current limit accuracy.

1480 System DC Accuracy
Two IC parameters effect system DC accuracy, the error comparator offset voltage, and the switching frequency variation with line and load. The 1480 regulates to the REFOUT voltage not the REFIN voltage. Since DDR specifications are written with respect to REFOUT, the offset of the reference buffer does not create a regulation error.

Applications Information (Cont.)

The error comparator offset is trimmed so that it trips when VOUT is 1.25 volts +/-1% at room temperature. This offset does not drift significantly with supply and temperature. Thus, the error comparator contributes 1% or less to DC system inaccuracy.

The on pulse in the SC1480 is calculated to give a pseudo fixed frequency. Nevertheless, some frequency variation with line and load can be expected. This variation changes the output ripple voltage. Because constant on regulators regulate to the valley of the output ripple, ½ of the output ripple appears as a DC regulation error. For example, if REFOUT=1.25 volts, then the valley of the output ripple will be 1.25 volts. If the ripple is 20mv with VIN=6, then the DC output voltage will be 1.26 volts. If the ripple is 40mv with VIN=25 volts, then the DC output voltage will be 1.27 volts. The best way to minimize this effect is to minimize the output ripple.

To compensate for valley regulation it is usually desirable to use passive droop. Take the feedback directly from the output side of the inductor incorporating a small amount of trace resistance between the inductor and output capacitor. This trace resistance should be optimized so that at full load the output droops to near the lower regulation limit. Passive droop minimizes the required output capacitance because the voltage excursions due to load steps are reduced. Passive droop also improves stability so it should be used when possible.

Thermal Considerations

The junction temperature of the device may be calculated as follows:

$$T_J = T_A + P_D \bullet \theta_{JA} \quad °C$$

Where:
T_A = ambient temperature (°C)
P_D = power dissipation in (W)
θ_{JA} = thermal impedance junction to ambient from absolute maximum ratings (°C/W)

The power dissipation may be calculated as follows:

$$P_D = VCCA \bullet I_{VCCA} + V_g \bullet Q_g \bullet f \quad W$$

Where:
VCCA = chip supply voltage (V)
I_{VCCA} = operating current (A)
V_g = gate drive voltage, typically 5V (V)
Q_g = FET gate charge, from the FET datasheet (C)
f = switching frequency (kHz)

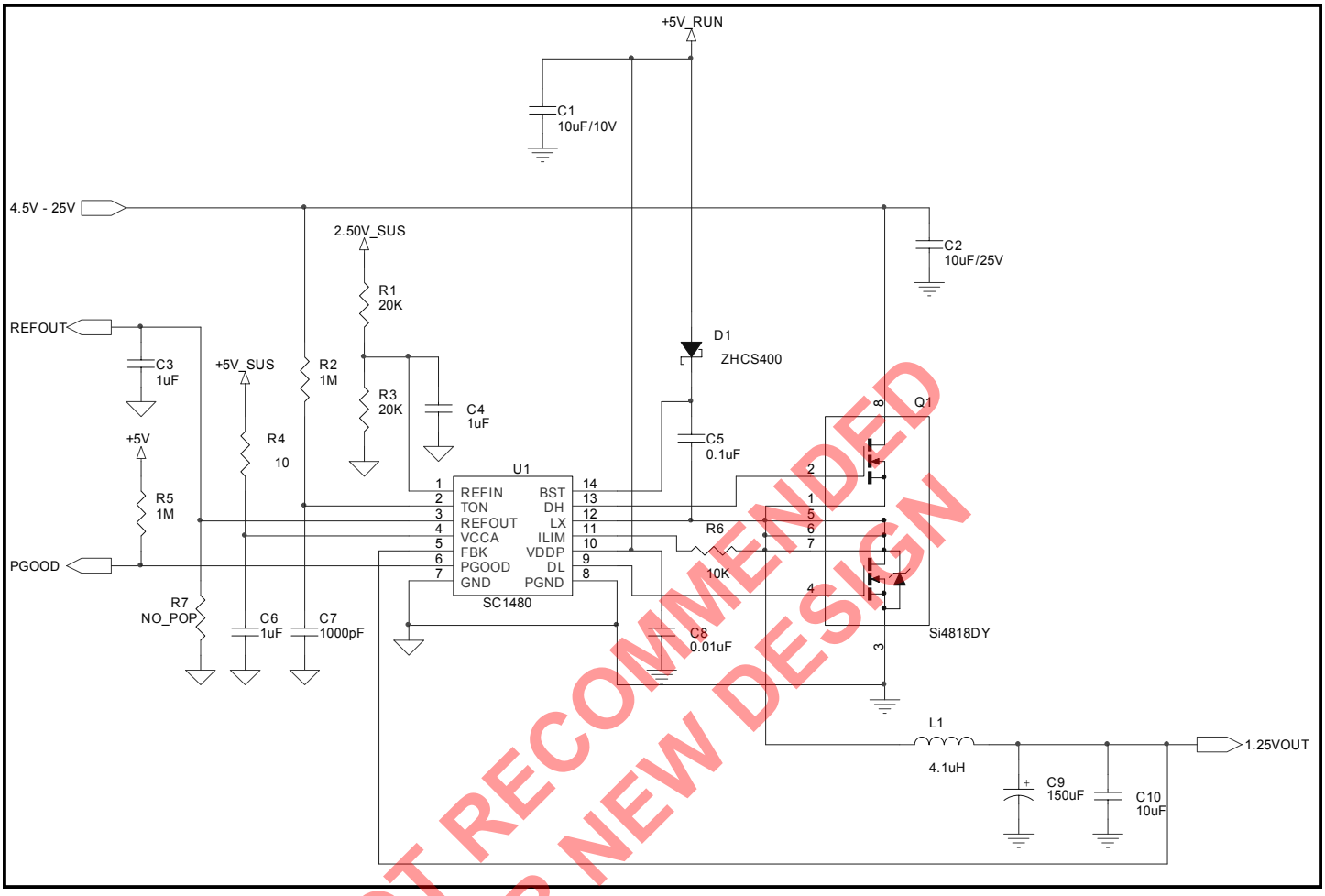
Inserting the following values as an example:
T_A = 85°C
θ_{JA} = 100°C/W
VCCA = 5V
I_{VCCA} = 1100µA (data sheet maximum)
V_g = 5V
Q_g = 60nC
f = 300kHz
gives us:

$$T_J = 85 + \left(5 \bullet 1100 \bullet 10^{-6} + 5 \bullet 60 \bullet 10^{-9} \bullet 300 \bullet 10^{3}\right) \bullet 100 = 95 \quad °C$$

As can be seen, the heating effects due to internal power dissipation are practically negligible, thus requiring no special consideration thermally during layout.

POWER MANAGEMENT

Reference Design



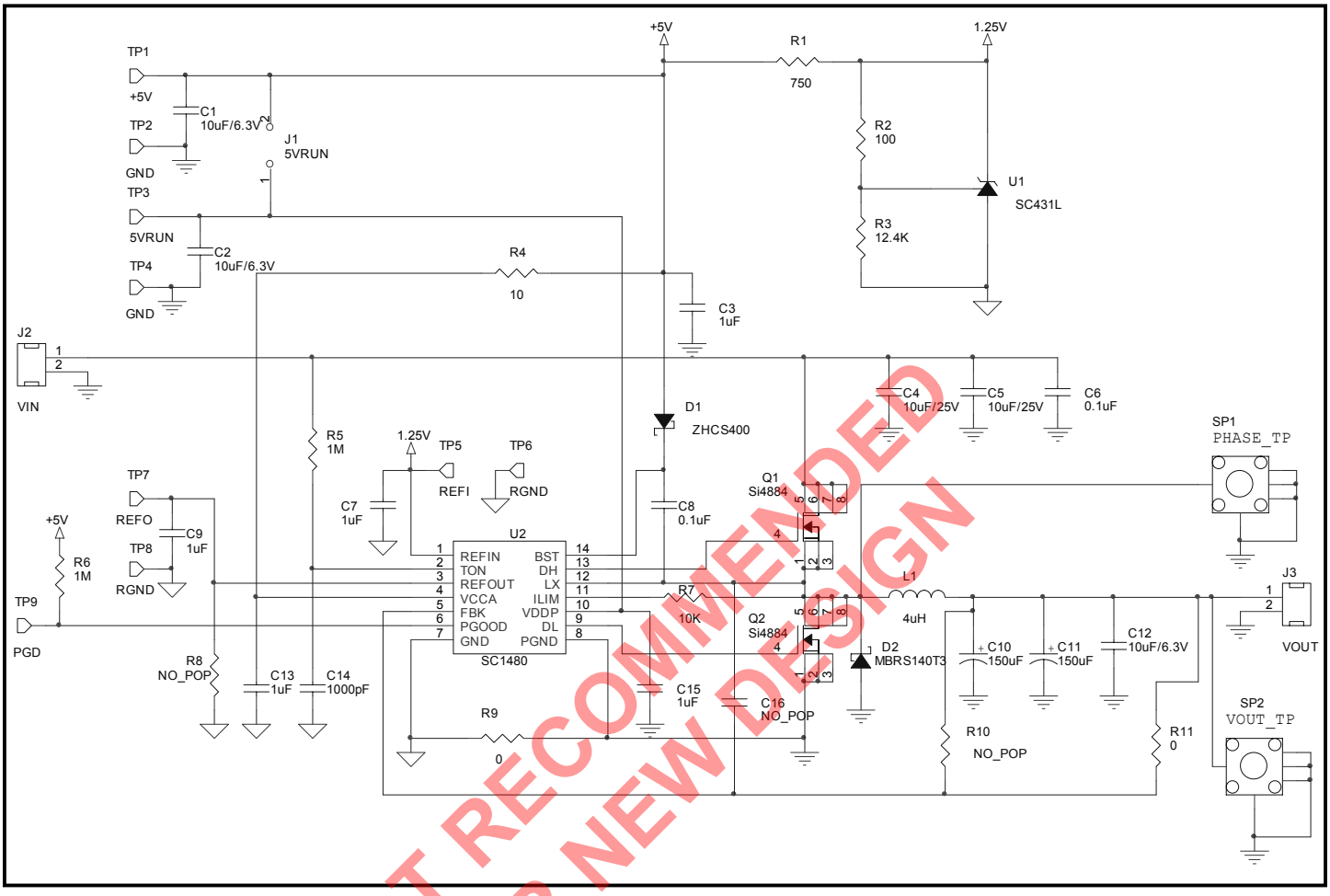
VIN = 4.5V - 25V
VOUT = 1.25V; IOUT = 3A

Reference Design - Bill of Material

Item	Quantity	Reference	Part	Vendor
1	1	C1	10uF/10V	
2	1	C2	10uF/25V	
3	3	C3,C4,C6	1uF	
4	1	C5	0.1uF	
5	1	C7	1000pF	
6	1	C8	0.01uF	
7	1	C9	150uF	
8	1	C10	10uF	
9	1	D1	ZHCS400	
10	1	L1	4.1uH	
11	1	Q1	Si4818DY	
12	2	R1, R3	20k	
13	2	R2, R5	1m	
14	1	R4	10	
15	1	R6	10k	
16	1	R7	No Pop	
17	1	U1	SC1480	

POWER MANAGEMENT

Evaluation Board Schematic

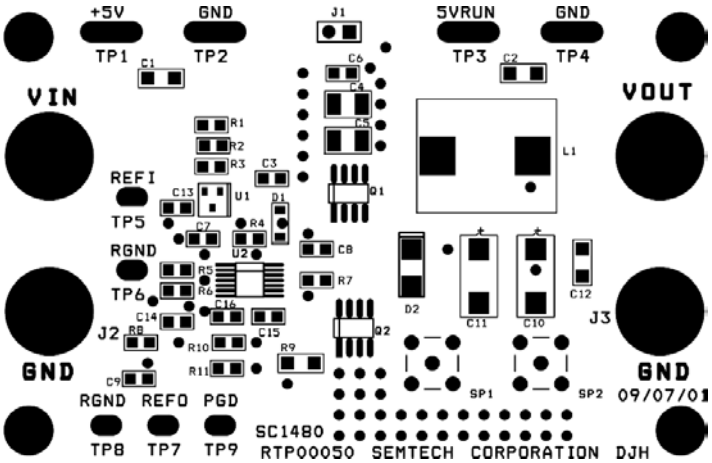


Evaluation Board - Bill of Materials

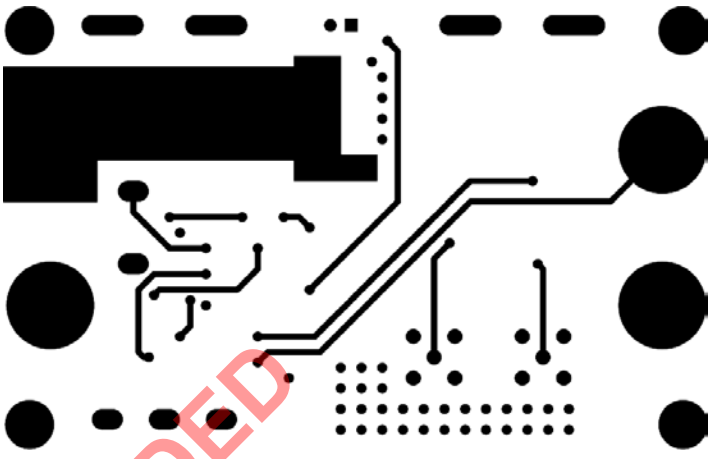
Item	Quantity	Reference	Part
1	3	C1,C2,C12	10uF/6.3V
2	5	C3,C7,C9,C13,C15	1uF
3	2	C4,C5	10uF/25V
4	2	C6,C8	0.1uF
5	2	C10,C11	150uF
6	1	C14	1000pF
7	3	R8,R10,C16	NO_POP
8	1	D1	ZHCS400
9	1	D2	MBRS140T3
10	1	J1	Header Post
11	2	J2,J3	Banana Jack
12	1	L1	4uH
13	2	Q1,Q2	Si4884
14	1	R1	750
15	1	R2	100
16	1	R3	12.4K
17	1	R4	10
18	2	R5,R6	1M
19	1	R7	10K
20	2	R9,R11	0
21	2	SP1,SP2	Probe test point
22	9	TP1 thru TP9	
23	1	U1	SC431L
24	1	U2	SC1480

Gerber Plots

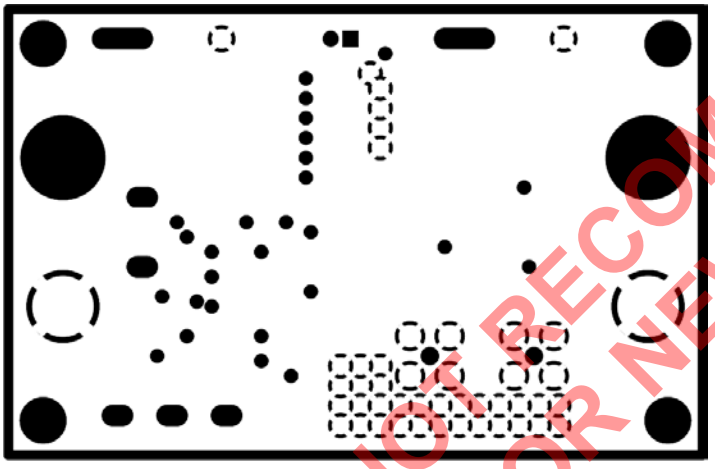
Silk Screen Layer



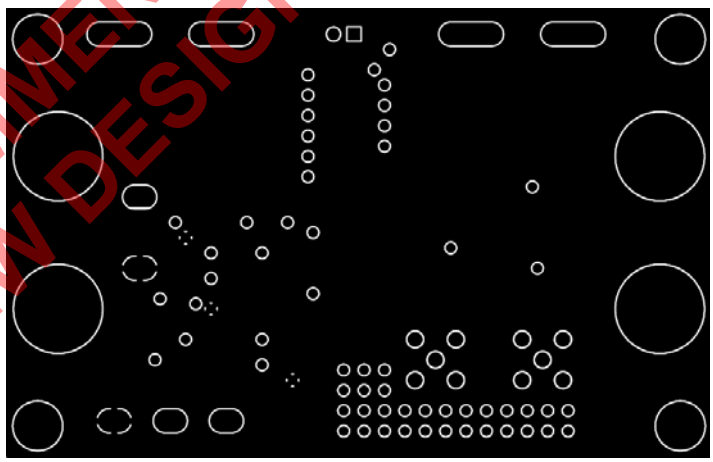
Bottom Layer



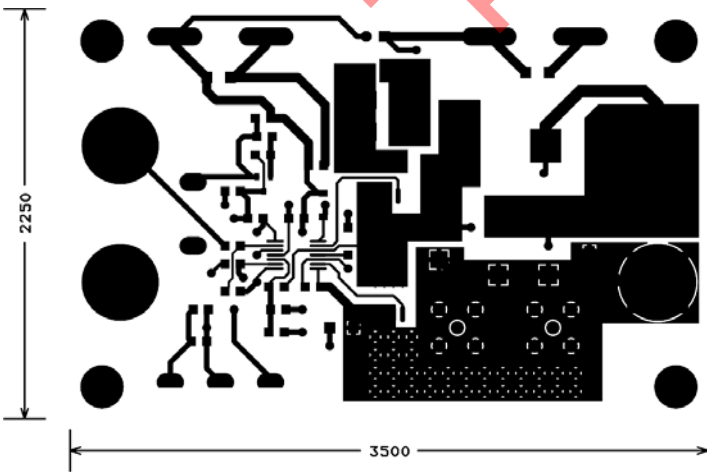
Power Ground Layer



Analog Ground Layer

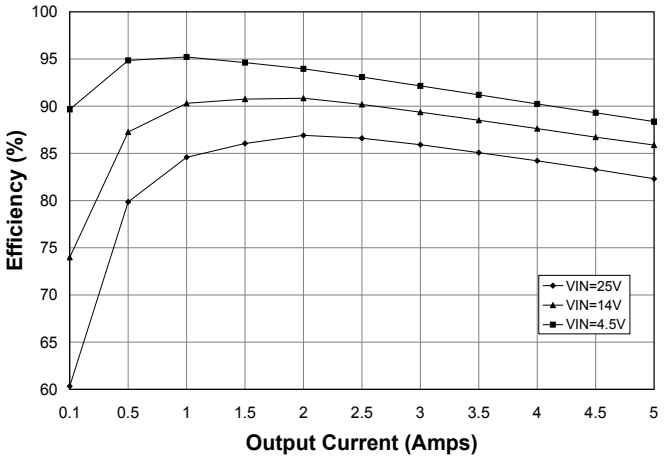


Top Layer

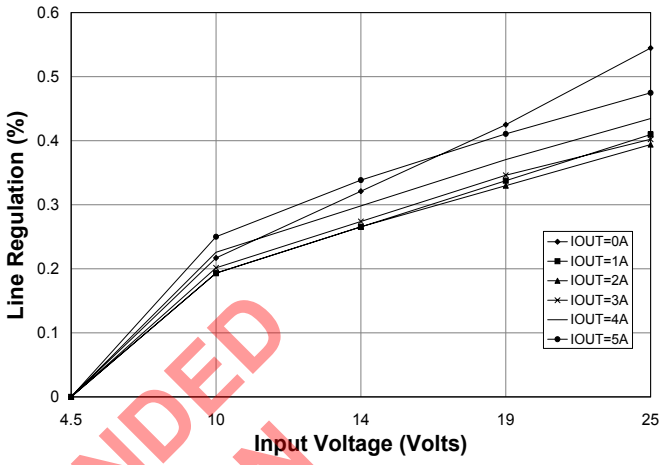


Typical Characteristic (Cont.)

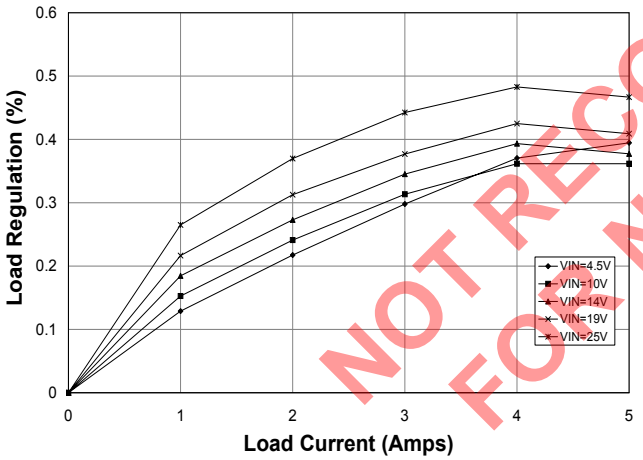
SC1480EVB Efficiency at V_{OUT} = 1.25V



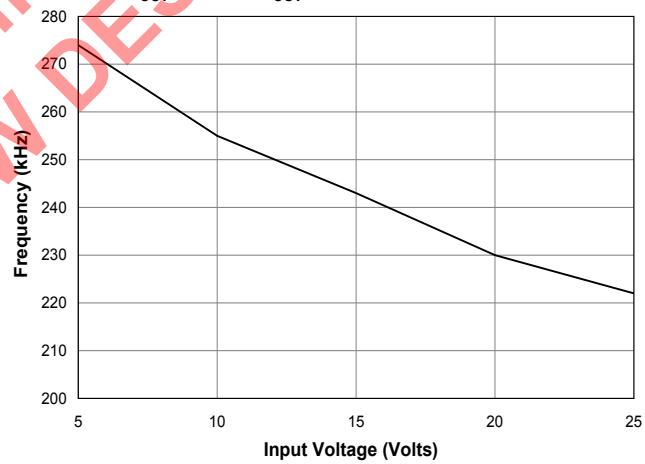
SC1480EVB Line Regulation at V_{OUT} = 1.25V



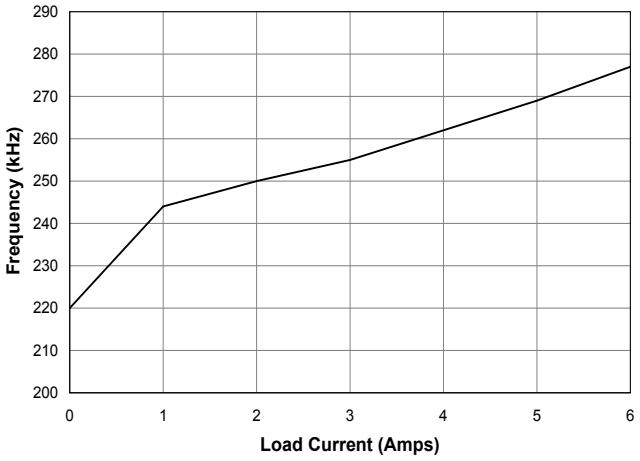
SC1480EVB Load Regulation at V_{OUT} = 1.25V



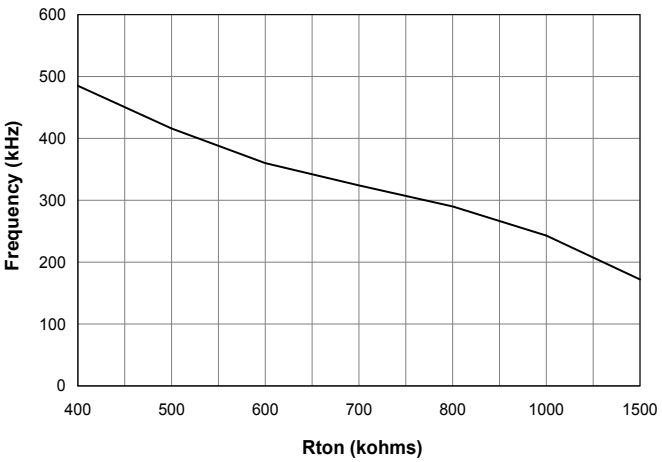
Frequency vs. Input Voltage (I_{OUT} = 1A, V_{OUT} = 1.25V, Rton = 1M)



Frequency vs. Load Current (V_{IN} = 15V, V_{OUT} = 1.25V, Rton = 1M)

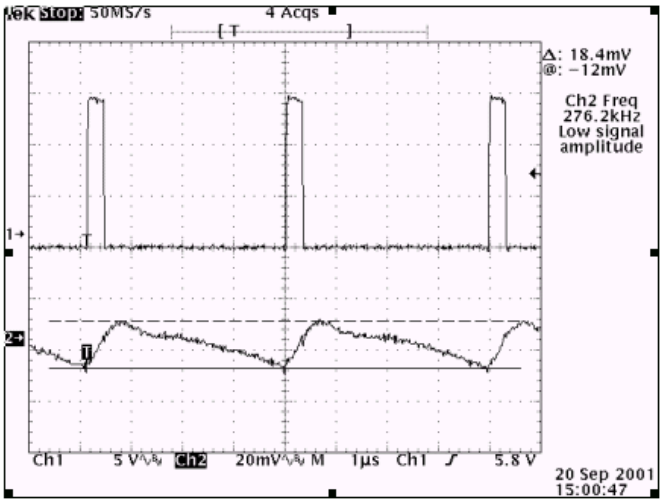


Rton vs. Frequency (V_{IN} = 15V, V_{OUT} = 1.25V, I_{OUT} = 1A)

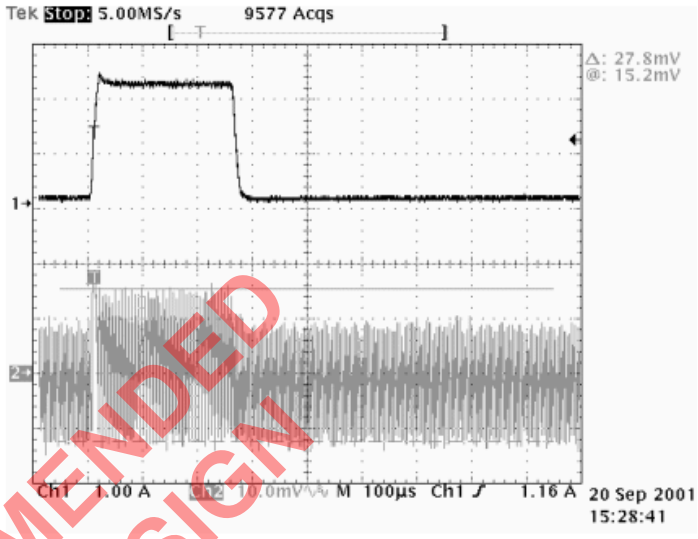


Typical Characteristic (Cont.)

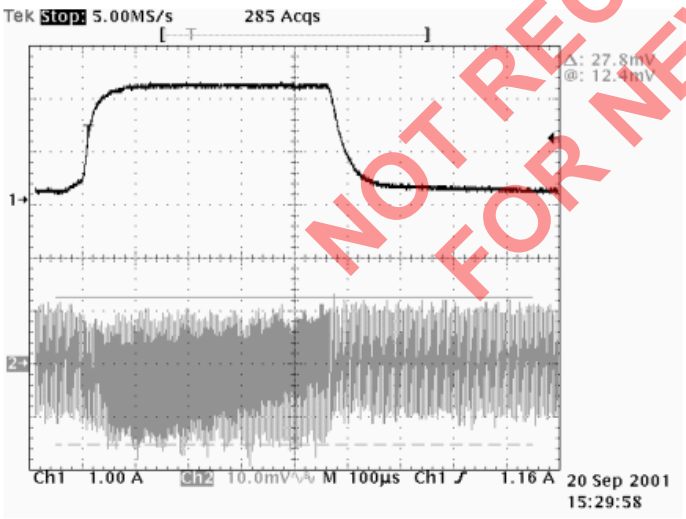
Upper Trace: Phase
Lower Trace: Output Ripple Voltage



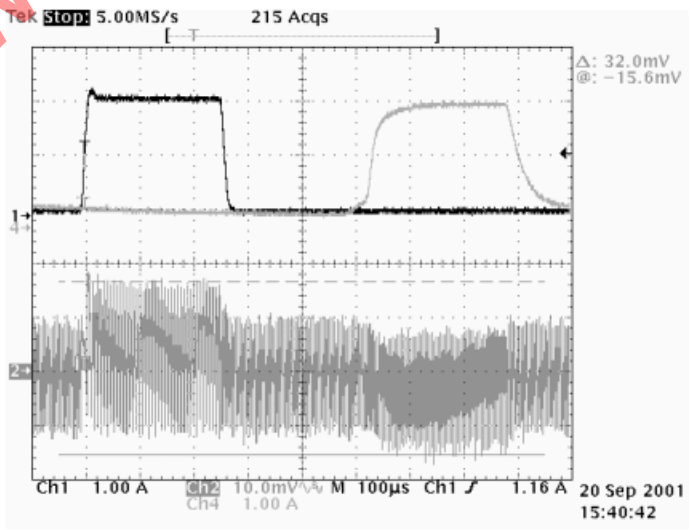
Upper Trace: 0A to +2A Transient
Lower Trace: Output Ripple Voltage



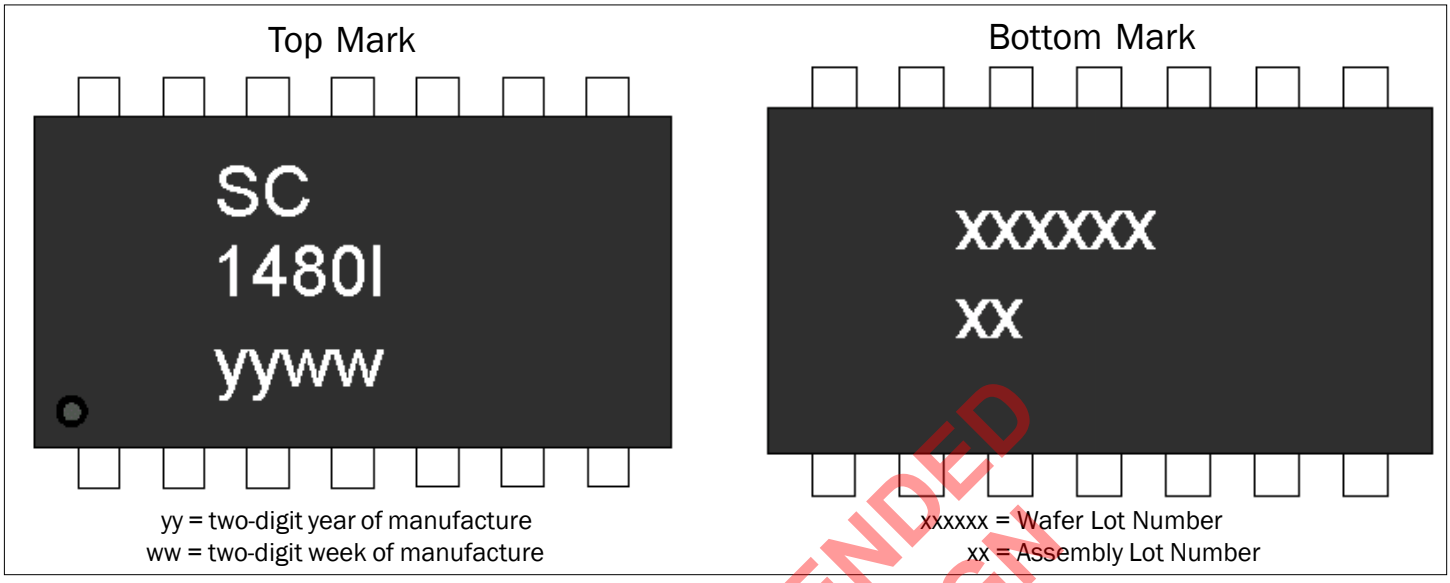
Upper Trace: 0A to -2A Load Transient
Lower Trace: Output Ripple Voltage



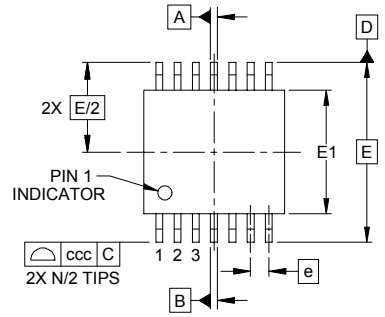
Upper Trace: 0A to +2A and 0A to -2A Transient
Lower Trace: Output Ripple Voltage



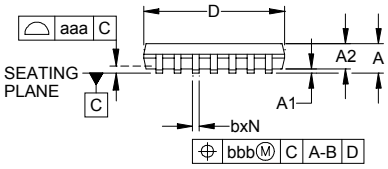
Marking Diagram

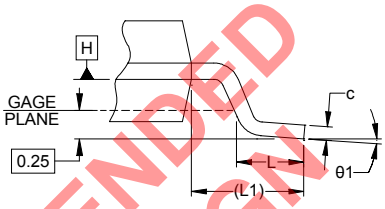


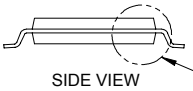
Outline Drawing - TSSOP-14



DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	.047	-	-	1.20
A1	.002	-	.006	0.05	-	0.15
A2	.031	-	.042	0.80	-	1.05
b	.007	-	.012	0.19	-	0.30
c	.003	-	.007	0.09	-	0.20
D	.193	.197	.201	4.90	5.00	5.10
E1	.169	.173	.177	4.30	4.40	4.50
E	.252 BSC			6.40 BSC		
e	.026 BSC			0.65 BSC		
L	.018	.024	.030	0.45	0.60	0.75
L1	(.039)			(1.0)		
N	14			14		
θ1	0°	-	8°	0°	-	8°
aaa	.004			0.10		
bbb	.004			0.10		
ccc	.008			0.20		



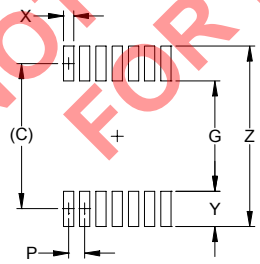




NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. REFERENCE JEDEC STD MO-153, VARIATION AB-1.

Land Pattern - TSSOP-14



DIM	INCHES	MILLIMETERS
C	(.222)	(5.65)
G	.161	4.10
P	.026	0.65
X	.016	0.40
Y	.061	1.55
Z	.283	7.20

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

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