RF2405

CDMA/FM LOW NOISE AMPLIFIER/MIXER

Typical Applications

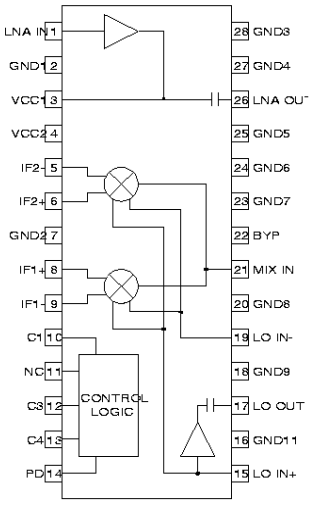
- CDMA/FM Cellular Systems
- Supports Dual-Mode AMPS/CDMA
- Supports Dual-Mode TACS/CDMA
- General Purpose Down Converter
- Commercial and Consumer Systems
- Portable Battery Powered Equipment

Product Description

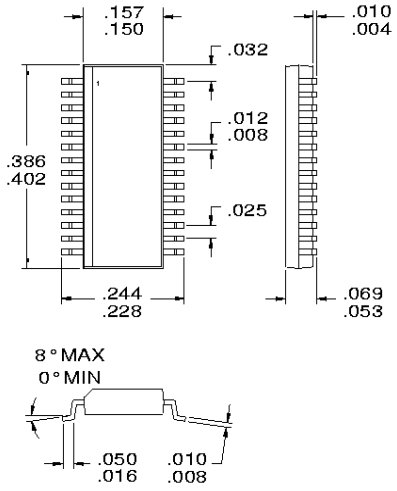
The RF2405 is a receiver front-end designed for the receive section of dual-mode CDMA/FM cellular applications. It is designed to amplify and down-convert RF signals and features IF output selection, LO buffer enable, power down mode, and low current "lazy" mode. The digitally selected "lazy" mode reduces current drain by approximately 10mA, putting the IC in a lower current drain, lower noise, lower IP3 state. This gives the receiver designer added flexibility to dynamically optimize these downconverter parameters. Noise Figure, IP3, and other specifications are designed to be compatible with the IS-95 Interim Standard for CDMA cellular communications. This circuit is designed as part of the RFMD CDMA Chip Set. The IC is manufactured on an advanced Silicon Bipolar process and packaged in a standard SSOP-28.

Optimum Technology Matching® Applied

☑ Si BJT ☐ GaAs HBT ☐ GaAs MESFET
☐ Si Bi-CMOS



Functional Block Diagram



Package Style: SSOP-28

Features

- Complete Receiver Front-End
- Single 2.7V to 4.0V Power Supply
- Low current-drain "Lazy" Mode
- Buffered LO Output
- Digitally Selectable IF Outputs
- 500MHz to 1100MHz Operation

Ordering Information

RF2405	CDMA/FM Low Noise Amplifier/Mixer
RF2405 PCBA	Fully Assembled Evaluation Board

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http://www.rfmd.com

Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.5 to +5.0	V_{DC}
Input LO and RF Levels	+6	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

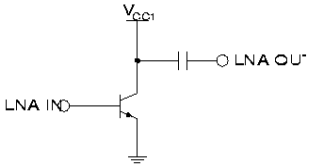
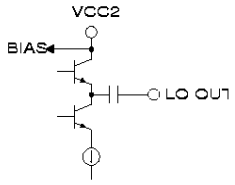
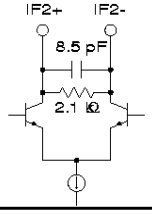
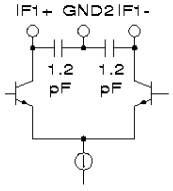
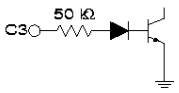
Caution! ESD sensitive device.

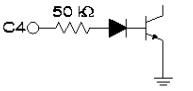
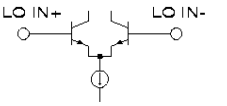
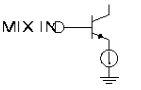
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T = 25 ° C, V_{CC}=3.0V, RF=881MHz, LO=966MHz @ 0dBm See Mode Control Logic Table
RF Frequency Range		500 to 1100		MHz	
LO Frequency Range		500 to 1100		MHz	
IF Frequency Range		0.1 to 250		MHz	
Power Supply					
Voltage		2.7 to 4.0		V	
Current Consumption		19		mA	FM
		23		mA	CDMA
		adds 4		mA	LO buffer ON
		subtracts 10		mA	"Lazy" Mode
		< 20		µA	Power Down
Max Dynamic Range Mode					
Cascaded Perform. to IF1					1kΩ balanced load, 3.0dB Image Filter Loss; CDMA
Cascade Conversion Gain		27.5		dB	
Cascade Input IP3 to IF1		-6		dBm	
Cascade Noise Figure		3.8		dB	
Cascaded Perform. to IF2					870Ω load, 3dB Image Filter Loss; FM
Cascade Conversion Gain		19		dB	
Cascade Input IP3		-6		dBm	
Cascade Noise Figure		3.8		dB	
First Section (LNA)					FM and CDMA
Gain		15.5		dB	
Noise Figure		2.1		dB	
Input IP3		+6		dBm	
Input P1dB		-11		dBm	
Reverse Isolation		25		dB	
Input VSWR		<3:1			Internally matched for optimum noise figure from 50Ω source
Output VSWR		<1.5:1			With external match (partial)
LO Input					
LO Input Range		-6 to 0		dBm	
LO Output Level		0		dBm	LO Buffer ON, 0dBm input
LO Output Level		-35		dBm	LO Buffer OFF, 0dBm input
LO IN to LNA Input Rejection		37		dB	
LO IN to IF1, IF2 Rejection		15		dB	
LO Input VSWR		<2:1			With external matching network

Second Section (Mixer, IF1 or IF2 Output)					
Conversion Gain		15		dB	IF 1, 1kΩ balanced load.
		7		dB	IF 2, 870Ω load.
Noise Figure		11.5		dB	Single sideband.
Input VSWR		<1.5:1			With external matching network
Input IP3 to IF1		+7		dBm	
Input IP3 to IF2		+7		dBm	
Input P1dB, IF2		-4		dBm	
Input P1dB, IF1		-8		dBm	
MIX IN to IF1, IF2 Rejection		35		dB	
IF1, IF2 Output Freq. Range		70 to 100		MHz	With external IF interface network
Output Impedance		>1		kΩ	IF1, balanced, open collector
		870		Ω	IF2, single ended, with external inductor.
"Lazy" Mode					
Cascaded Perform. to IF1					1kΩ balanced load, 3.0dB Image Filter Loss CDMA
Cascade Conversion Gain		25.2		dB	
Cascade Input IP3 to IF1		-10		dBm	
Cascade Noise Figure		3.4		dB	
Cascaded Perform. to IF2					870Ω load, 3dB Image Filter Loss. FM
Cascade Conversion Gain		17		dB	
Cascade Input IP3		-10		dBm	
Cascade Noise Figure		3.4		dB	
First Section (LNA)					FM and CDMA
Gain		14.5		dB	
Noise Figure		2.1		dB	
Input IP3		+2		dBm	
Input P1dB		-16		dBm	
Reverse Isolation		25		dB	
Input VSWR		<3:1			Internally matched for optimum noise figure from 50Ω source
Output VSWR		<1.5:1			With external match (partial)
Second Section (Mixer, IF1 or IF2 Output)					
Conversion Gain		13.7		dB	IF 1, 1kΩ balanced load.
		5.5		dB	IF 2, 870Ω load.
Noise Figure		9.5		dB	Single sideband.
Input VSWR		<1.5:1			With external matching network
Input IP3 to IF1		+2		dBm	
Input IP3 to IF2		+2		dBm	
Input P1dB, IF2		-9		dBm	
Input P1dB, IF1		-6		dBm	
MIX IN to IF1, IF2 Rejection		35		dB	
IF1, IF2 Output Freq. Range		70 to 100		MHz	With external IF interface network
Output Impedance		>1		kΩ	IF1, balanced, open collector
		870		Ω	IF2, single ended, with external inductor.
LO Input					
LO Input Range		-6 to 0		dBm	
LO Output Level		0		dBm	LO Buffer ON, 0dBm input
LO Output Level		-35		dBm	LO Buffer OFF, 0dBm input
LO IN to LNA Input Rejection		30		dB	
LO IN to IF1, IF2 Rejection		15		dB	
LO Input VSWR		<2:1			With external matching network

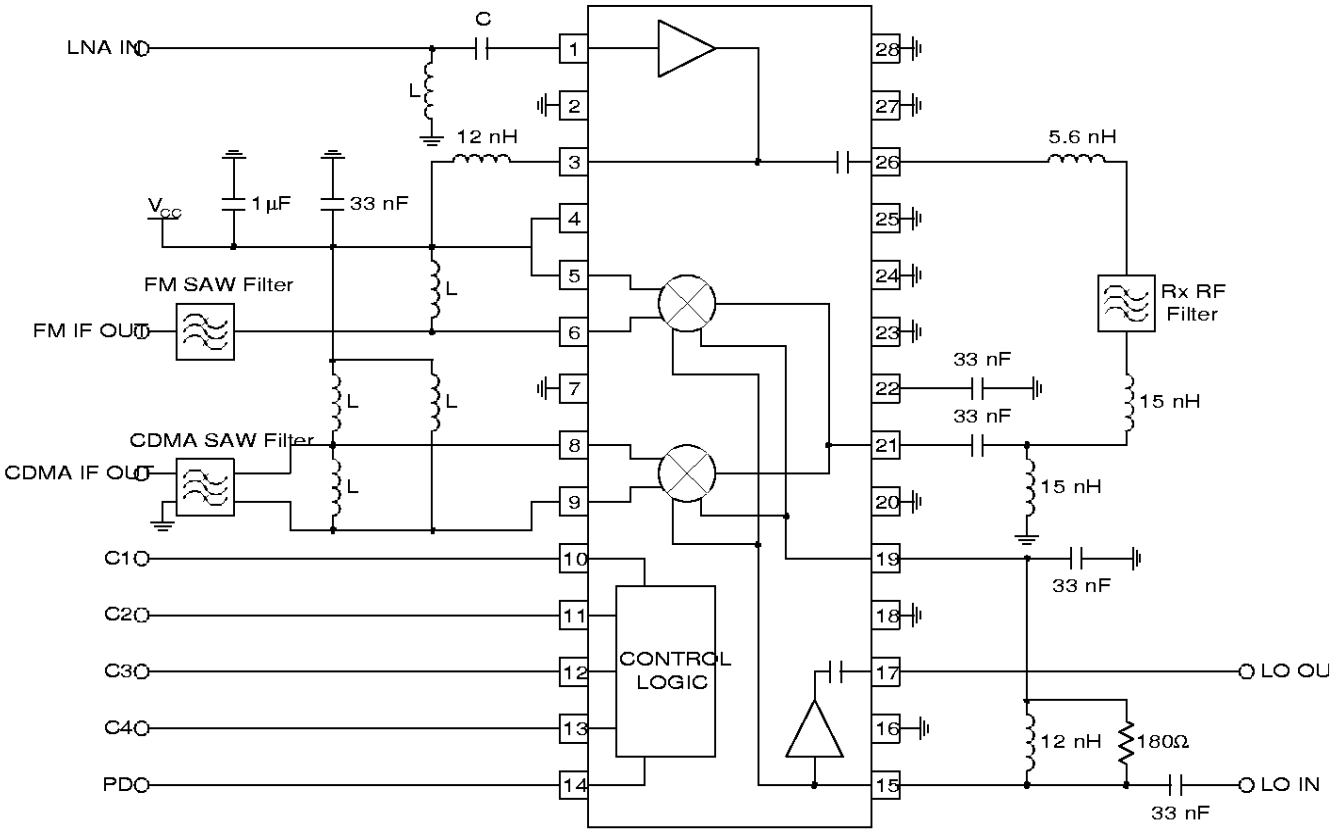
Mode Control Logic

MODE	C1	C3	C4	PD
FM (IF2)	L	X	H	H
CDMA (IF1)	H	X	H	H
Lazy FM (IF2)	L	X	L	H
Lazy CDMA (IF1)	H	X	L	H
LO Buffer ON	X	H	X	H
LO Buffer OFF	X	L	X	X
Power Down	L	X	X	L

Pin	Function	Description	Interface Schematic
1	LNA IN	RF Input pin. This pin is internally matched for optimum noise fgure from a 50Ω source. This pin is internally DC biased and, if connected to a device with DC present, should be DC blocked with a capacitor suitable for the frequency of operation.	
2	GND1	Ground connection for the LNA circuits. Keep traces physically short and connect immediately to ground plane for best performance.	
3	VCC1	Supply Voltage for the LNA. External inductance, ~12 nH, is required in addition to internal inductance to achieve optimum LNA performance. This extra inductance can be easily achieved with a thin microstrip line. The value of this inductance will change with the frequency of operation. RF and IF bypassing is required on the supply side of the inductance. The ground side of the bypass capacitors should connect immediately to ground plane.	See pin 1.
4	VCC2	Supply Voltage for the LO buffer amplifier, bias circuits, and control logic. External RF and IF bypassing is required. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane.	
5	IF2-	Same as pin 6, except complementary output. For typical single ended operation, this pin is connected directly to V_{CC}.	See pin 6.
6	IF2+	FM IF Output pin. This is a balanced output, but is typically used as a single-ended output. The internal circuitry, in conjunction with an external matching/bias inductor to V_{CC}, sets the operating impedance. This inductor is typically incorporated in the matching network between the output and IF filter. The net output impedance, including the external inductor, is about 870Ω at 85MHz. Because this pin is biased to V_{CC}, a DC blocking capacitor must be used if the IF filter input has a DC path to ground. See Application Schematic.	
7	GND2	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
8	IF 1+	CDMA IF Output pin. This is a balanced output. The internal circuitry, in conjunction with an external matching/bias inductor to V_{CC}, sets the operating impedance. This inductor is typically incorporated in the matching network between the output and IF filter. The net output impedance, including the external inductor, at 85MHz is higher than 1kΩ, even though the part is designed to drive a 1kΩ load. Because this pin is biased to V_{CC}, a DC blocking capacitor must be used if the IF filter input has a DC path to ground. See Application Schematic.	
9	IF 1-	Same as pin 8, except complementary output.	See pin 8.
10	C1	Control line for IF select. See specification table for details. The threshold voltage is 1.6V, and the pin draws less than 50μA when selected.	
11	NC	No connection.	
12	C3	Enable pin for the LO output buffer amplifier. This is a digitally controlled input. A logic "high" turns the buffer amplifier on, and the current consumption increases by 4mA (with 0dBm LO input). A logic "low" turns the buffer amplifier off. The threshold voltage is approximately 1.6V.	

13	C4	Enable pin for "Lazy Mode". This is a digitally controlled input. A logic "high" maintains the part in full performance mode. A logic "low" places the part in a reduced-current/reduced performance mode. See the specification table for details. The threshold voltage is 1.6V, and the pin draws less than 50μA when selected.	
14	PD	Power down pin. A logic "low" turns the part off. A logic "high" (>1.6V) turns the part on. In addition, pin 10 (C1) should also be taken low during power down.	
15	LO IN+	Mixer LO Balanced Input Pin. For single-ended input operation, this pin is used as an input and pin 18 is bypassed to ground.	
16	GND11	Ground connection for LO buffer amplifier. Keep traces physically short and connect immediately to ground plane for best performance.	
17	LO OUT	Optional Buffered LO Output. This pin is internally DC blocked and matched to 50Ω. The buffer amplifier is switched on or off by the voltage level at pin 12.	See pin 4.
18	GND9	Die flag ground. Keep traces physically short and connect immediately to ground plane for best performance.	
19	LO IN-	Mixer LO bypass.	See pin 15.
20	GND8	Ground connection for the mixer. Keep traces physically short and connect immediately to ground plane for best performance.	
21	MIX IN	Mixer RF Input Pin. This pin is internally DC biased and should be DC blocked if connected to a device with DC present. External matching network sets RF and IF impedance for optimum performance.	
22	BYP	Internal voltage reference. External RF and IF bypassing is required. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane.	
23	GND7	Same as pin 2.	
24	GND6	Same as pin 2.	
25	GND5	Same as pin 2.	
26	LNA OUT	LNA Output pin. This pin is internally DC blocked and externally matched to 50Ω at pin 3 in order to facilitate an easy interface to a 50Ω Image Filter.	See pin 1.
27	GND4	Same as pin 25.	
28	GND3	Same as pin 25.	

Application Schematic



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FRONT-ENDS