P54/74FCT3480B/C-P54/74FCT3481B/C
3.3V SSOP (QSOP) NOTEBOOK LOGIC
3.3V DUAL ODD-PARITY, DUAL EVEN-PARITY GENERATOR/CHECKERS

ADVANCE INFORMATION

FEATURES

- Function and Drive Compatible with the Fastest TTL Logic
- Inputs and Outputs Interface with TTL Logic Levels
- 3.3V ± 10% Power Supply and CMOS for Lowest Power Dissipation
- FCT3-B speed at 5.6ns max. (Com'l)
  FCT3-C speed at 4.8ns max. (Com'l)
- Edge-rate Control Circuitry for Significantly Improved Noise Characteristics
- ESD protection exceeds 2000V
- 48 mA Sink Current (Com'l), 32 mA (Mil)
  15mA Source Current (Com'l), 12 mA (Mil)
- QSOP (SSOP150) package for minimum board space requirements
- Input Clamp Diodes to Limit Bus Reflections
- Two 8-Bit Parity Generator/Checkers Per Device
- Open Drain Low-Active Parity Error Widths
- Expandable for Larger Word Widths
- Manufactured in 0.4 micron PACE Technology™

DESCRIPTION

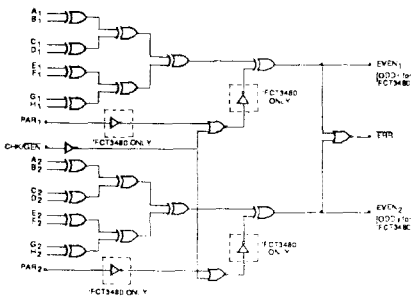
The 'FCT3480 and 'FCT3481 are high speed dual 8-bit parity generator/checkers. Each parity generator/checker accepts eight data bits and one parity bit as inputs, and generates a parity and a parity error output. The 'FCT3480 generates and checks odd parity, while the 'FCT481 generates and checks even parity. In the CHECK mode, the parity output for each generator in the 'FCT3480 ('FCT3481) is low whenever an odd (even) number of inputs is high; the common parity error output in the 'FCT3480 or the 'FCT3481 is low, indicating an error, if either of the generated parity outputs is high. In the GENERATE mode, the two input parity bits are disabled and each device functions as in the CHECK mode.

The parity error output is open-drain, designed for easy expansion of the word width by a simple wired-OR connection of several 'FCT3480 and 'FCT3481 type devices. Since additional logic is not needed, the parity generation and checking times remain the same as for each 'FCT480 device.

The 'FCT3480 and 'FCT3481 are manufactured using PACE II Technology™ which is Performance Advanced CMOS Engineered to use 0.4 micron effective channel lengths giving 250 picoseconds loaded* internal gate delays. The nominal supply voltage is reduced from the conventional 5.0V to 3.3V, thus reducing output swings dramatically.

*For a fan-in/fan-out of 4, at 85°C junction temperature and 3.3V.

FUNCTIONAL BLOCK DIAGRAM



NOTE: Functional description only.
Not representative of propagation delays.

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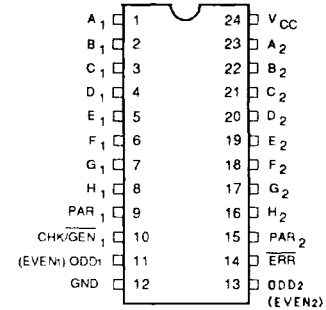
PIN CONFIGURATIONS



QSOP (SSOP150)

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