

SRAM

64K x 4 SRAM

FAST SRAM

FEATURES

- High speed: 15, 20, 25, 30, 35 and 45ns
- High-performance, low-power, CMOS double-metal process
- Single +5V $\pm 10\%$ power supply
- Easy memory expansion with $\overline{CE}$ option
- All inputs and outputs are TTL compatible

OPTIONS

- Timing
 - 15ns access
 - 20ns access
 - 25ns access
 - 30ns access
 - 35ns access
 - 45ns access

MARKING

-15
-20
-25
-30
-35
-45

- Packages

Plastic DIP (300 mil)	None
Plastic SOJ (300 mil)	DJ
Plastic SOIC (300 mil)	SG

 Available in ceramic packages tested to meet military specifications. Please refer to Micron's *Military Data Book*.

- 2V data retention L

- Temperature

Industrial	(-40°C to +85°C)	IT
Automotive	(-40°C to +125°C)	AT
Extended	(-55°C to +125°C)	XT

GENERAL DESCRIPTION

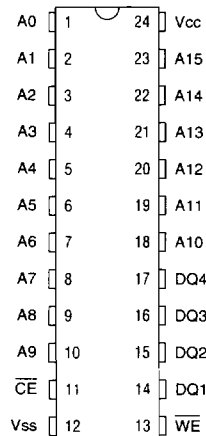
The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) on all organizations. This enhancement can place the outputs in High-Z for additional flexibility in system design.

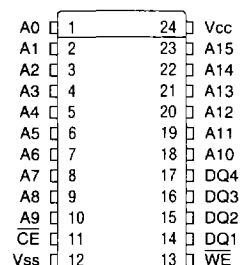
Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes to LOW. The device offers a reduced power standby mode

PIN ASSIGNMENT (Top View)

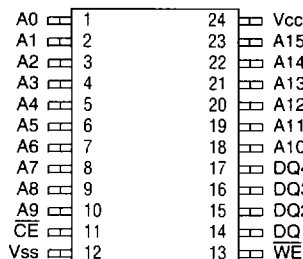
24-Pin DIP (A-7)



24-Pin SOJ (E-4)



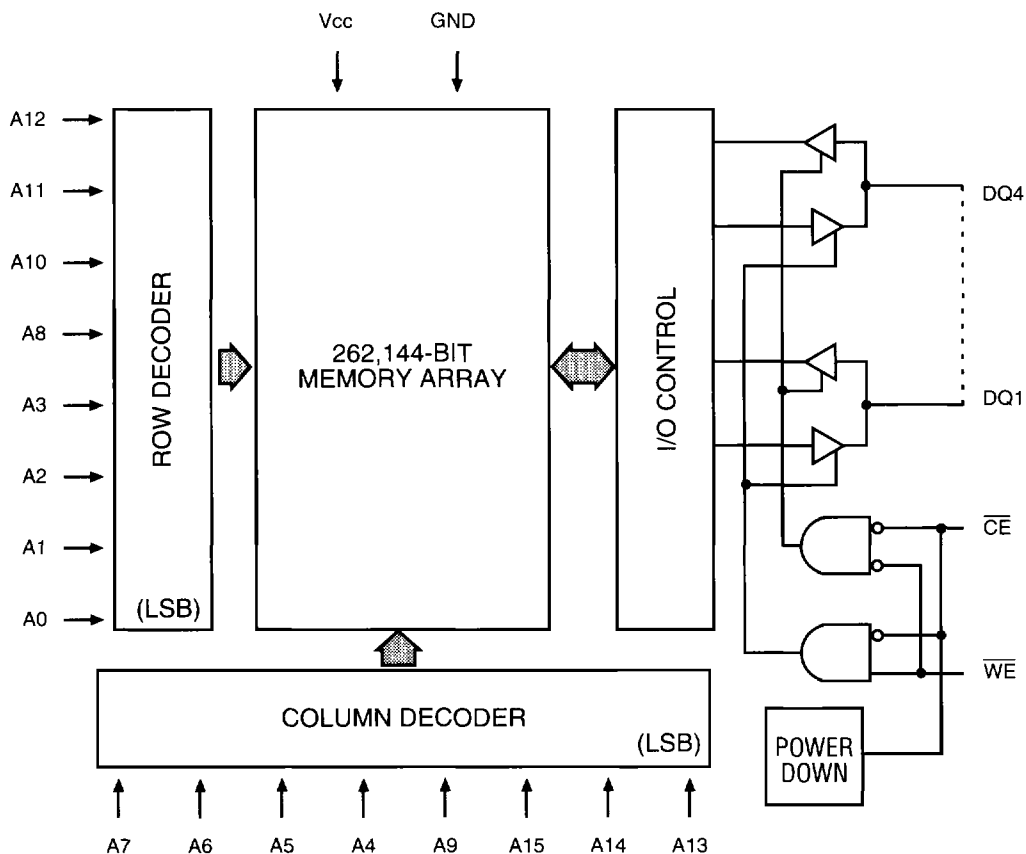
24-Pin SOIC (F-1)



when disabled. This allows system designers to achieve their low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	H	X	HIGH-Z	STANDBY
READ	L	H	Q	ACTIVE
WRITE	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS}-1V to +7V
Storage Temperature (Plastic)-55°C to +150°C
Power Dissipation1W
Short Circuit Output Current50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V _{IH}	2.2	V _{CC} +1	V	1
Input Low (Logic 0) Voltage		V _{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V _{IN} ≤ V _{CC}	I _{LI}	-5	5	μA	
Output Leakage Current	Output(s) Disabled 0V ≤ V _{OUT} ≤ V _{CC}	I _{LO}	-5	5	μA	
Output High Voltage	I _{OH} = -4.0mA	V _{OH}	2.4		V	1
Output Low Voltage	I _{OL} = 8.0mA	V _{OL}		0.4	V	1

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX						UNITS	NOTES
				-15	-20	-25	-30	-35	-45		
Power Supply Current: Operating	$\overline{CE} \leq V_{IL}$; V _{CC} = MAX f = MAX = 1/1RC Outputs Open	I _{CC}	75	140	120	110	95	90	90	mA	3, 14
Power Supply Current: Standby	$\overline{CE} \geq V_{IH}$; V _{CC} = MAX f = MAX = 1/1RC Outputs Open	I _{SB1}	11	30	30	25	25	25	25	mA	14
	$\overline{CE} \geq V_{CC} - 0.2V$; V _{CC} = MAX V _{IL} ≤ V _{SS} +0.2V V _{IH} ≥ V _{CC} -0.2V; f = 0	I _{SB2}	.04	5	5	5	5	7	7	mA	14

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T _A = 25°C, f = 1 MHz V _{CC} = 5V	C _I	6	pF	4
Output Capacitance		C _O	5	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

 (Note 5, 13) ($0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$; $V_{CC} = 5V \pm 10\%$)

DESCRIPTION		-15		-20		-25		-30		-35		-45			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle															
READ cycle time	^t RC	15		20		25		30		35		45		ns	
Address access time	^t AA		15		20		25		30		35		45	ns	
Chip Enable access time	^t ACE		15		20		25		30		35		45	ns	
Output hold from address change	^t OH	3		3		5		5		5		5		ns	
Chip Enable to output in Low-Z	^t LZCE	4		6		6		6		6		6		ns	
Chip disable to output in High-Z	^t HZCE		8		9		9		12		15		18	ns	6, 7
Chip Enable to power-up time	^t PU	0		0		0		0		0		0		ns	
Chip disable to power-down time	^t PD		15		20		25		30		35		45	ns	
WRITE Cycle															
WRITE cycle time	^t WC	15		20		20		25		30		35		ns	
Chip Enable to end of write	^t CW	10		15		15		18		20		25		ns	
Address valid to end of write	^t AW	10		15		15		18		20		25		ns	
Address setup time	^t AS	0		0		0		0		0		0		ns	
Address hold from end of write	^t AH	0		0		0		0		0		0		ns	
WRITE pulse width	^t WP1	10		15		15		18		20		25		ns	
WRITE pulse width	^t WP2	12		15		15		18		20		25		ns	
Data setup time	^t DS	10		10		10		12		15		20		ns	
Data hold time	^t DH	0		0		0		0		0		0		ns	
Write disable to output in Low-Z	^t LZWE	4		5		5		5		5		5		ns	
Write Enable to output in High-Z	^t HZWE		7		10		10		12		15		18	ns	6

AC TEST CONDITIONS

Input pulse levels	V _{SS} to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

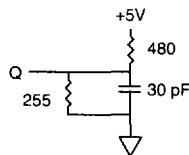


Fig. 1 OUTPUT LOAD EQUIVALENT

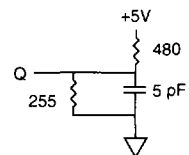


Fig. 2 OUTPUT LOAD EQUIVALENT

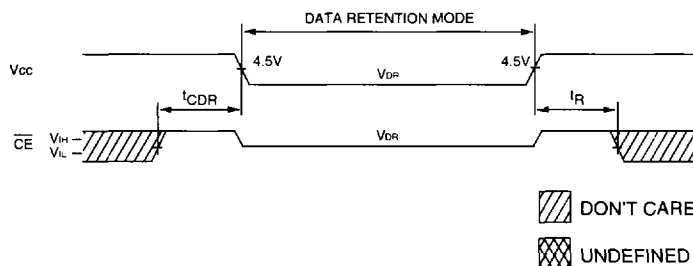
NOTES

1. All voltages referenced to V_{SS} (GND).
2. -3V for pulse width < 20ns.
3. I_{CC} is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^tHZCE and ^tHZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.
7. At any given temperature and voltage condition, ^tHZCE is less than ^tLZCE and ^tHZWE is less than ^tLZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to or coincident with latest occurring chip enable.
11. ^tRC = Read Cycle Time.
12. Chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) can initiate and terminate a WRITE cycle.
13. For automotive, industrial and extended temperature specifications, refer to page 1-175.
14. Typical values are measured at 5V, 25°C and 20ns cycle time.

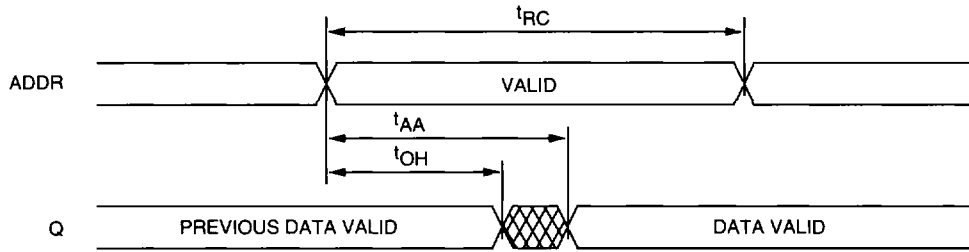
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V _{CC} for Retention Data		V _{DR}	2		—	V	
Data Retention Current	$\overline{CE} \geq (V_{CC} - 0.2V)$ $V_{IN} \geq (V_{CC} - 0.2V)$ or $\leq 0.2V$	V _{CC} = 2V	I _{CCDR}	95	300	μA	
		V _{CC} = 3V		350	400	μA	
Chip Deselect to Data Retention Time		^t CDR	0		—	ns	4
Operation Recovery Time		^t R	^t RC			ns	4, 10

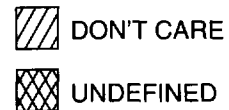
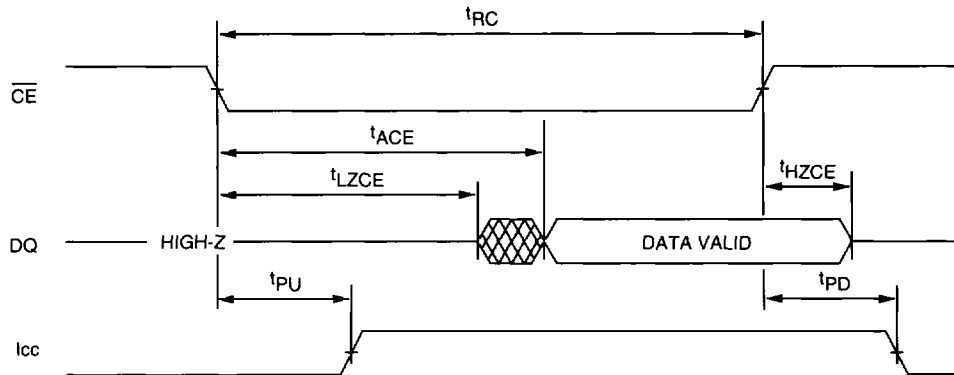
LOW V_{CC} DATA RETENTION WAVEFORM



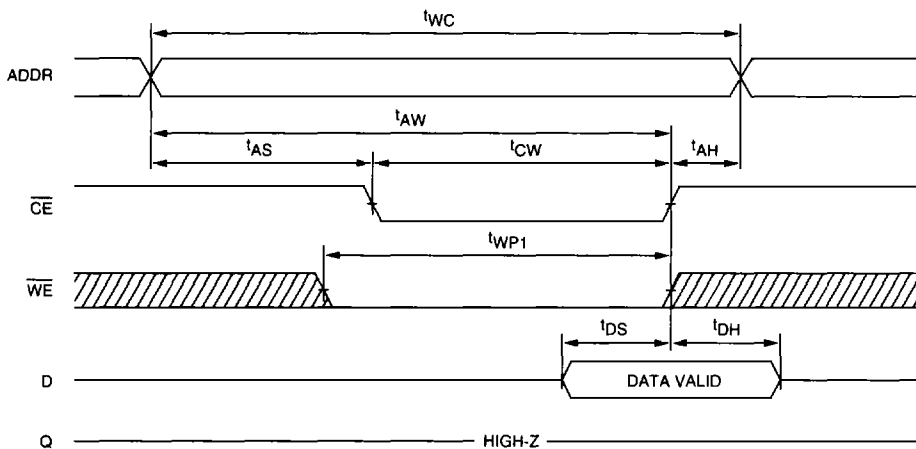
READ CYCLE NO. 1 8, 9



READ CYCLE NO. 2 7, 8, 10



WRITE CYCLE NO. 1
(Chip Enable Controlled)



WRITE CYCLE NO. 2
(Write Enable Controlled) 7, 12

