256K × 16 Bit CMOS Dynamic RAM with Extended Data Out

FEATURES

- **Performance range:**

	tRAC	tCAC	tRC	tHPC
KM416C254B/BL/BLL-5	50ns	17ns	90ns	20ns
KM416C254B/BL/BLL-6	60ns	17ns	110ns	24ns
KM416C254B/BL/BLL-7	70ns	20ns	130ns	29ns

- **Fast Page Mode with Extended Data Out**
- **Byte word Read/Write operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **Self Refresh operation (LL-ver)**
- **TTL compatible inputs and outputs**
- **Early write or output enable controlled write**
- **Triple +5V±10% power supply**
- **Refresh Cycle**
  - **-512 cycle/8ms (Normal)**
  - **-512 cycle/64ms (L-version)**
  - **-512 cycle/128ms (LL-version)**
- **Power Dissipation**
  - **-Standby : 5.5mW(Normal)**
  - **1.1mW(L-version)**
  - **0.83mW(LL-version)**
  - **-Active (50/60/70): 605/495/440 mW**
- **JEDEC standard pinout**
- **Available in plastic SOJ and TSOP II**

GENERAL DESCRIPTION

The Samsung KM416C254B/BL/BLL is a CMOS high speed 262,144 bit × 16 Dynamic Random Access Memory. Its design is optimized for high performance applications such as personal computer, graphics and high performance portable computers.

The KM416C254B/BL/BLL features EDO Mode operation which allows high speed random access of memory cells within the same row. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

The KM416C254B/BL/BLL is fabricated using Samsung's advanced CMOS process.

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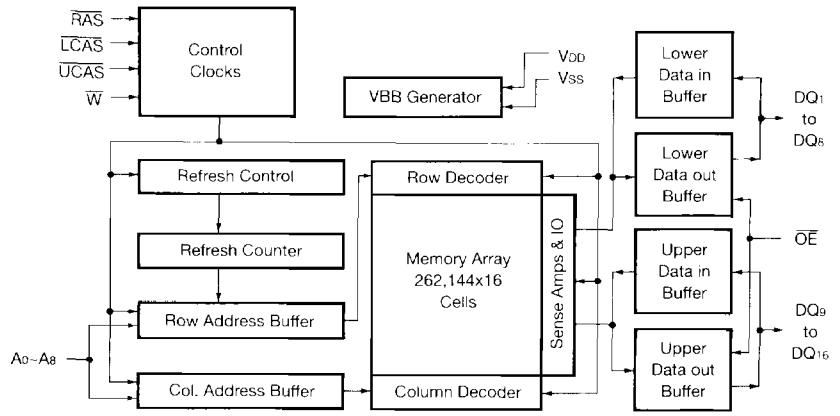
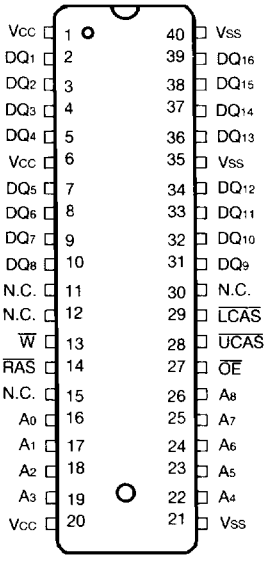
FUNCTIONAL BLOCK DIAGRAM

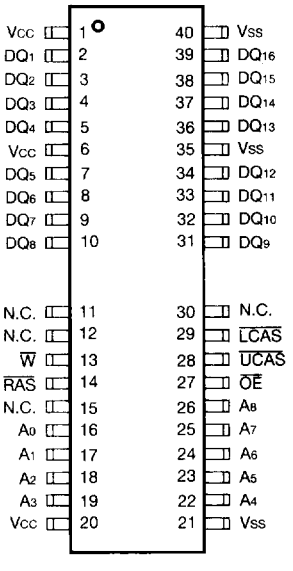


PIN CONFIGURATION (Top Views)

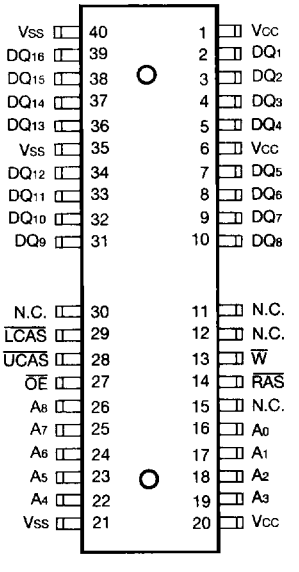
• KM416C254BJ/BLJ/BLLJ



• KM416C254BT/BLT/BLLT



• KM416C254BTR/BLTR/BLLTR



Pin Name	Pin Function
A0-A8	Address Inputs
DQ1~16	Data In/Out
VSS	Ground
RAS	Row Address Strobe
UCAS	Upper Column Address Strobe
LCAS	Lower Column Address Strobe
W	Read/Write Input
OE	Data Output Enable
VCC	Power(+5V)
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-1~+7.0	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-1~+7.0	V
Storage Temperature	T_{stg}	-55 to + 150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	V_{CC}+1	V
Input Low Voltage	V_{IL}	-1.0	-	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$, $\overline{CAS}$, Address Cycling @ t_{RC}=min.)	KM416C254B/BL/BLL-5	I_{CC1}	-	110	mA
	KM416C254B/BL/BLL-6			90	mA
	KM416C254B/BL/BLL-7			80	mA
Standby Current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=$\overline{W}$=V_{IH})		I_{CC2}	-	2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{UCAS}$=$\overline{LCAS}$=V_{IH}, $\overline{RAS}$, Address Cycling @ t_{RC}=min.)	KM416C254B/BL/BLL-5	I_{CC3}	-	110	mA
	KM416C254B/BL/BLL-6			90	mA
	KM416C254B/BL/BLL-7			80	mA
Hyper page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{UCAS}$=$\overline{LCAS}$, Address Cycling @ t_{PC}=min.)	KM416C254B/BL/BLL-5	I_{CC4}	-	70	mA
	KM416C254B/BL/BLL-6			60	mA
	KM416C254B/BL/BLL-7			55	mA
Standby Current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=$\overline{W}$=V_{CC}-0.2V)	KM416C254B	I_{CC5}	-	1	mA
	KM416C254BL			200	μA
	KM416C254BLL			150	μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{UCAS}$=$\overline{LCAS}$ Cycling @ t_{RC}=min.)	KM416C254B/BL/BLL-5	I_{CC6}	-	110	mA
	KM416C254B/BL/BLL-6			90	mA
	KM416C254B/BL/BLL-7			80	mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage(V_{IH})=V_{CC}-0.2V Input Low Voltage(V_{IL})=0.2V $\overline{UCAS}$=$\overline{LCAS}$= 0.2V D_{IN}=Don't Care, T_{RC}=125μS T_{RAS}=T_{RAS} min.~300ns	KM416C254BL	I_{CC7}	-	300	μA
Self Refresh Current $\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=0.2V $\overline{W}$=$\overline{OE}$=A_0-A_8=V_{CC}-0.2V or 0.2V DQ_1-DQ_{16}=V_{CC}-0.2V, 0.2V or Open	KM416C254BLL	I_{CC8}	-	200	μA

DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any input $0 < V_{IN} < V_{CC}+0.5V$, all other pins not under test=0 volts.)	$I_{I(L)}$	-10	10	μA
Output Leakage Current (Data out is disabled, $0V < V_{OUT} < V_{CC}$)	$I_{O(L)}$	-10	10	μA
Output High Voltage Level (I_{OH}=-5mA)	V_{OH}	2.4	-	V
Output Low Voltage Level (I_{OL}=4.2mA)	V_{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum two times while RAS=V_{IL}. In I_{CC4}, address can be changed maximum once within one hyper page cycle.

CAPACITANCE (T_A=25°C, V_{CC}=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0~A_8)	C_{IN1}	-	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	-	7	pF
Input Capacitance (DQ_1~DQ_{16})	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C < T_A < 70°C, V_{CC}=5V ± 10%, See notes 1,2)

Test condition : V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.0/0.8V, Output loading C_L=100pF

Parameter	Symbol	-5(*)		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	90		110		130		ns	
Read-modify-write cycle time	t_{RWC}	135		155		185		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60		70	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		17		17		20	ns	3,4,5
Access time from column address	t_{AA}		25		30		35	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	3		3		3		ns	3
Turn-off delay from $\overline{CAS}$	t_{CEZ}	3	13	3	15	3	20	ns	7,14
Transition time (rise and fall)	t_T	2	50	2	50	2	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		50		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10,000	60	10,000	70	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	17		17		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	40		50		60		ns	
$\overline{CAS}$ pulse width	t_{CAS}	8	10,000	10	10,000	15	10,000	ns	12
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	37	20	45	20	50	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	30	15	35	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		ns	

(*) -50ns Product : Output Loading (C_L)=50pF, V_{CC}=5V ± 5%

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5(*)		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Column address set-up time	tASC	0		0		0		ns	
Column address hold time	tCAH	8		10		15		ns	
Column address hold time referenced to $\overline{RAS}$	tAR	40		45		55		ns	6
Column address to $\overline{RAS}$ lead time	tRAL	25		30		35		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		ns	9
Write command hold time	tWCH	10		10		10		ns	
Write command hold time referenced to $\overline{RAS}$	tWCR	40		45		50		ns	6
Write command pulse width	tWP	10		10		10		ns	
Write command to $\overline{RAS}$ lead time	tRWL	13		15		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	8		10		15		ns	
Data set-up time	tDS	0		0		0		ns	10
Data hold time	tDH	10		10		15		ns	10
Data hold time referenced to $\overline{RAS}$	tDHR	40		45		55		ns	6
Refresh period (Normal)	tREF		8		8		8	ms	
Refresh period (L-version)	tREF		64		64		64	ms	
Refresh Period(LL-version)	tREF		128		128		128	ms	
Write command set-up time	tWCS	0		0		0		ns	8
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	40		42		50		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	73		85		95		ns	8
Column address to $\overline{W}$ delay time	tAWD	48		55		60		ns	8
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	53		60		65		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	tCPT	20		20		25		ns	
Access time from $\overline{CAS}$ precharge	tCPA		30		35		40	ns	3
Hyper Page mode cycle time	tHPC	20		24		29		ns	12
Hyper Page mode read-modity-write cycle time	tHPRWC	62		71		81		ns	12
$\overline{CAS}$ precharge time (Hyper Page mode)	tCP	8		10		10		ns	
$\overline{RAS}$ pulse width (Hyper Page mode)	tRASP	50	100K	60	100K	70	100K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	30		35		40		ns	
$\overline{OE}$ access time	tOEA		15		15		20	ns	
$\overline{OE}$ to Output in Low-z	tOLZ	3		3		3		ns	
$\overline{OE}$ to data delay	tOED	13		15		20		ns	
Output buffer turn off delay time from $\overline{OE}$	tOEZ	3	13	3	15	3	20	ns	7

(*) -50ns Product : Output Loading (C_L)=50pF, V_{CC}=5V ± 5%

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5(*)		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
$\overline{OE}$ commend hold time	tOEH	13		15		20		ns	
Output data hold time	tDOH	5		5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	tREZ	3	13	3	15	3	20	ns	7,14
Output buffer turn off delay from $\overline{W}$	tWEZ	3	13	3	15	3	20	ns	7
$\overline{W}$ to data delay	tWED	13		15		20		ns	
$\overline{OE}$ to $\overline{CAS}$ hold time	tOCH	5		5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	tCHO	5		5		5		ns	
$\overline{OE}$ precharge time	tOEP	5		5		5		ns	
$\overline{W}$ pulse width (Hyper Page Cycle)	tWPE	5		5		5		ns	
$\overline{RAS}$ pulse width(LL-ver)	tRASS	100		100		100		μs	13
$\overline{RAS}$ precharge time (LL-ver)	tRPS	90		110		130		ns	13
$\overline{CAS}$ hold time (LL-ver)	tCHS	-50		-50		-50		ns	13

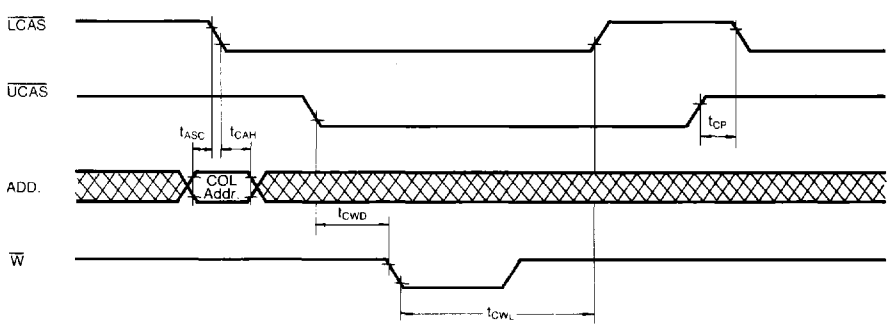
(*) -50ns Product : Output Loading (C_L)=50pF, V_{CC}=5V $\pm$ 5%

KM416C254B/BL/BLL Truth Table

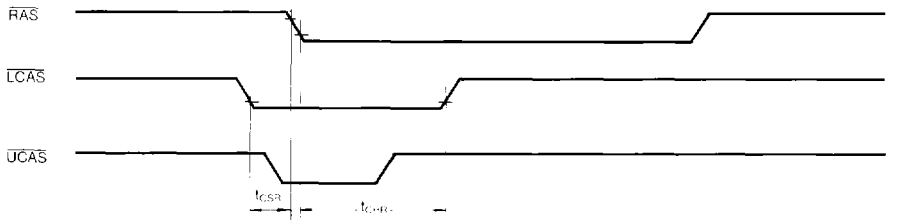
$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{W}$	$\overline{OE}$	DQ_1~DQ_8	DQ_9~DQ_{16}	STATE
H	X	X	X	X	HI-Z	HI-Z	Standby
L	H	H	X	X	HI-Z	HI-Z	Refresh
L	L	H	H	L	DQ-OUT	HI-Z	Byte Read
L	H	L	H	L	HI-Z	DQ-OUT	Byte Read
L	L	L	H	L	DQ-OUT	DQ-OUT	Word Read
L	L	H	L	H	DQ-IN	-	Byte Write
L	H	L	L	H	-	DQ-IN	Byte Write
L	L	L	L	H	DQ-IN	DQ-IN	Word Write
L	L	L	H	H	HI-Z	HI-Z	-

NOTES

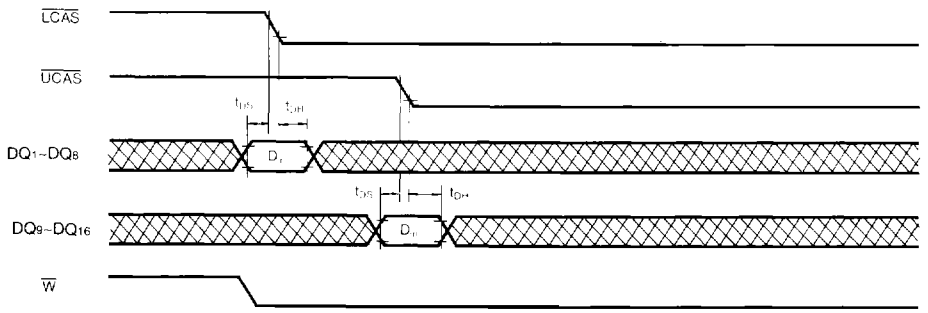
1. An initial pause of 200μs is required after power-up followed by any 8 ROR or CBR cycles before device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) are assumed to be 5ns for all inputs except t_{HPC} and t_{HPRWC}.
3. Measured with a load equivalent to 2 TTL loads and 100pF
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
12. $t_{ASC} \geq t_{CP}$ min, Assume tT=2.0 ns
13. 512 cycle of burst refresh must be executed within 8ms before and after self refresh in order to meet refresh specification (LL-Ver)
14. If $\overline{RAS}$ goes high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes high before $\overline{RAS}$ high going, the open circuit condition of the output is achieved by $\overline{RAS}$ high going.
15. t_{ASC}, t_{CAH} are referenced to the earlier $\overline{CAS}$ falling edge.
16. t_{CP} is specified from the last $\overline{CAS}$ rising edge in the previous cycle to the first $\overline{CAS}$ falling edge in the next cycle.
17. t_{CWD} is referenced to the later $\overline{CAS}$ falling edge at word read-modify-write cycle.
18. t_{CWL} is specified from $\overline{W}$ falling edge to the earlier $\overline{CAS}$ rising edge.



19. t_{CSR} is refernced to earlier $\overline{CAS}$ falling low before $\overline{RAS}$ transition low.
20. t_{CHR} is referenced to the later $\overline{CAS}$ rising high after $\overline{RAS}$ transition low



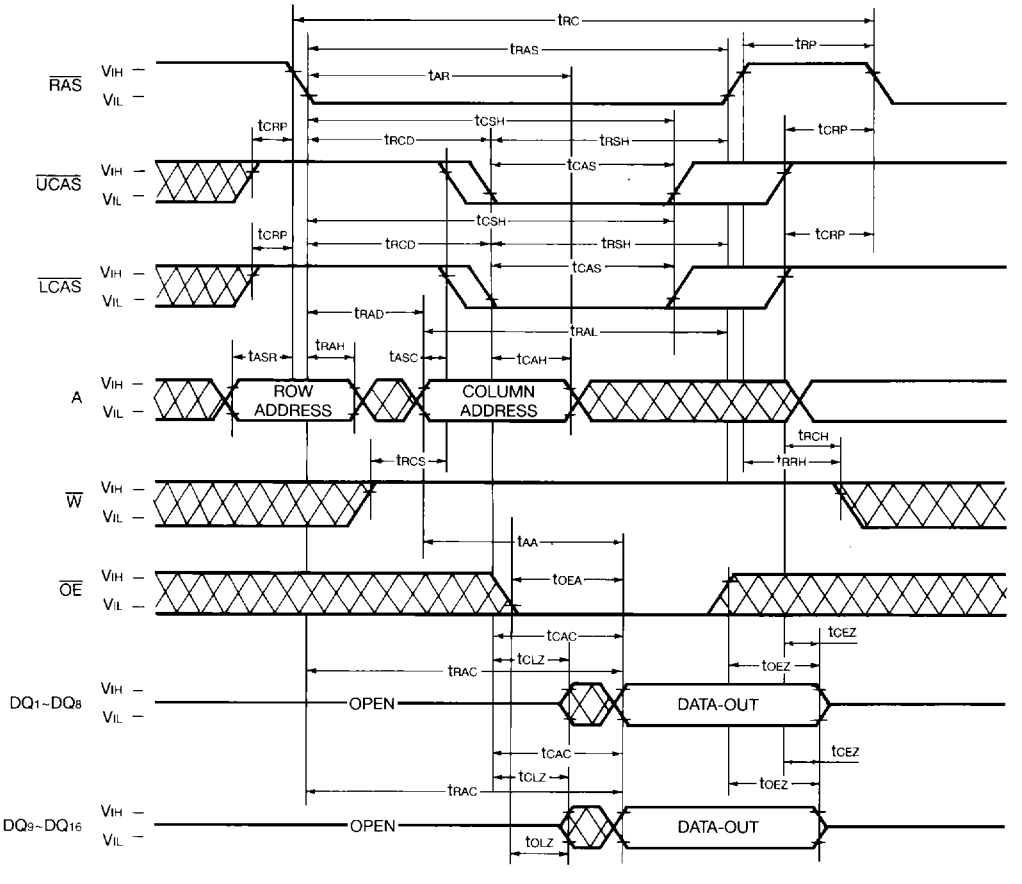
21. t_{DS}, t_{DH}, is independently specified for lower byte $D_{IN(1-8)}$, upper byte $D_{in(9-16)}$.



TIMING DIAGRAM

WORD READ CYCLE

NOTE : DIN=OPEN

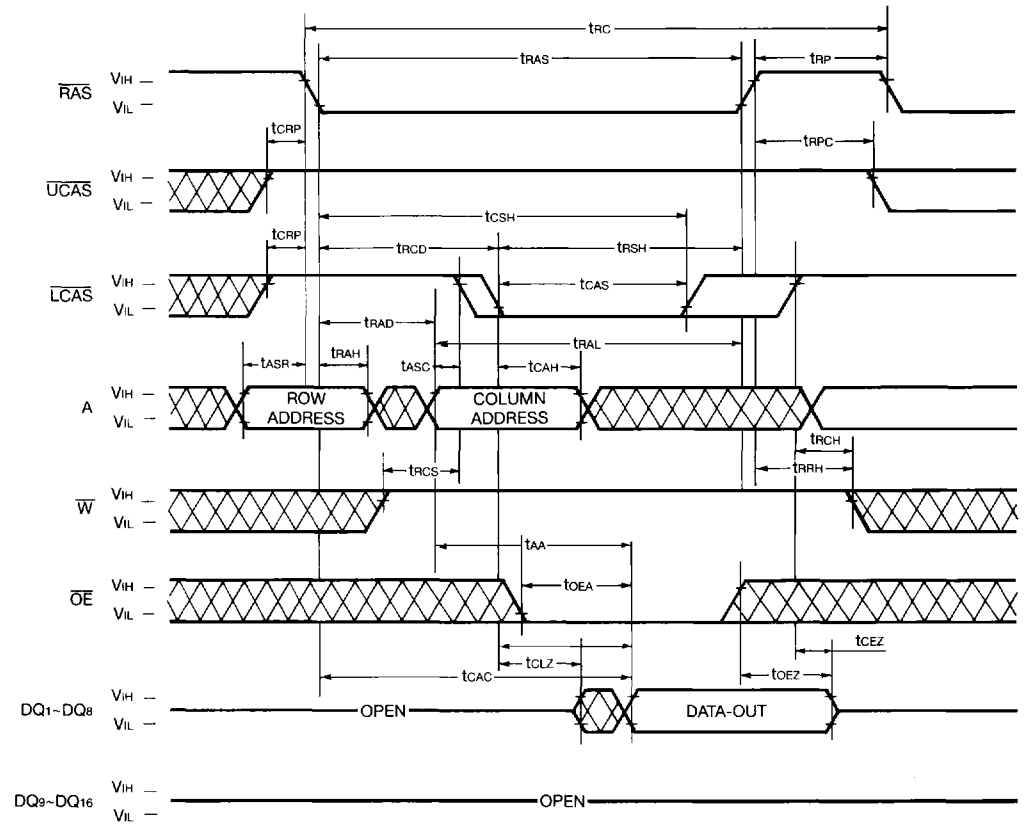


SAMSUNG ELECTRONICS

TIMING DIAGRAM

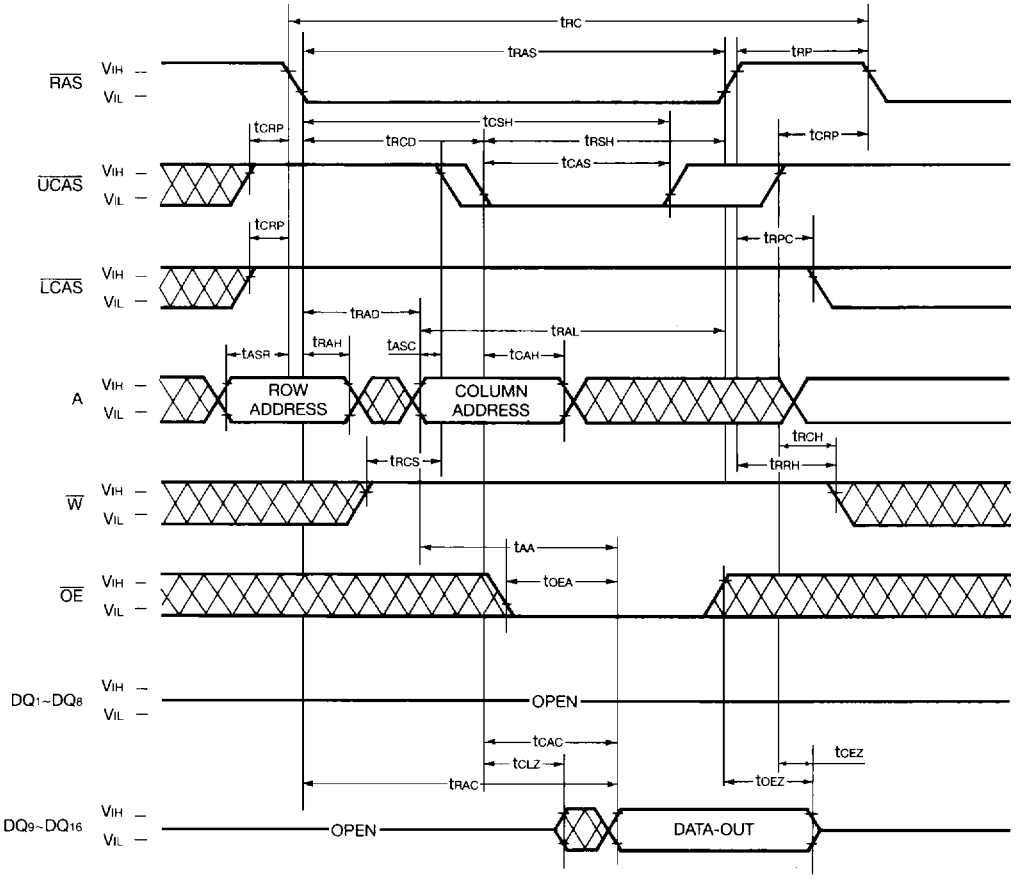
LOWER BYTE READ CYCLE

NOTE : DIN=OPEN



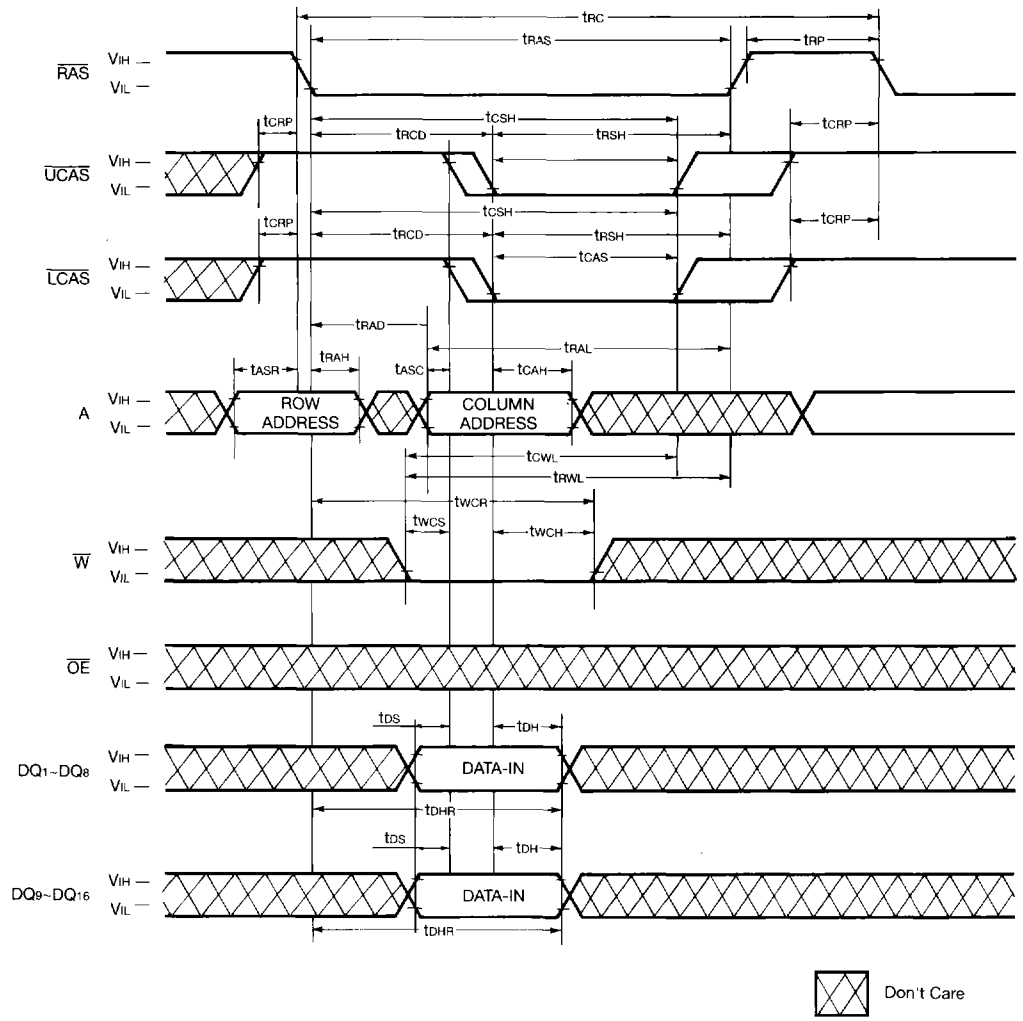
UPPER BYTE READ CYCLE

NOTE : DIN=OPEN



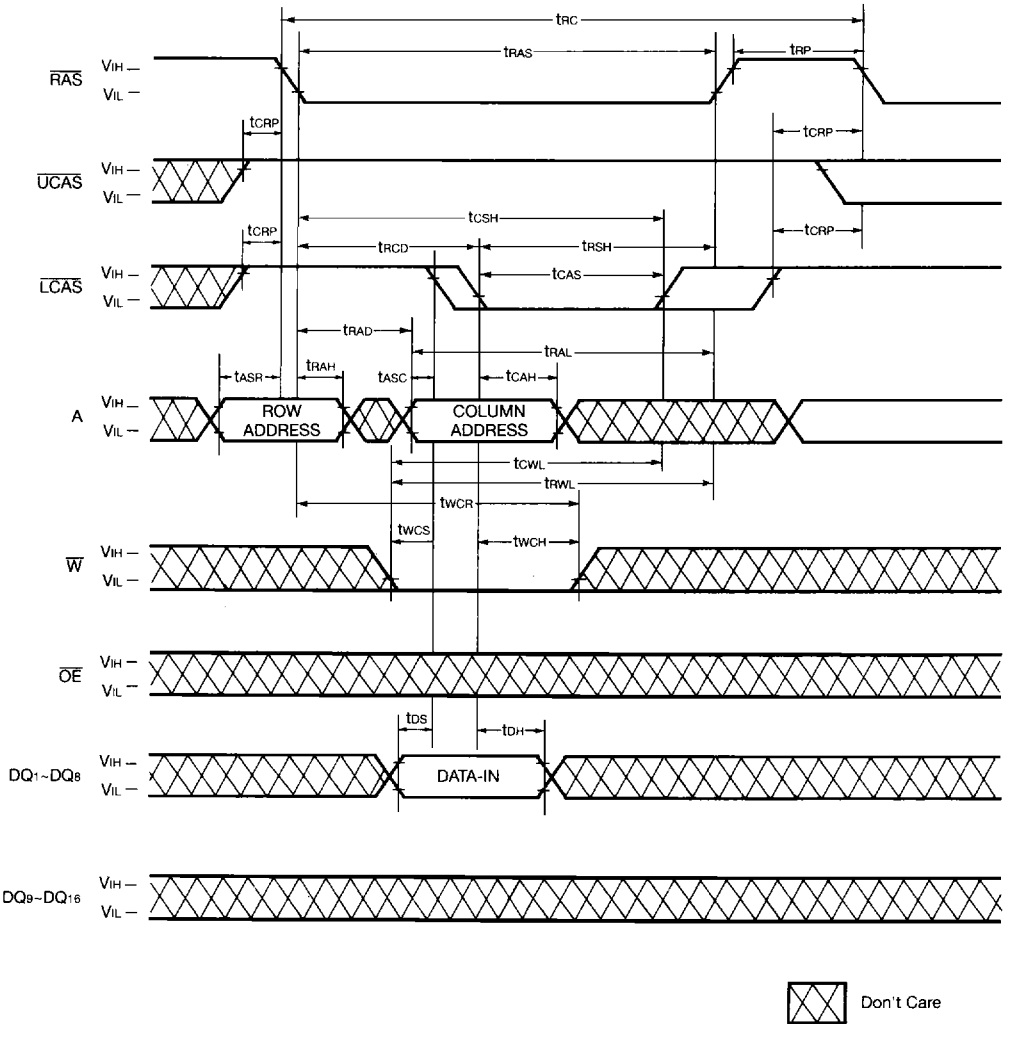
WORD WRITE CYCLE (EARLY WRITE)

NOTE : DOUT=OPEN



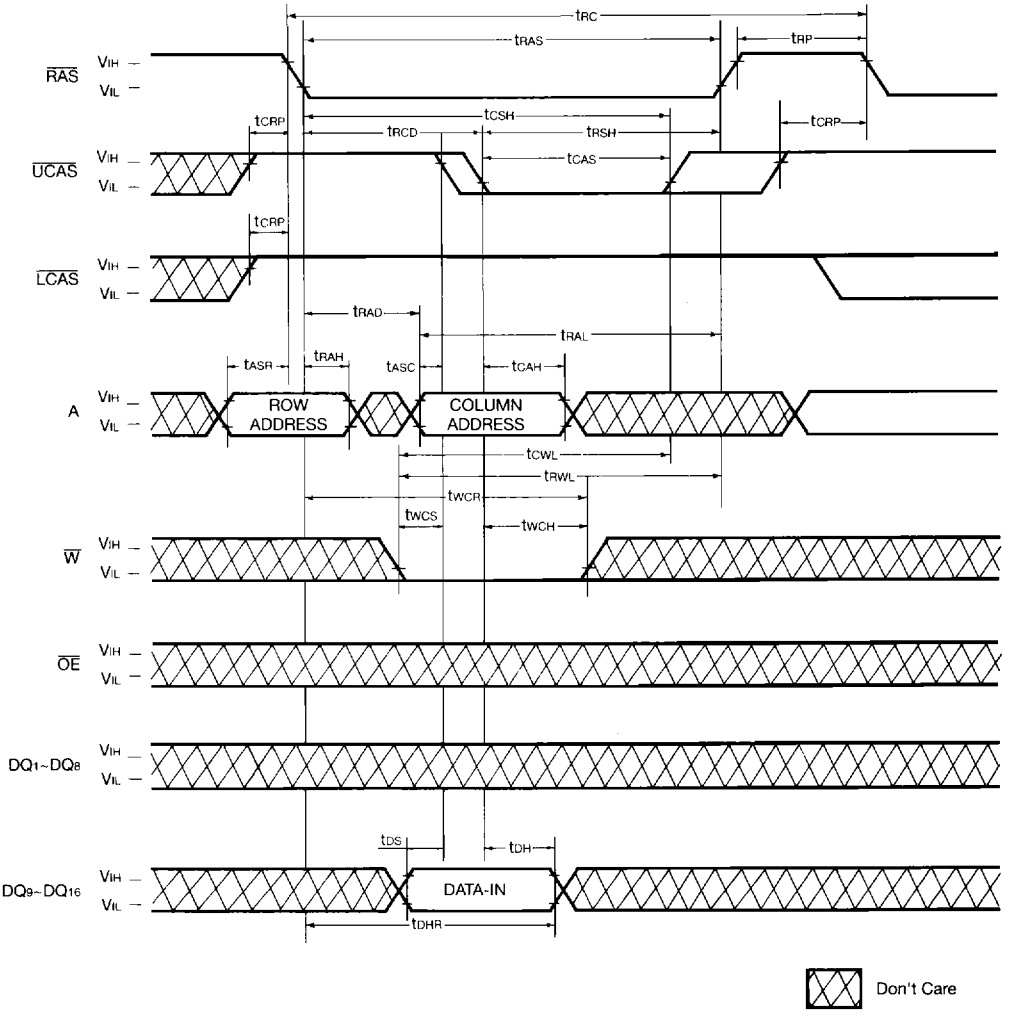
LOWER BYTE WRITE CYCLE (EARLY WRITE)

NOTE : DOUT=OPEN



UPPER BYTE WRITE CYCLE (EARLY WRITE)

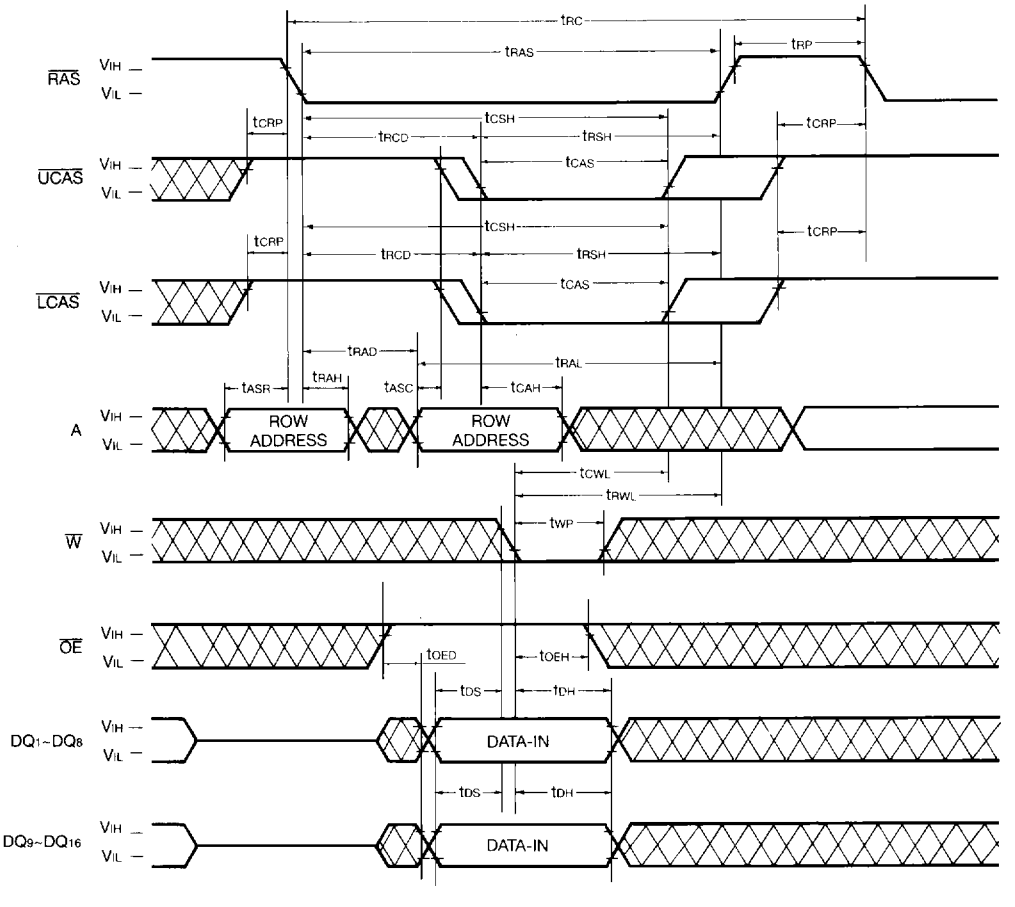
NOTE : DOUT=OPEN



SAMSUNG ELECTRONICS

WORD WRITE CYCLE (OE CONTROLLED WRITE)

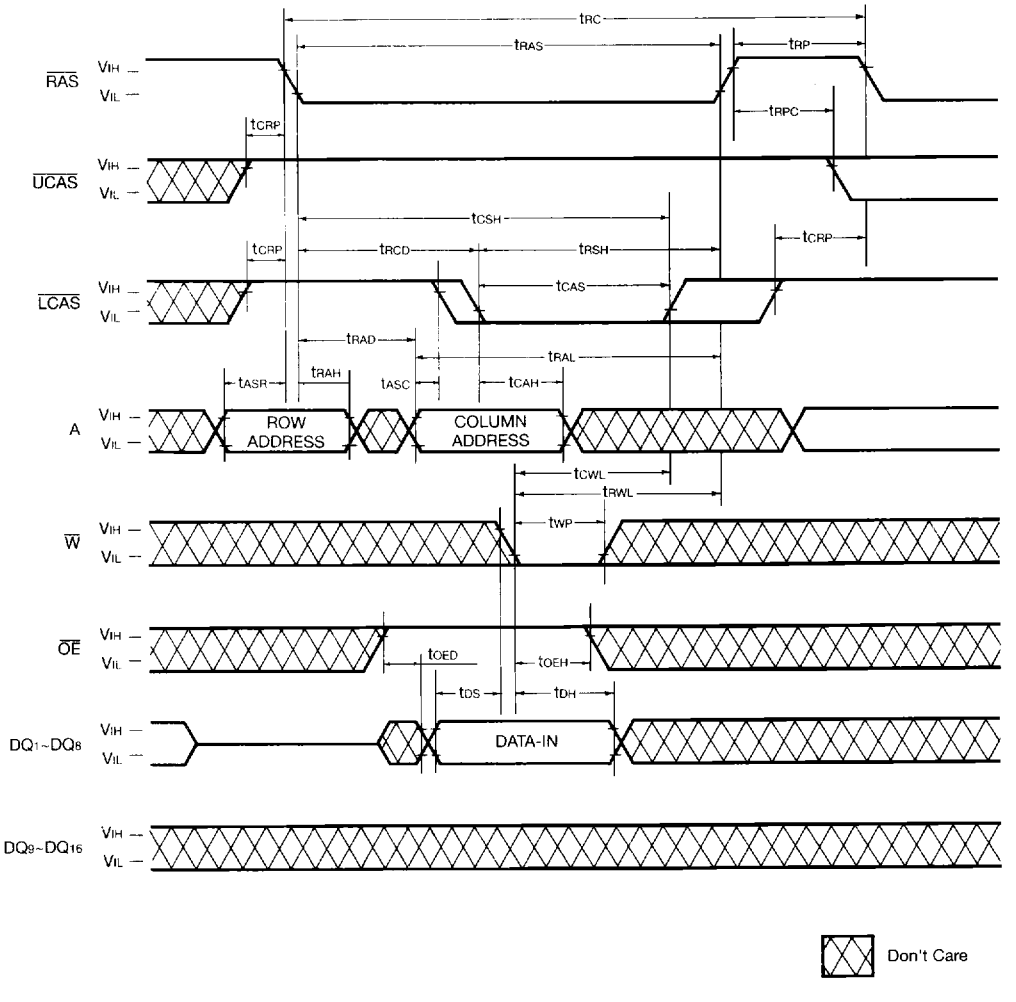
NOTE : DOUT=OPEN



SAMSUNG ELECTRONICS

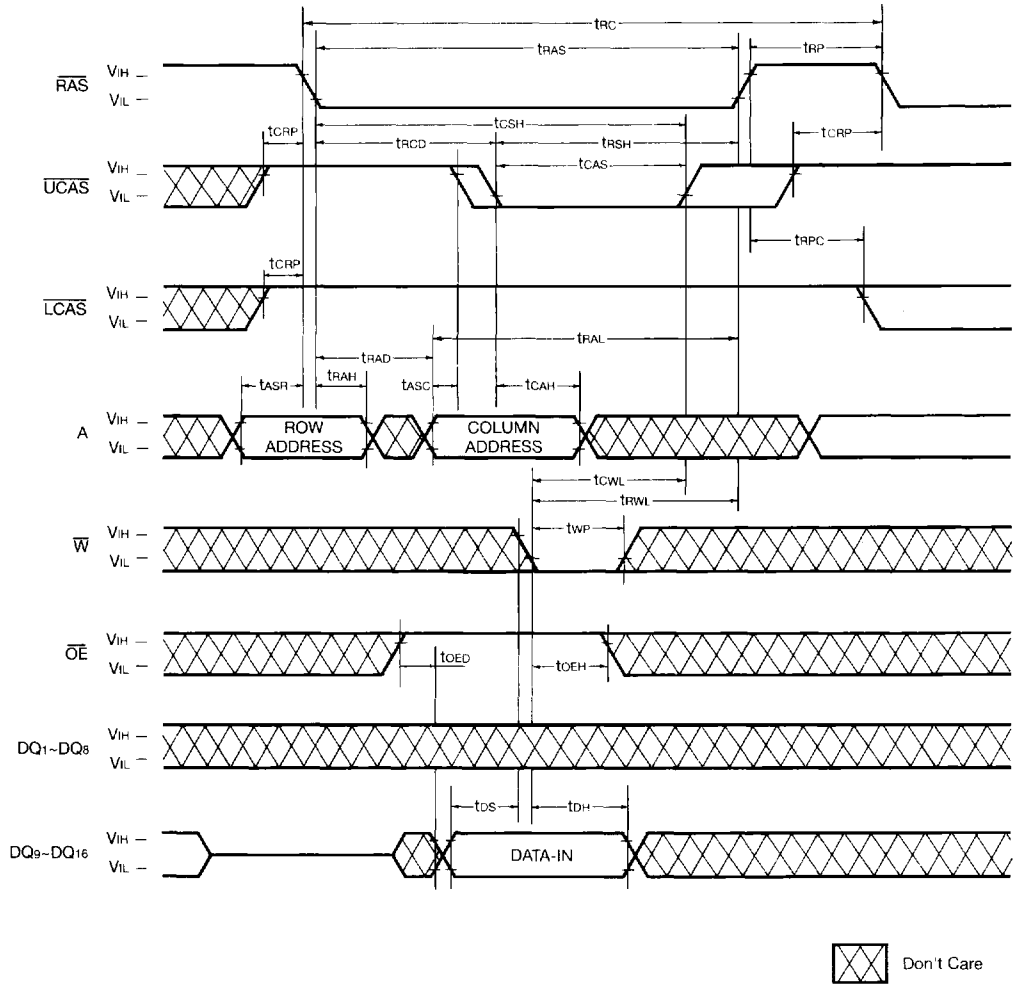
LOWER BYTE WRITE CYCLE (OE CONTROLLED WRITE)

NOTE : DOUT=OPEN

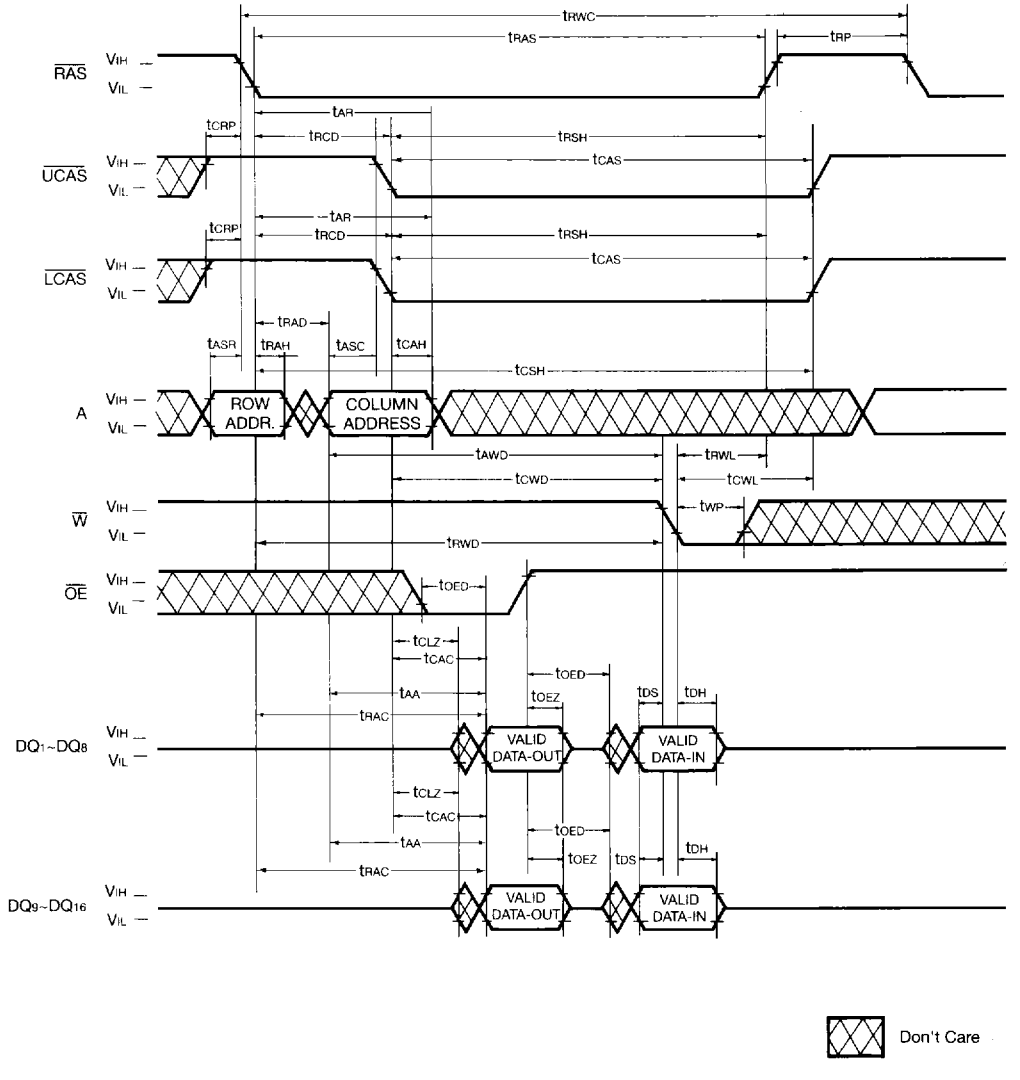


UPPER BYTE WRITE CYCLE (OE CONTROLLED WRITE)

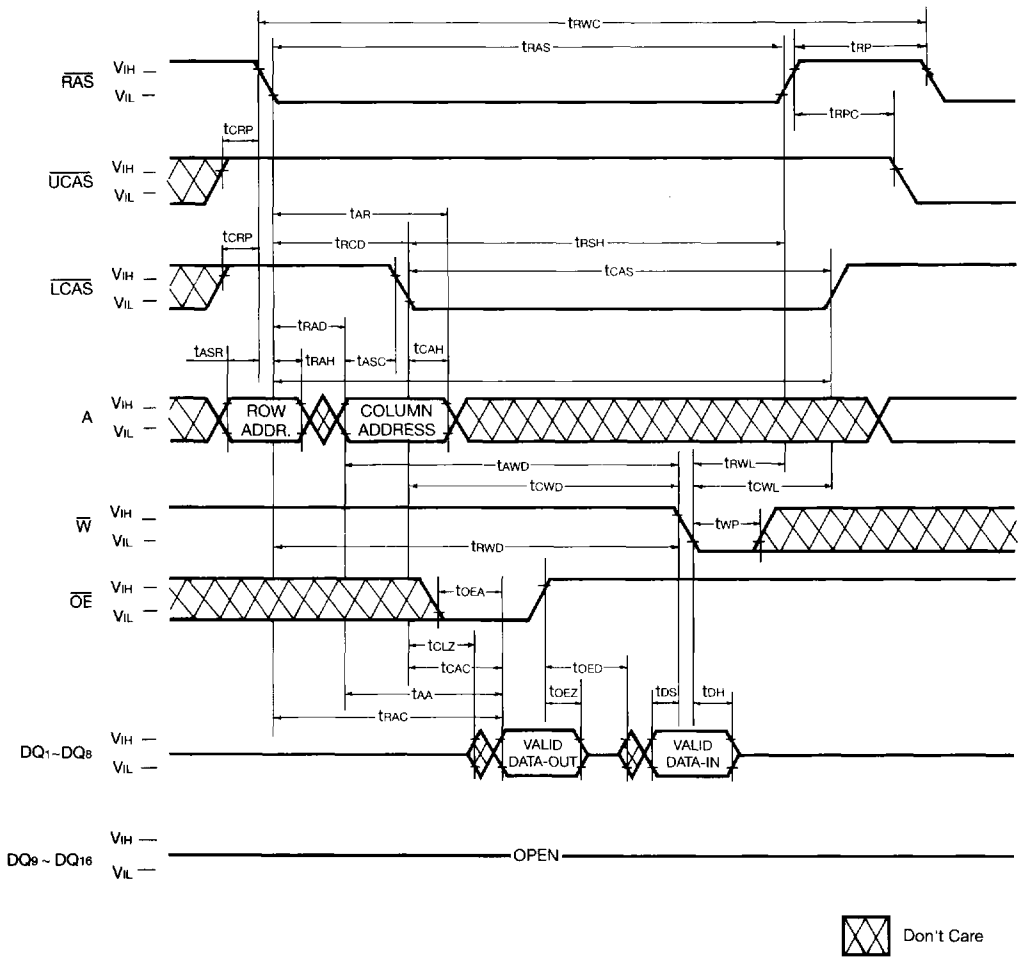
NOTE : DOUT=OPEN



WORD READ-MODIFY-WRITE CYCLE

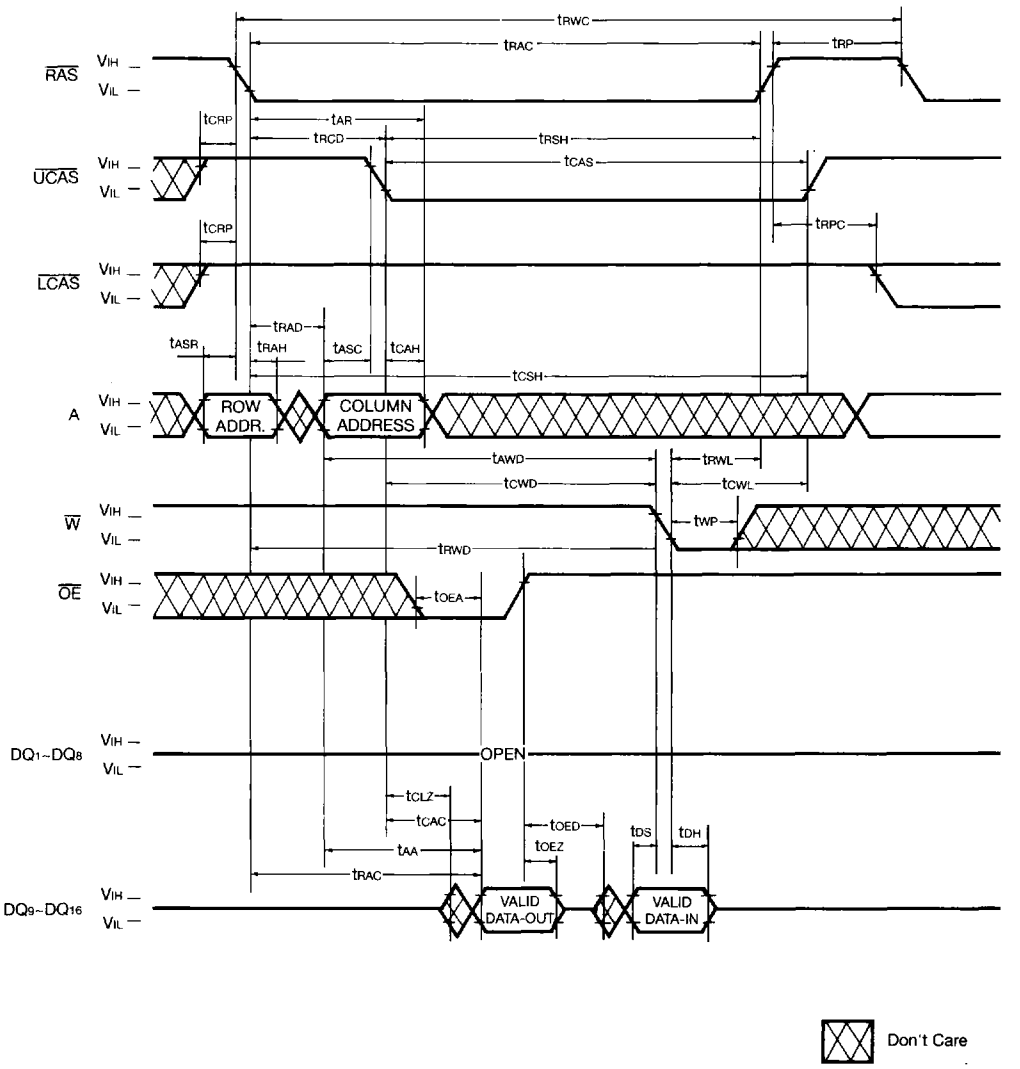


LOWER-BYTE READ-MODIFY-WRITE CYCLE

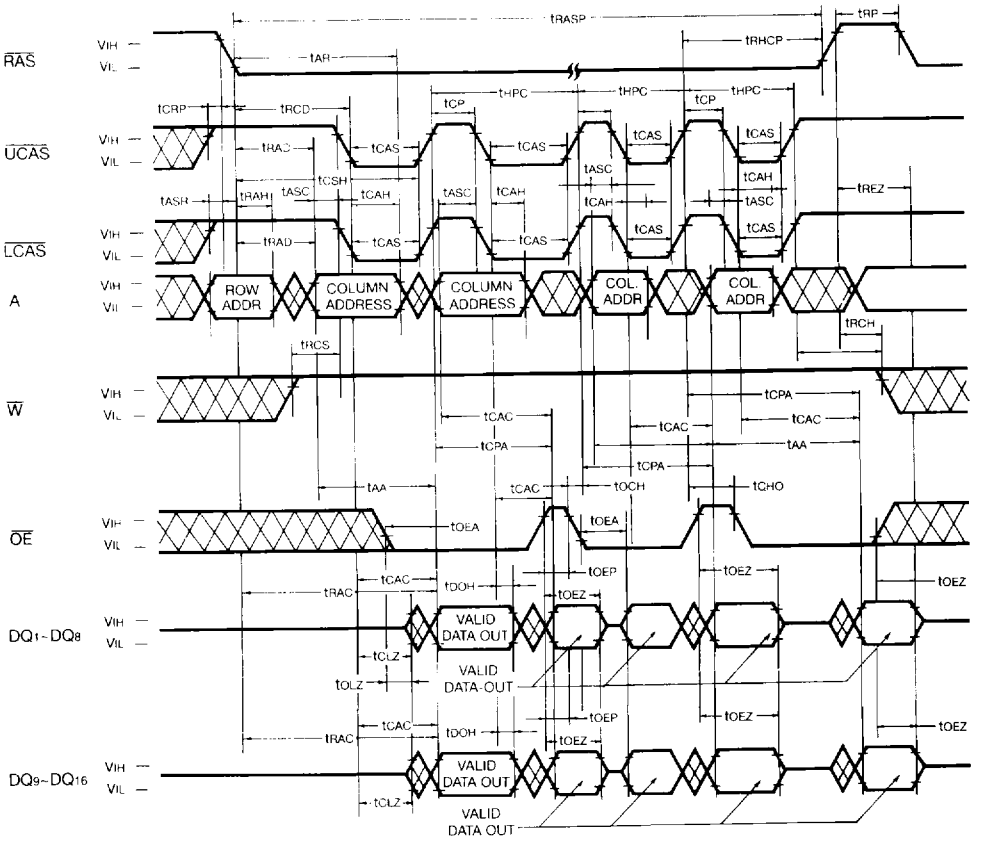


4

UPPER-BYTE READ-MODIFY-WRITE CYCLE

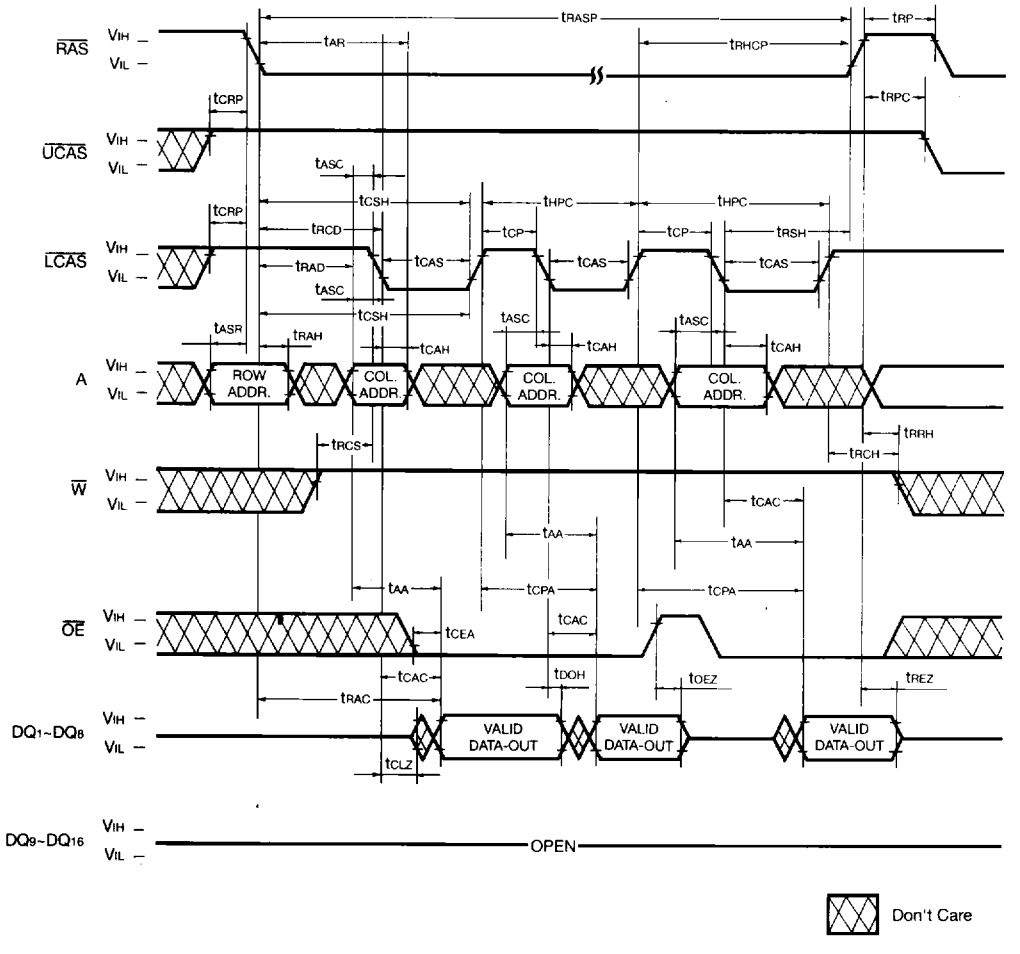


HYPER PAGE MODE WORD READ CYCLE

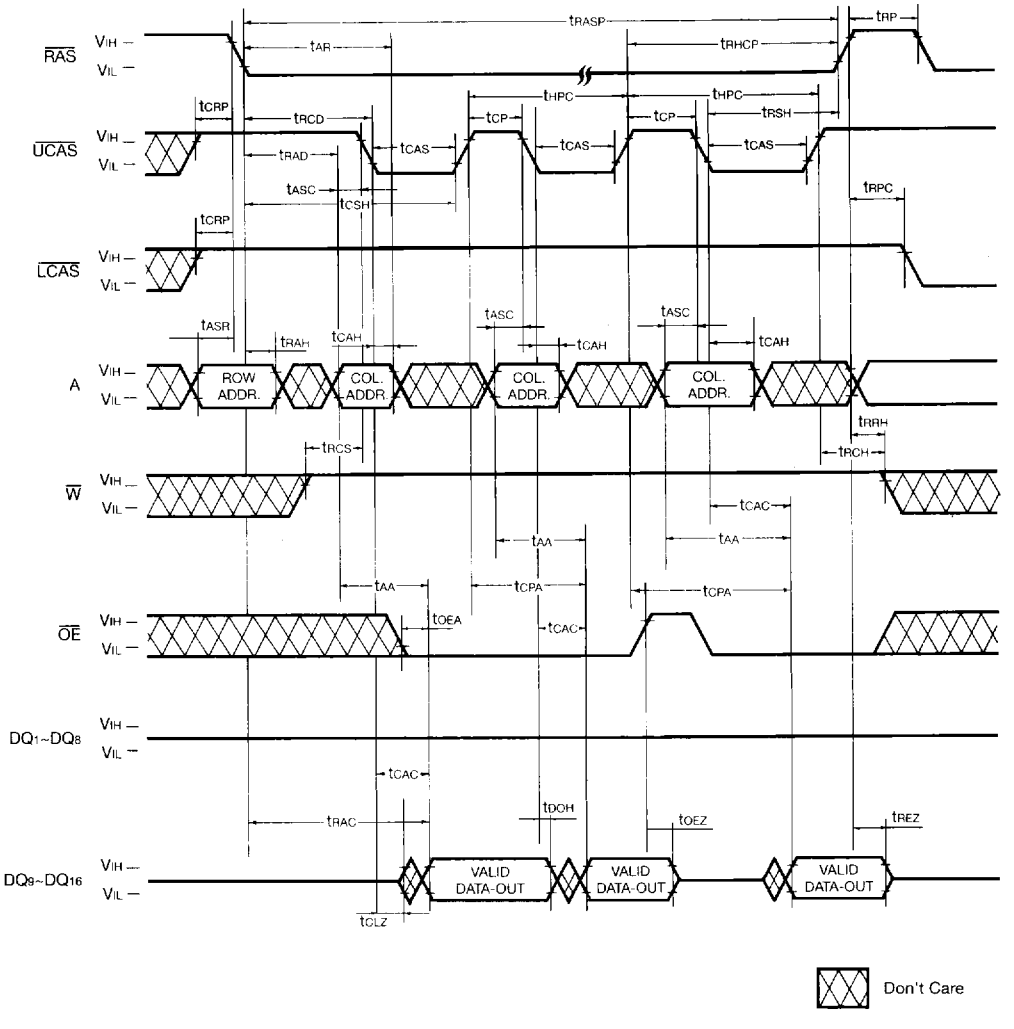


SAMSUNG ELECTRONICS

HYPER PAGE MODE LOWER BYTE READ CYCLE

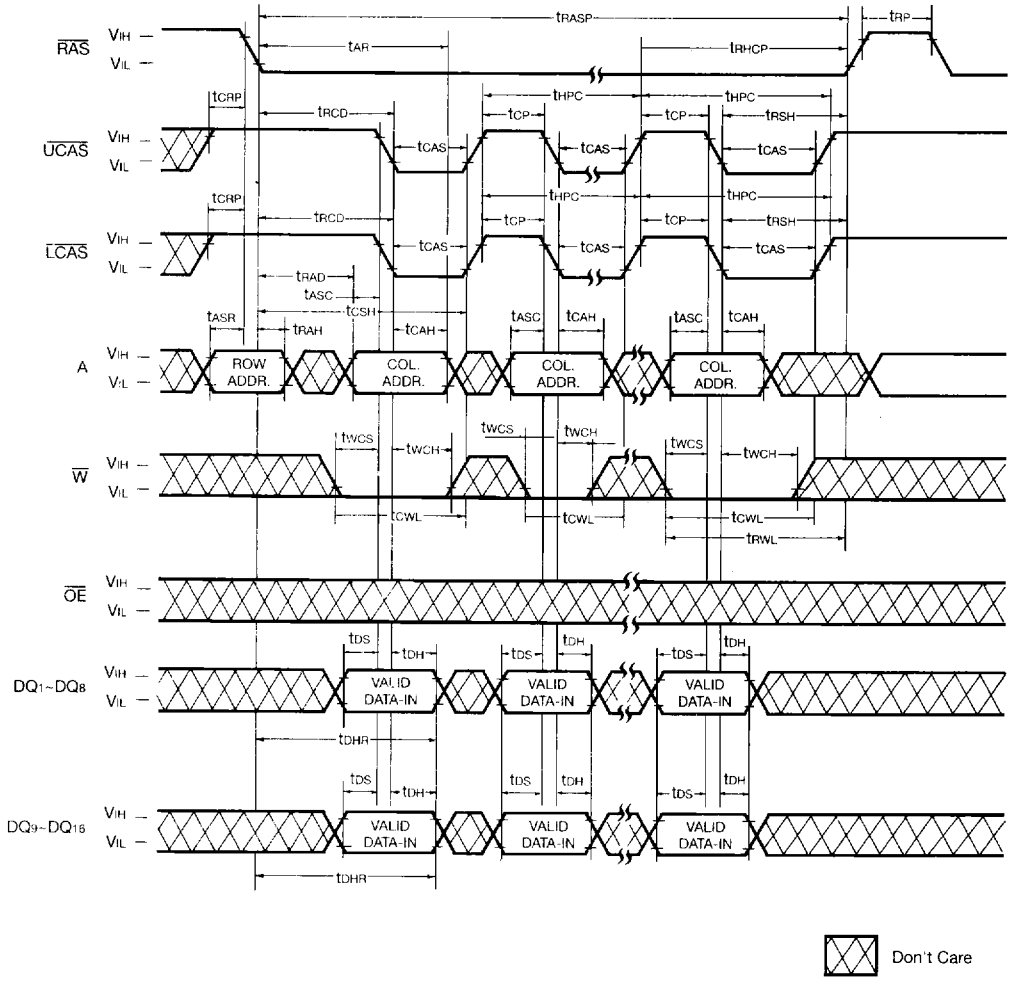


HYPER PAGE MODE UPPER BYTE READ CYCLE



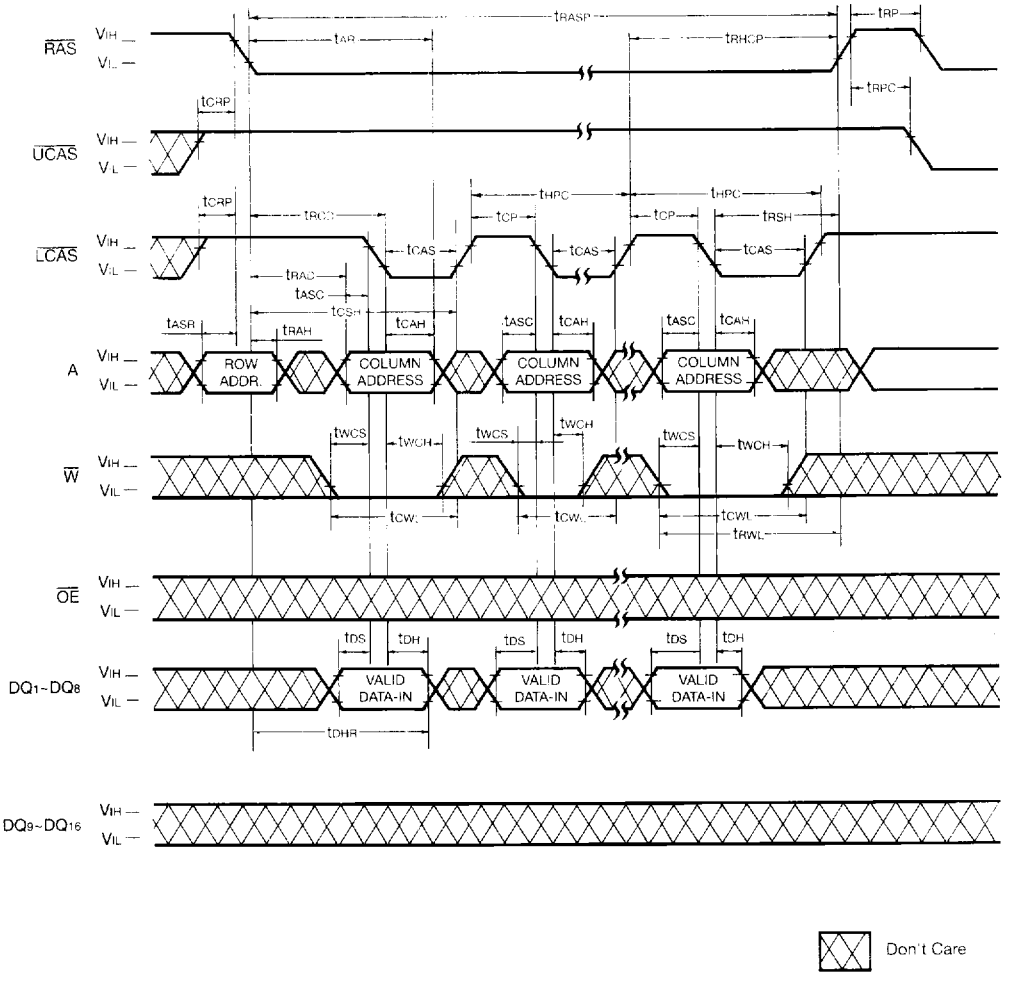
HYPER PAGE MODE WORD WRITE CYCLE (EARLY WRITE)

NOTE : DOUT=OPEN



HYPER PAGE MODE LOWER BYTE WRITE CYCLE (EARLY WRITE)

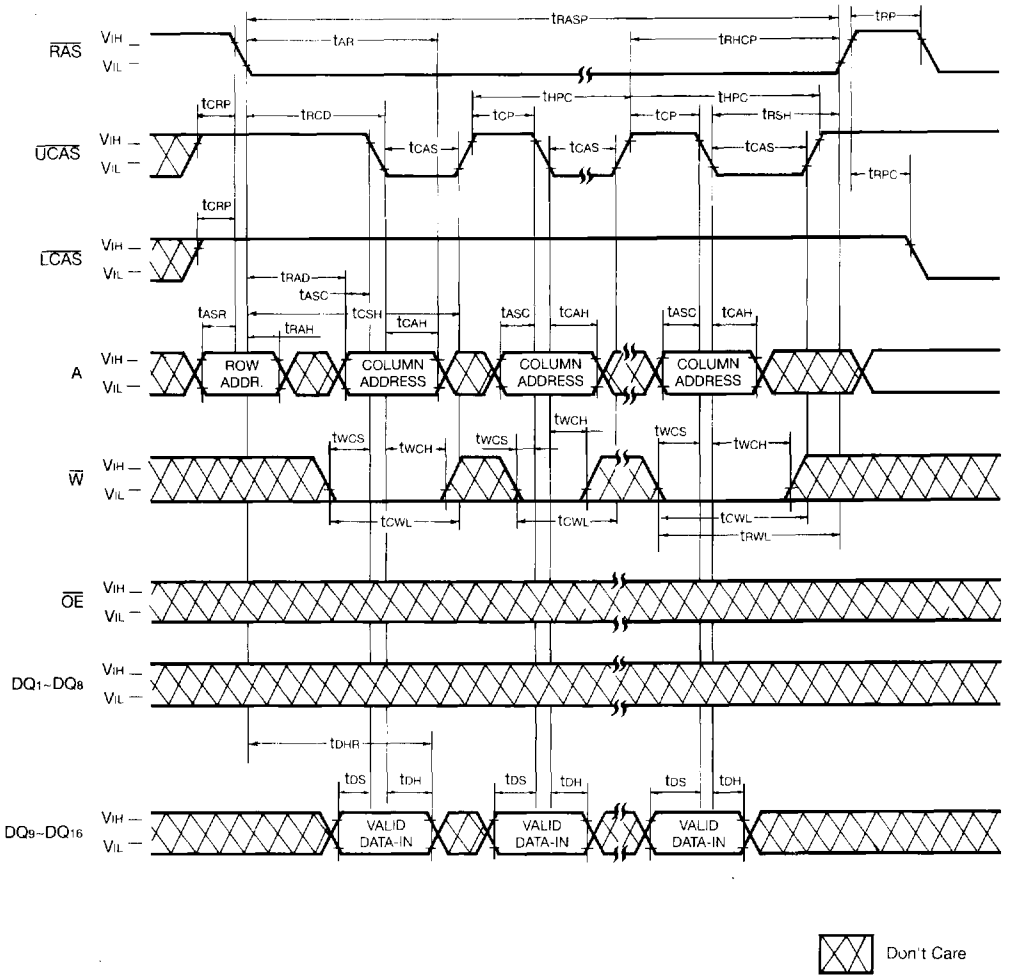
NOTE : DOUT=OPEN



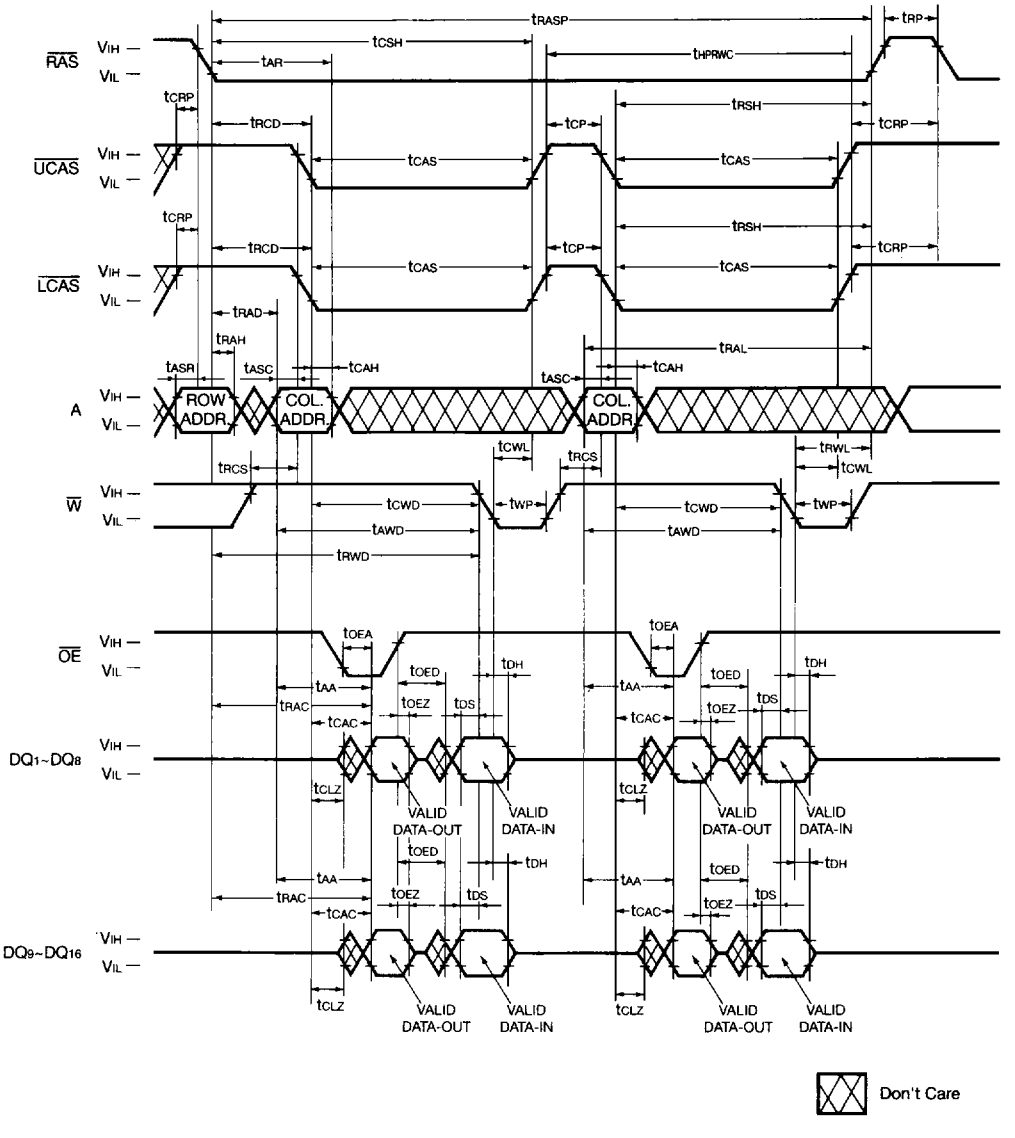
SAMSUNG ELECTRONICS

HYPER PAGE MODE UPPER BYTE WRITE CYCLE (EARLY WRITE)

NOTE : DOUT=OPEN

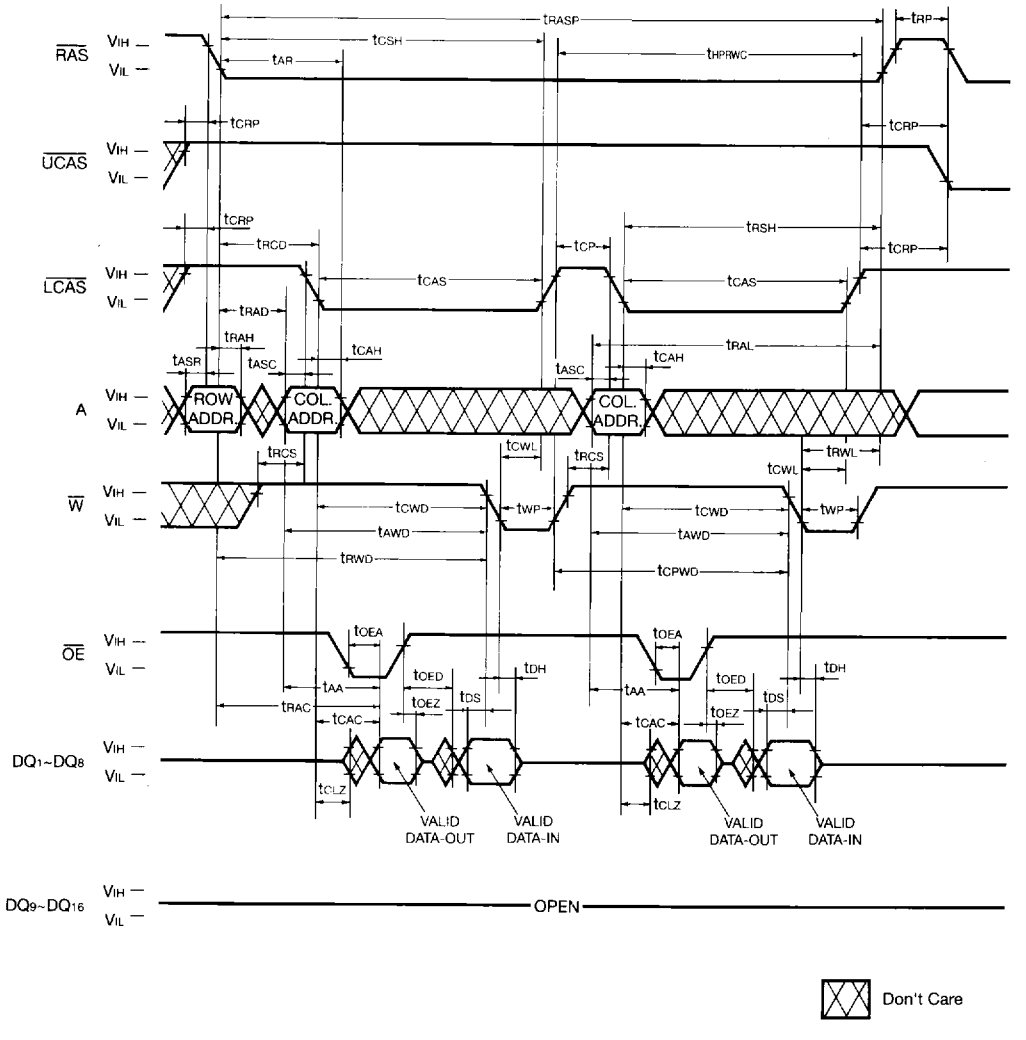


HYPER PAGE MODE WORD READ-MODIFY-WRITE CYCLE

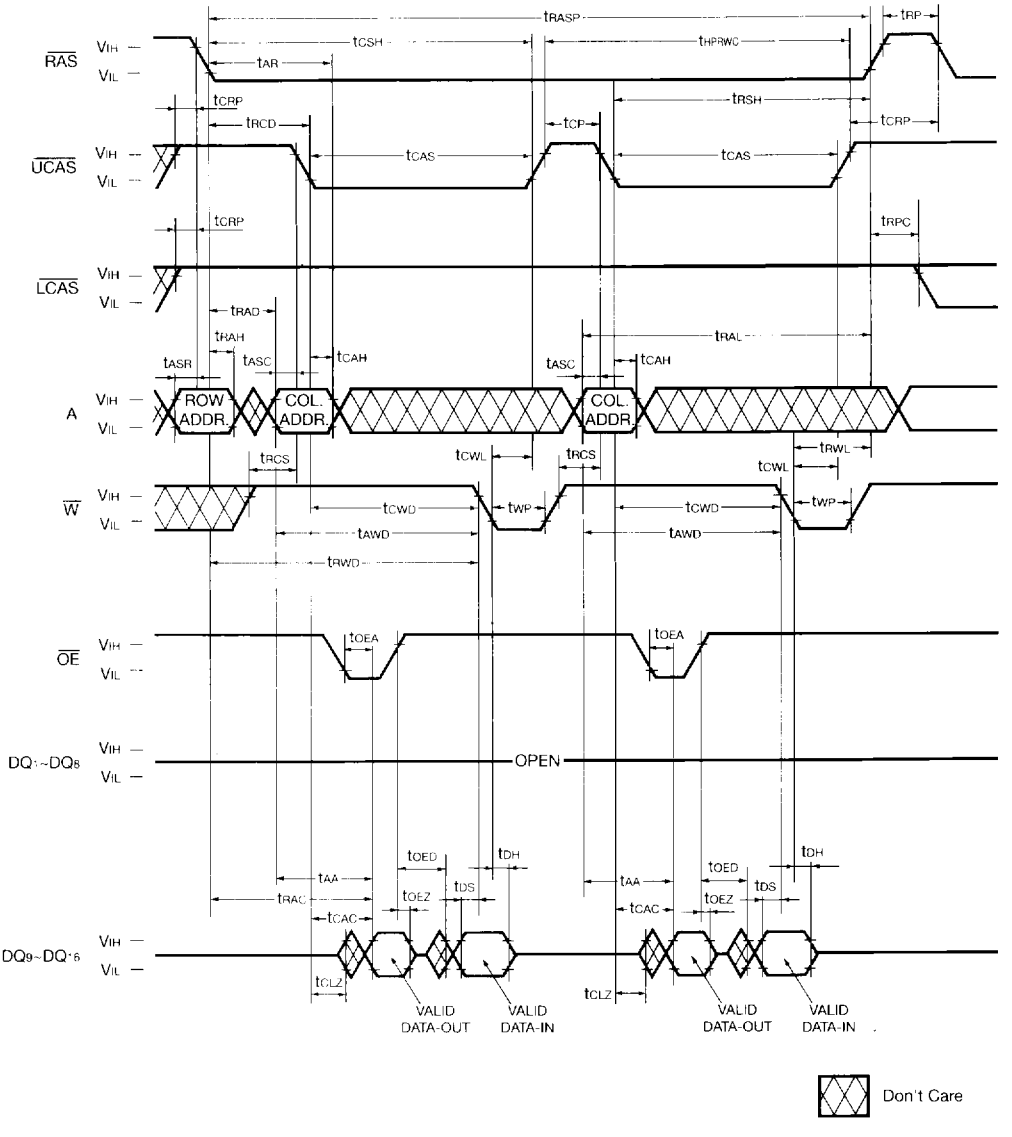


SAMSUNG ELECTRONICS

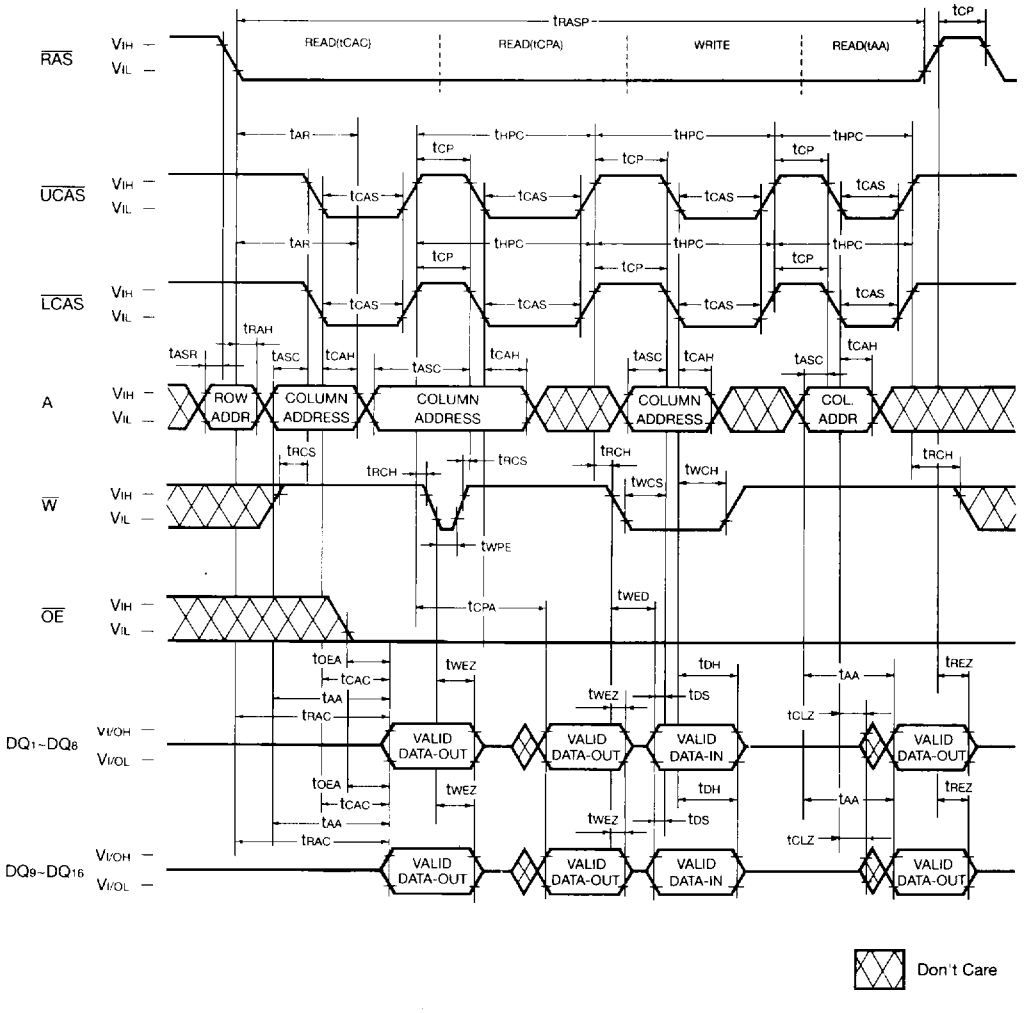
HYPER PAGE MODE LOWER-BYTE-READ-MODIFY-WRITE CYCLE



HYPER PAGE MODE UPPER-BYTE-READ-MODIFY-WRITE CYCLE

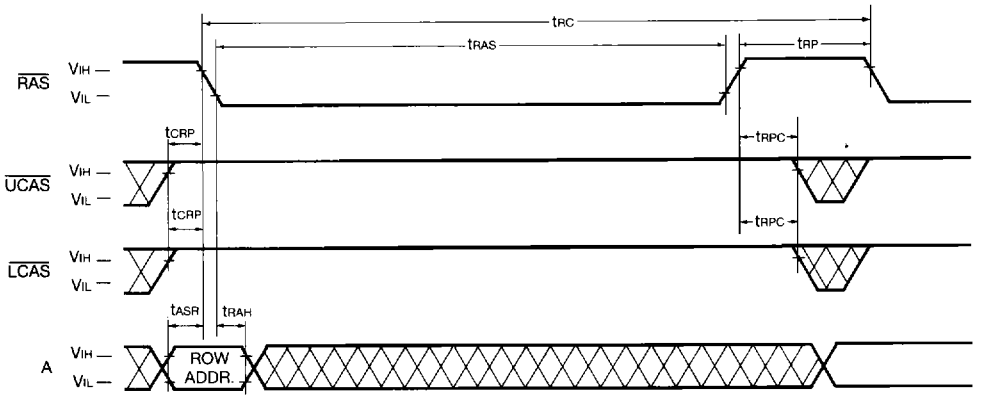


HYPER PAGE READ AND WRITE MIXED CYCLE



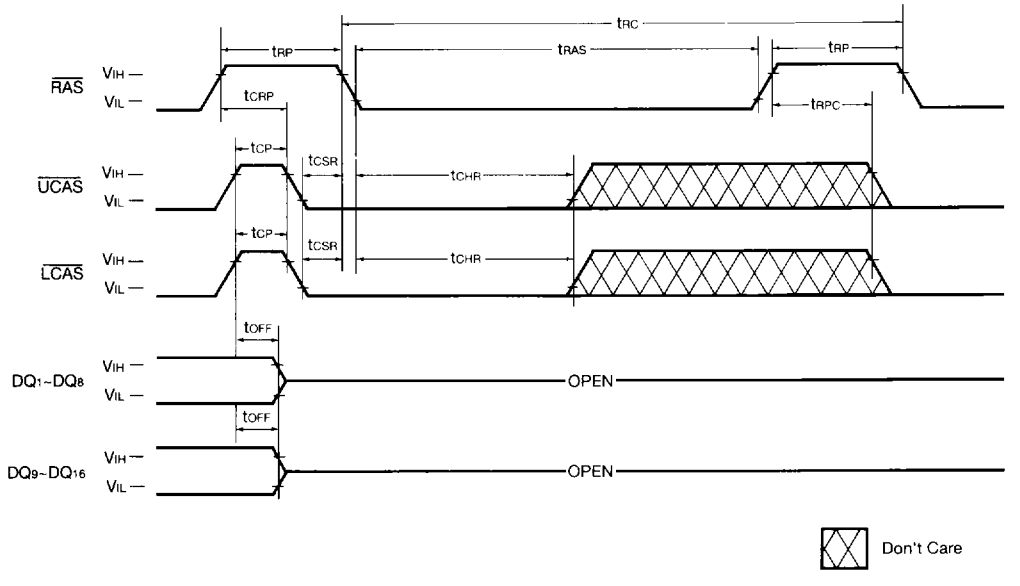
$\overline{RAS}$-ONLY REFRESH CYCLE

NOTE : $\overline{W}$, $\overline{OE}$, D_{IN}=Don't Care
D_{OUT}=OPEN



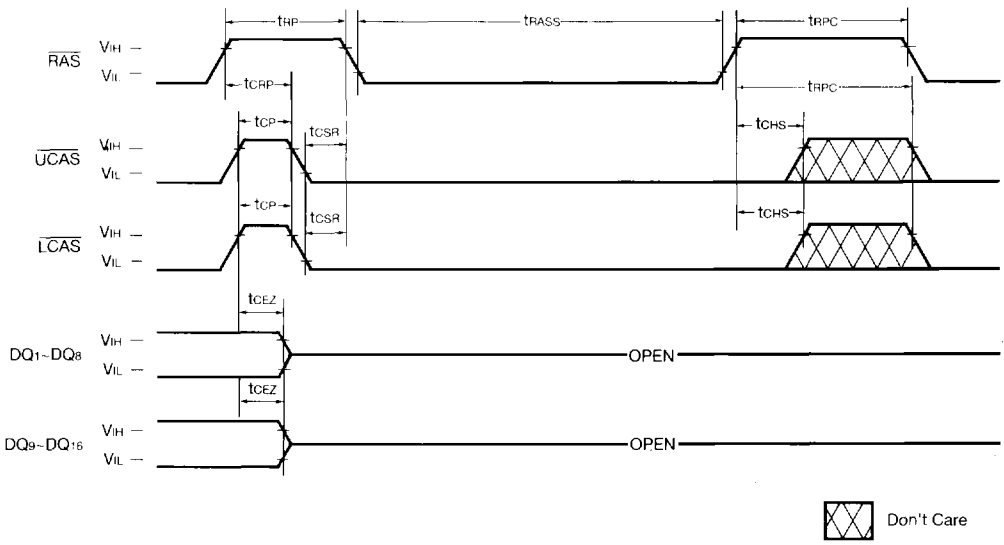
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE : $\overline{W}$, $\overline{OE}$, A=Don't Care

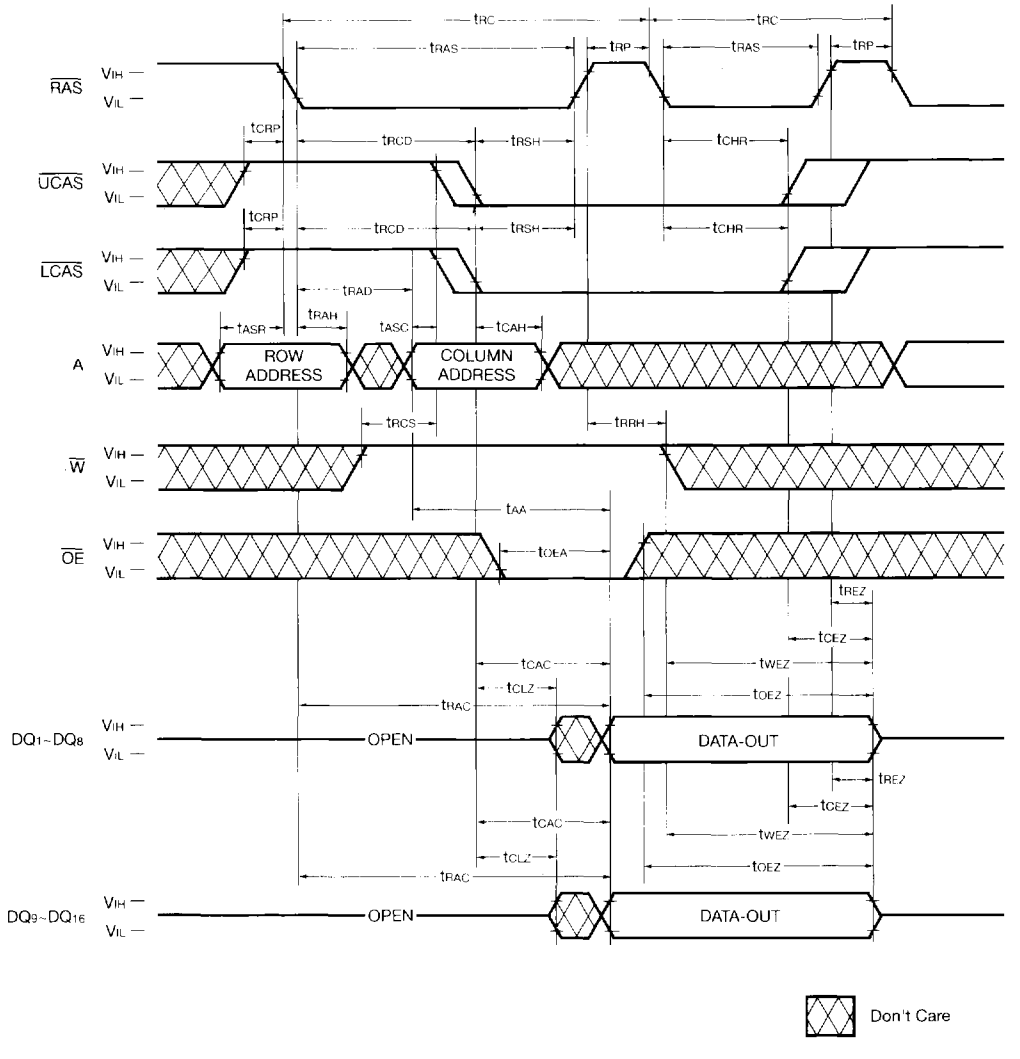


$\overline{CAS}$-BEFORE-$\overline{RAS}$ SELF REFRESH CYCLE (LL-Version)

NOTE : $\overline{W}$, $\overline{OE}$, A=Don't Care



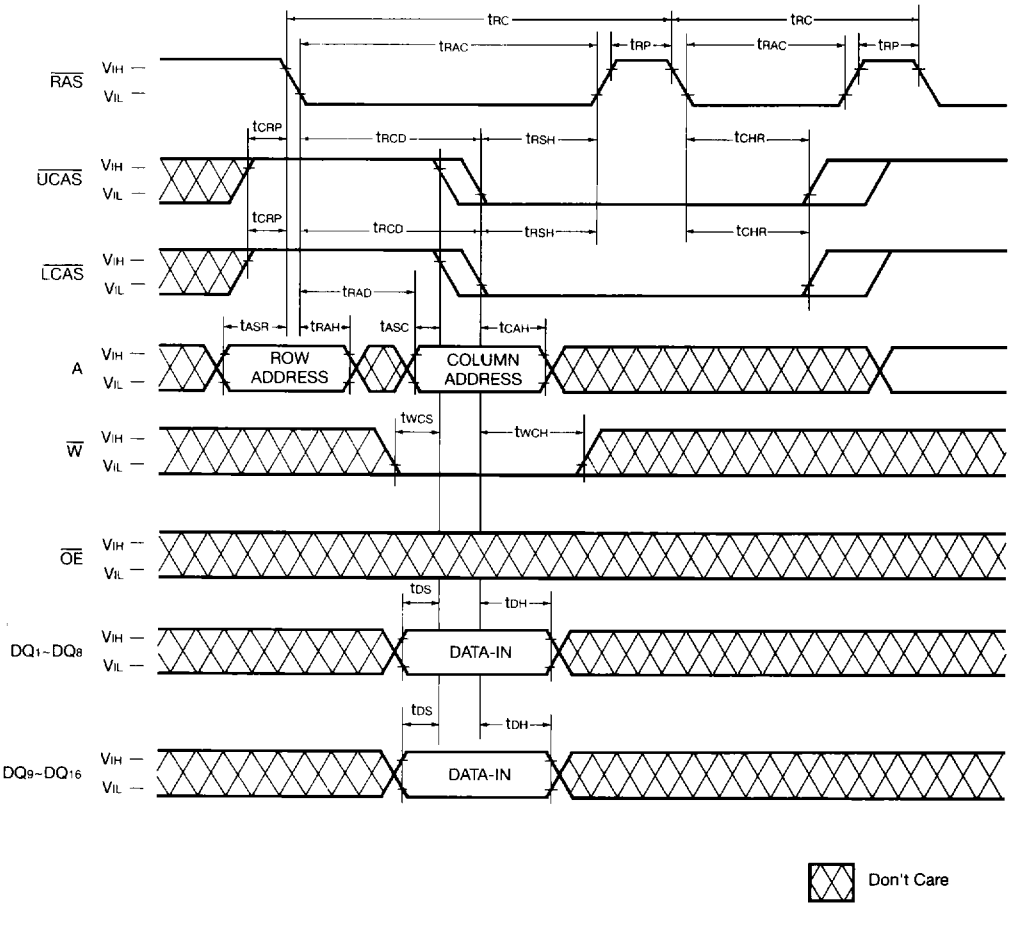
HIDDEN REFRESH CYCLE (READ)



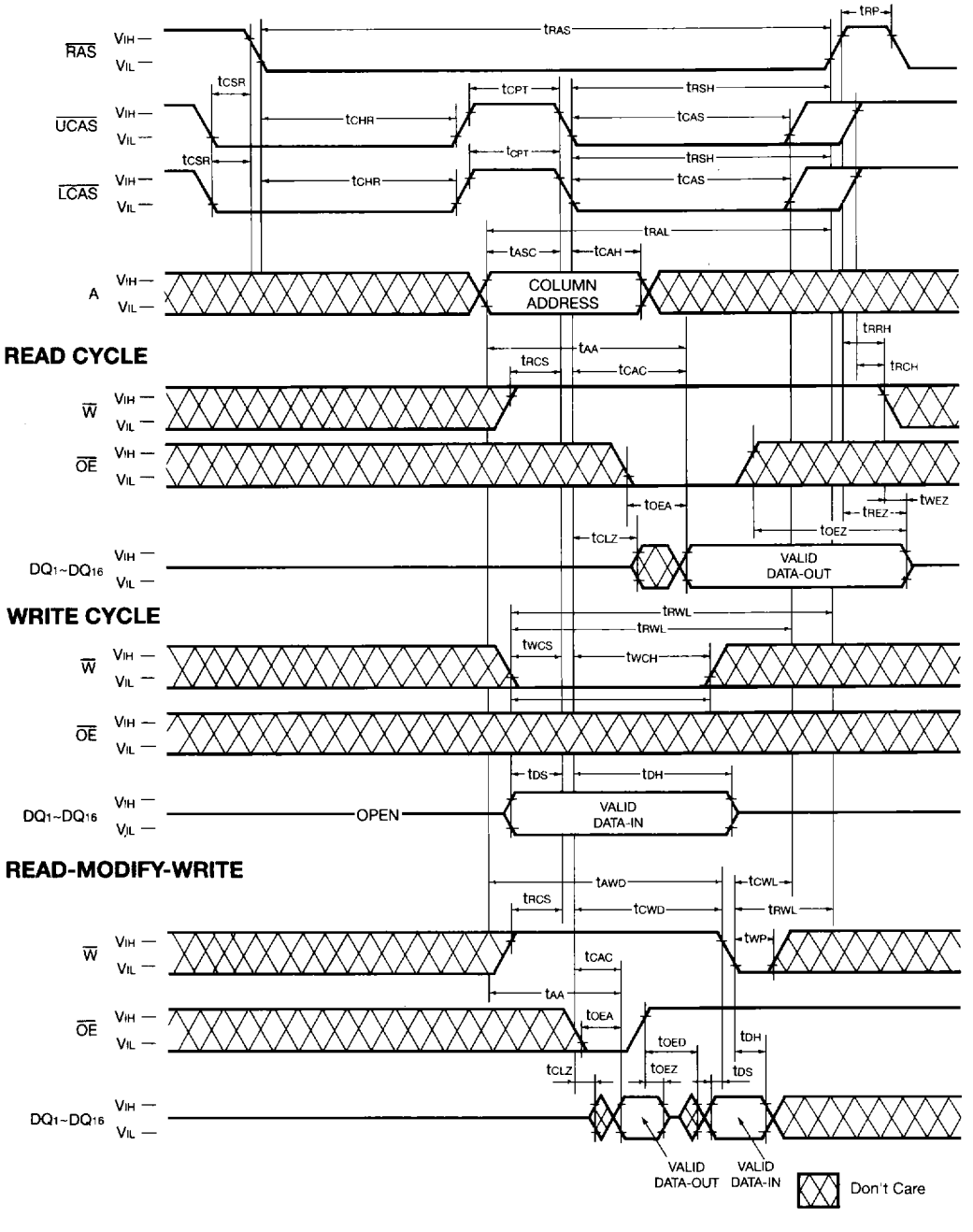
4

HIDDEN REFRESH CYCLE (WRITE)

NOTE : DOUT=OPEN



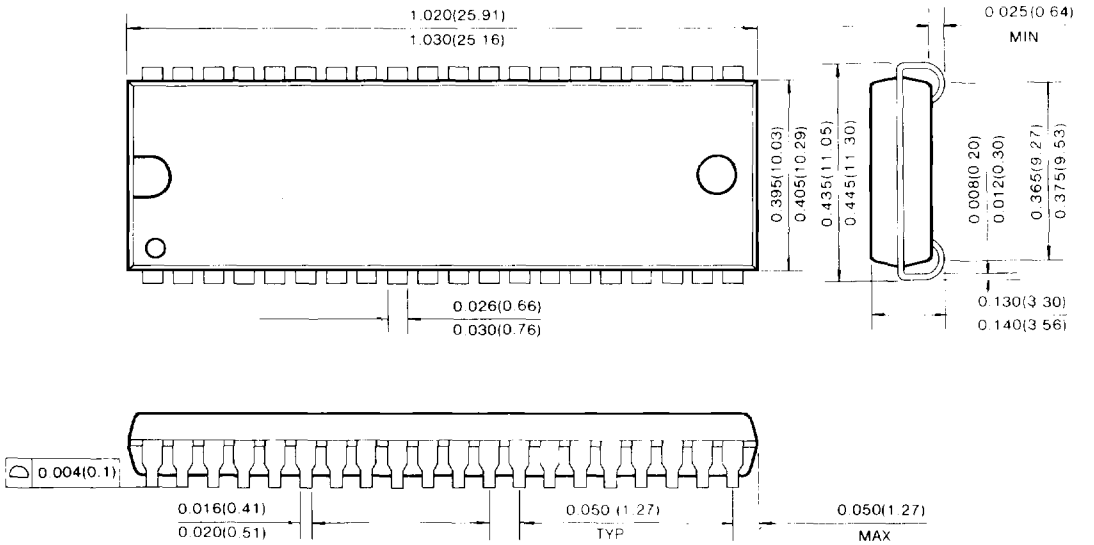
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



PACKAGE DIMENSION

40-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



40 LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE (II)
(Forward and Reverse Type)