IT8711F Application Circuit V0.2

REVISION HISTORY

SCHEMATIC REVISION	PCB REVISION	MODIFICATION ITEMS	DRAWING AND MODIFICATION DESCRITION	DATE
IT-8711-CG-S01 VER 0.1	N/A	First Draft	For INTEL Chipset	April 17,2001
IT-8711-CG-S01 VER 0.2	N/A	1. Modify U1 Pin27 Connect to 3VSB 2. Adding VID Circuit 3. Modify R11 & R12 from 22 ohm to 4.7K ohm 4. Modify R33 & RN8 from 1k ohm to 150 ohm 5. Add JP8 for Keyboard/Mouse Power supplied by VCC/VCCH 6. Add Layout/Routing Guidelines for 3VSB circuit 7. Swap IT8711 Pin67 and Pin68 off-page connector label		June 21,2001

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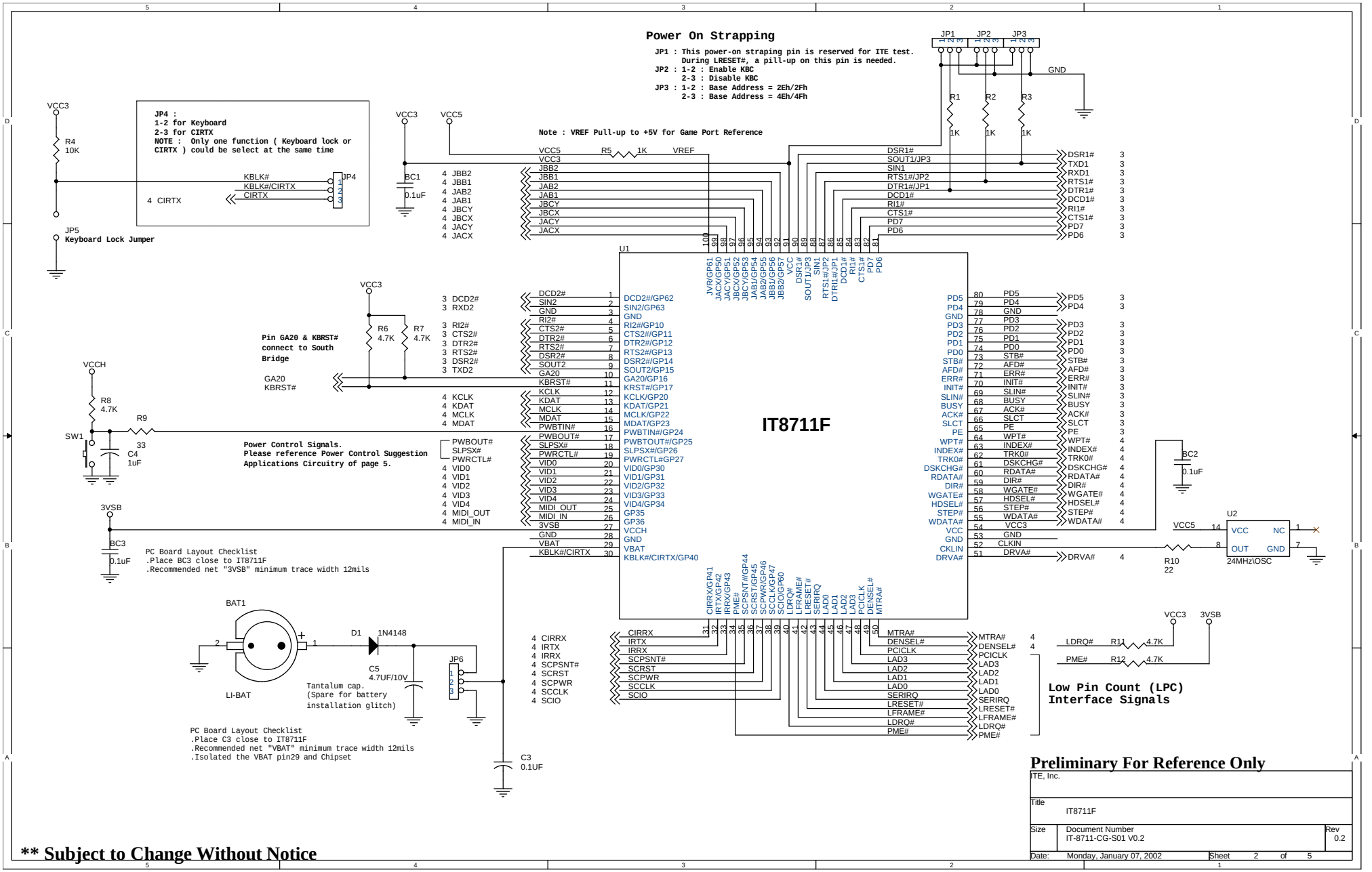
Power On Strapping
JP1 : This power-on straping pin is reserved for ITE test.
During LRESET#, a pill-up on this pin is needed.
JP2 : 1-2 : Enable KBC
2-3 : Disable KBC
JP3 : 1-2 : Base Address = 2Eh/2Fh
2-3 : Base Address = 4Eh/4Fh
JP1
JP2
JP3
GND
R1
R2
R3
1K
JP4 :
1-2 for Keyboard
2-3 for CIRTX
NOTE : Only one function (Keyboard lock or CIRTX) could be select at the same time
VCC3
R4
10K
KBLK#
KBLK#/CIRTX
CIRTX
4 CIRTX
JP4
JP5
Keyboard Lock Jumper
VCC5
R5
VREF
Note : VREF Pull-up to +5V for Game Port Reference
BC1
0.1uF
4 JBB2
4 JBB1
4 JAB2
4 JAB1
4 JBCY
4 JBCX
4 JACY
4 JACX
U1
IT8711F
DSR1#
SOUT1/JP3
SIN1
RTS1#/JP2
DTR1#/JP1
DCD1#
RI1#
CTS1#
PD7
PD6
DSR1# 3
TXD1 3
RXD1 3
RTS1# 3
DTR1# 3
DCD1# 3
RI1# 3
CTS1# 3
PD7 3
PD6 3
3 DCD2#
3 RXD2
3 RI2#
3 CTS2#
3 DTR2#
3 RTS2#
3 DSR2#
3 TXD2
R6
4.7K
R7
4.7K
Pin GA20 & KBRST# connect to South Bridge
GA20
KBRST#
4 KCLK
4 KDAT
4 MCLK
4 MDAT
PWBOUT#
SLPSX#
PWRCTL#
4 VID0
4 VID1
4 VID2
4 VID3
4 VID4
4 MIDI_OUT
4 MIDI_IN
DCD2#/GP62
SIN2/GP63
GND
RI2#/GP10
CTS2#/GP11
DTR2#/GP12
RTS2#/GP13
DSR2#/GP14
SOUT2/GP15
GA20/GP16
KRST#/GP17
KCLK/GP20
KDAT/GP21
MCLK/GP22
MDAT/GP23
PWBTIN#/GP24
PWBTOUT#/GP25
SLPSX#/GP26
PWRCTL#GP27
VID0/GP30
VID1/GP31
VID2/GP32
VID3/GP33
VID4/GP34
GP35
GP36
VCCH
GND
VBAT
KBLK#/CIRTX/GP40
PD5
PD4
GND
PD3
PD2
PD1
PD0
STB#
AFD#
ERR#
INIT#
SLIN#
BUSY
ACK#
SLCT
PE
WPT#
INDEX#
TRK0#
DSKCHG#
RDATA#
DIR#
WGATE#
HDSEL#
STEP#
WDATA#
VCC
GND
CKLIN
DRVA#
VCCH
R8
4.7K
R9
SW1
33
C4
1uF
Power Control Signals.
Please reference Power Control Suggestion Applications Circuitry of page 5.
3VSB
BC3
0.1uF
PC Board Layout Checklist
.Place BC3 close to IT8711F
.Recommended net "3VSB" minimum trace width 12mils
BC2
0.1uF
U2
VCC
NC
OUT
GND
24MHz\OSC
R10
22
DRVA# 4
BAT1
LI-BAT
D1
1N4148
C5
4.7UF/10V
Tantalum cap.
(Spare for battery installation glitch)
JP6
4 CIRRX
4 IRTX
4 IRRX
4 SCPSNT#
4 SCRST
4 SCPWR
4 SCCLK
4 SCIO
CIRRX
IRTX
IRRX
SCPSNT#
SCRST
SCPWR
SCCLK
SCIO
MTRA#
DENSEL#
PCICLK
LAD3
LAD2
LAD1
LAD0
SERIRQ
LRESET#
LFRAME#
LDRQ#
PME#
MTRA# 4
DENSEL# 4
LDRQ#
R11
4.7K
PME#
R12
4.7K
Low Pin Count (LPC) Interface Signals
PC Board Layout Checklist
.Place C3 close to IT8711F
.Recommended net "VBAT" minimum trace width 12mils
.Isolated the VBAT pin29 and Chipset
C3
0.1UF
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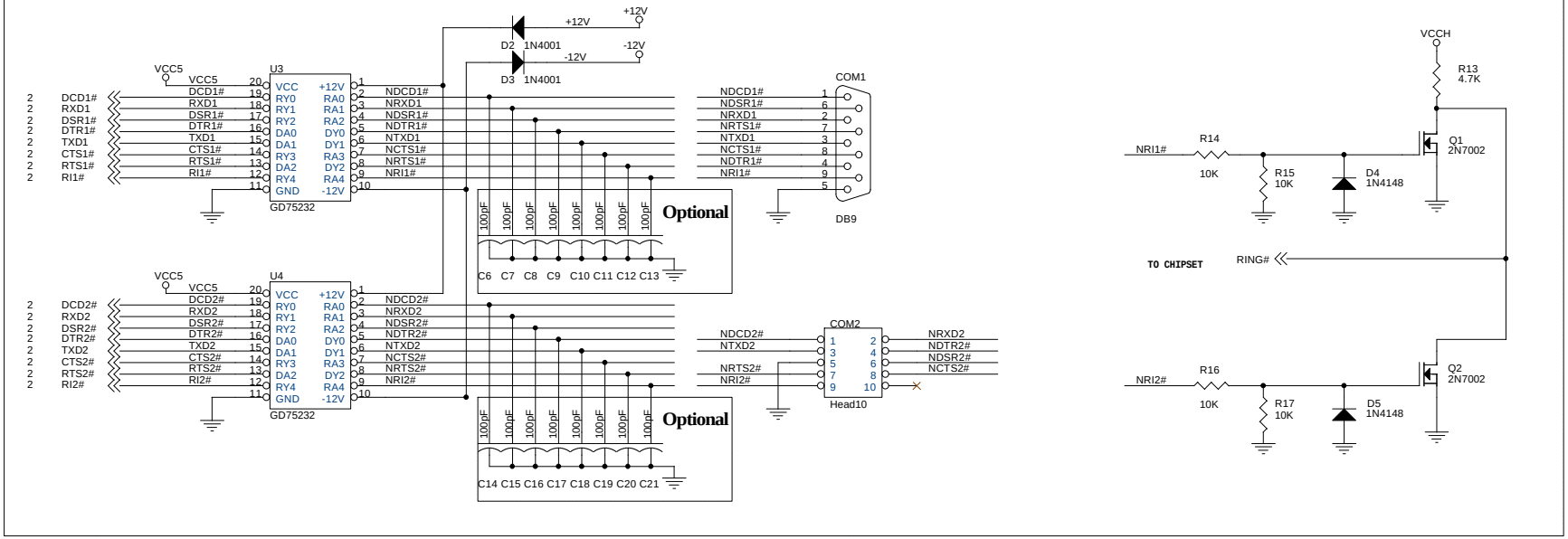
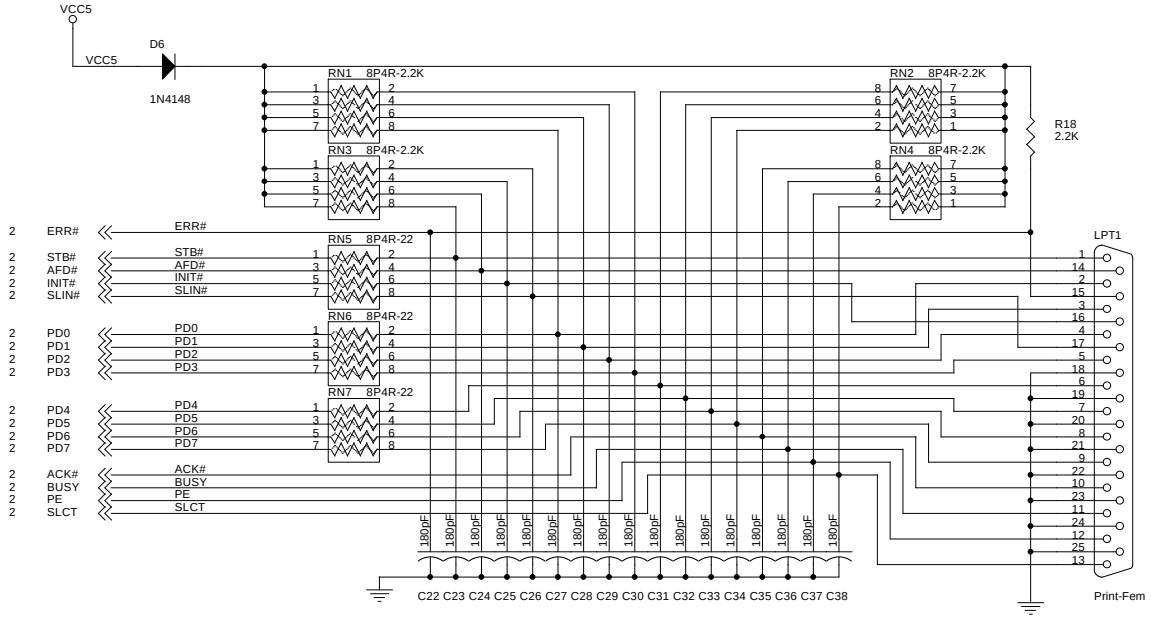
Serial Ports



Parallel Port



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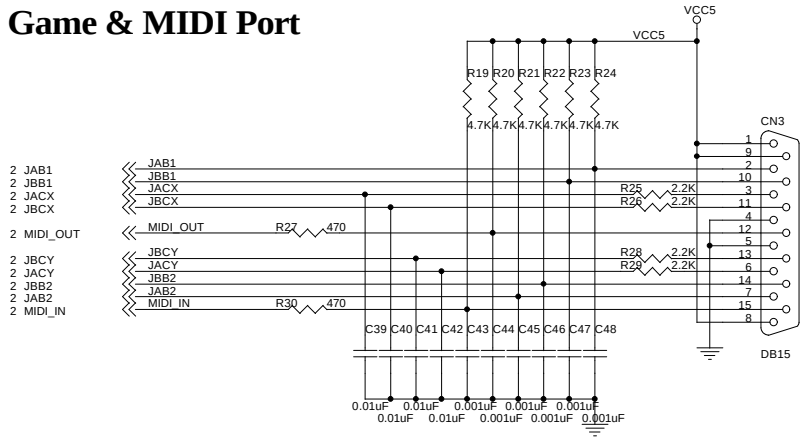
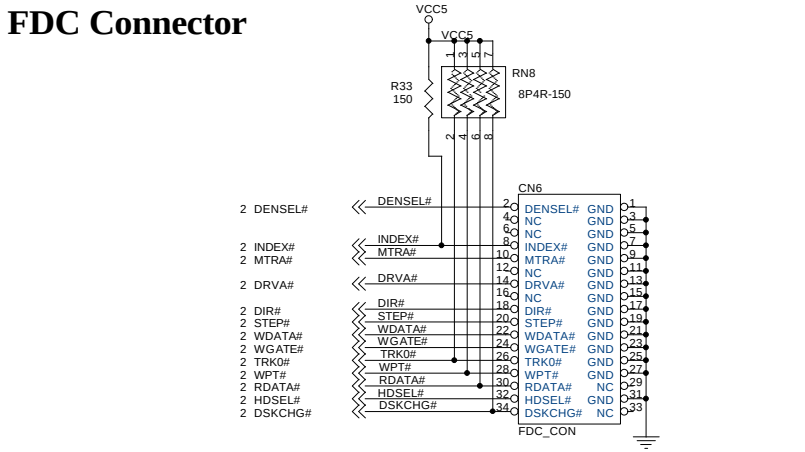
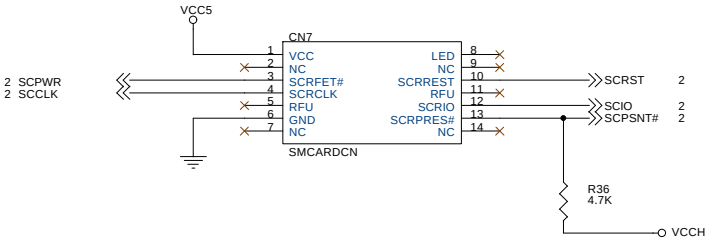
Game & MIDI Port



FDC Connector

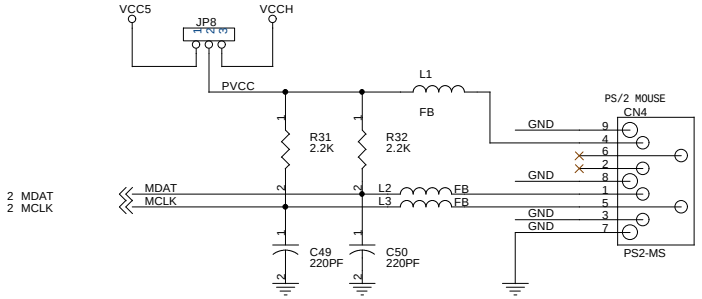


Smart Card Reader Connector

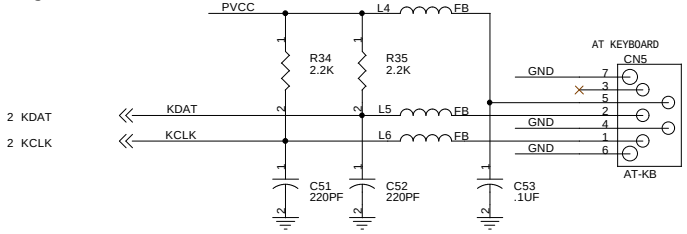


IR & CIR Connector

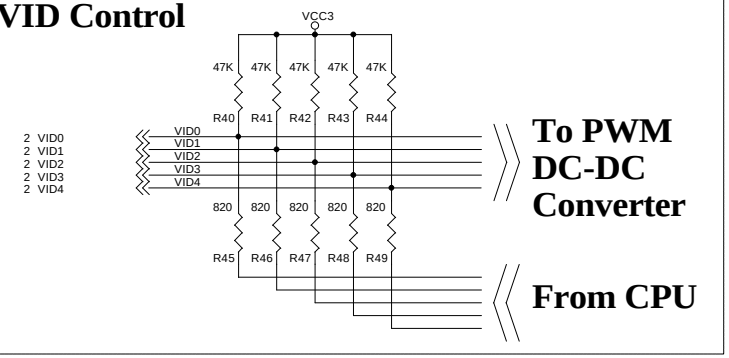
PS/2 Mouse Port



Keyboard Port



VID Control



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LAYOUT/ROUTING GUIDELINES

1.For clock Lines :

1)If possible, please avoid using any through-hole.

2)Please make the trace length short, and the trace width wide enough.

3)The spacing to the closest neighbor should be wide enough.

4)The discrete damping resistors and capacitors are recommended.

5)Please don't share the I/O clock, 24/48MHz, with other device.

2.For the VBAT circuits :

1)Place the 1uF capacitor of VBAT pin close to ITE I/O chip.

2)VBAT should be routed with a minimum trace width of 12 mils.

3)Isolate the VBAT pin of ITE I/O chip from the pin G1/VCCRTC of INTEL's ICH with diode.

4)The 4.7uF/10V tantalum capacitor connected to the diode of battery is spare for battery installation glitches.

3.For the 3VSB circuits :

1)Place the 0.1uF capacitor of pin27 close to ITE I/O chip.

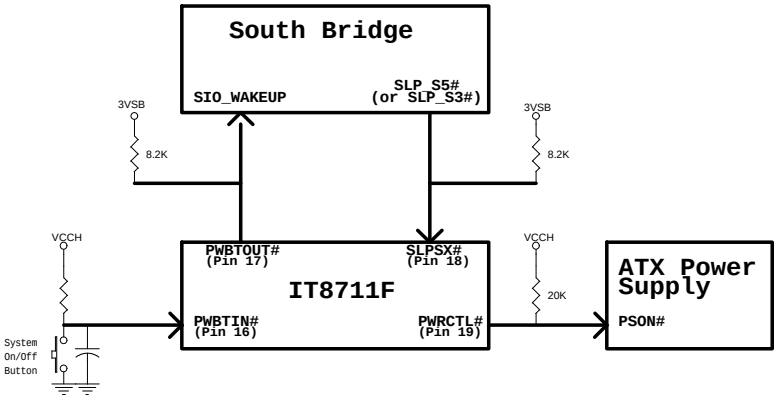
2)3VSB should be routed with a minimum trace width of 12 mils.

4.Please don't remove the pull-up resistor of LDRQ#.

5.Please don't change the resistors and capacitors values in the Game and MIDI circuits.

6. The physical pin layout of Smart Card Reader connector MUST match with the pin arrangement of the 2x7 connector in ITE schematics.

7.IT8711F Power Control Suggestion Applications Circuitry.



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Title: Layout & Routing Guideline		
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