Military Products *Advance Information*

128K x 8 RADIATION-HARDENED STATIC RAM - SOI HX6828

FEATURES

RADIATION

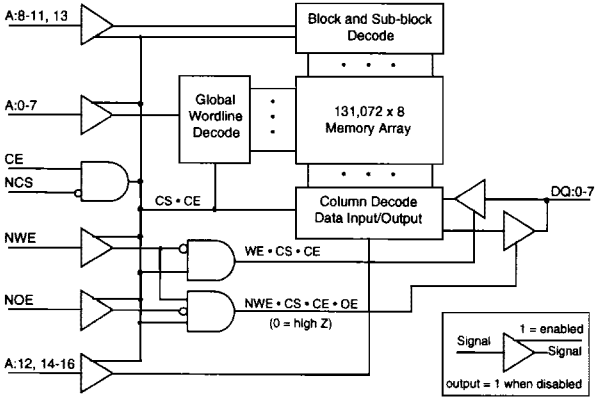
- Fabricated with RICMOS™ Silicon on Insulator (SOI) 0.7 µm Process
- Total Dose Hardness through $1x10^6$ rad(SiO_2)
- Neutron Hardness through $1x10^{14}$ cm^{-2}
- Dynamic and Static Transient Upset Hardness through $1x10^{11}$ rad(Si)/sec
- Soft Error Rate less than $1x10^{-10}$ upsets/bit-day
- Dose Rate Survivability through $1x10^{12}$ rad(Si)/sec
- Latchup Free

OTHER

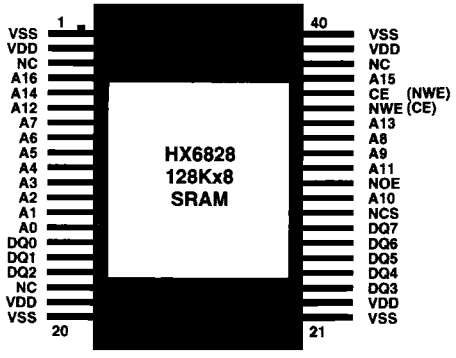
- Full Military Temperature Operation (-55°C to 125°C)
- Access Time ≤ 25 ns
- Low Power Disabled Mode
- Low Operating and Standby Current
- Data Retention down to 2.5 V
- Asynchronous Operation
- CMOS and TTL Compatible I/O
- High Output Drive
- Tri-State Outputs
- Single 5 V ± 10% Power Supply

3

FUNCTIONAL DIAGRAM



PINOUT CONFIGURATION



NC - no connect
(xx) - optional pinout assignment

TRUTH TABLE

CE	NCS	NWE	NOE	MODE	DQ
H	L	H	L	Read	Data Out
H	L	L	X	Write	Data In
H	H	X	XX	Deselected	High Z
L	XX	XX	XX	Disabled	High Z

Notes: X : $V_I = V_{IH}$ or V_{IL} XX: $V_{SS} \leq V_I \leq V_{DD}$

PACKAGE DESIGN

The HX6828 is offered in a custom 40-lead flat pack with a 25-mil pin pitch. The package body is constructed of multilayer ceramic (Al_2O_3) and contains internal signal, power and ground planes to minimize the effect of resistance and inductance, especially in transient radiation environments. Multiple power and ground bonding pads provide for low internal voltage drops in the power busing system. Capacitor pads are located on the package for optional on-package decoupling capacitance.

DC and AC ELECTRICAL CHARACTERISTICS (1,2)

Symbol	Parameter	Min	Max	Units	Test Condition
IDDSB1	Static Supply Current		2.0	mA	VIH/VIL=VDD/VSS IO=0, Inputs Stable
IDDOP	Dynamic Supply Current (Read or Write)		6.5	mA/MHz	All inputs switching
IDDSEI	Static Supply Current per Enabled Input		30	µA/Input	VI=VDD-0.5 V VI=0.5 V
VDR	Data Retention Voltage	2.5		V	NCS=VDR VI=VDR or VSS
IDR	Data Retention Current		500	µA	NCS=VDD=VDR VI=VDR or VSS
VIL_{CMOS}	Low-Level Input Voltage - CMOS Inputs		$0.3*V_{DD}$	V	VDD=4.5V
VIL_{TTL}	Low-Level Input Voltage - TTL Inputs		0.8	V	VDD=4.5V
VIH_{CMOS}	High-Level Input Voltage - CMOS Inputs	$0.7*V_{DD}$		V	VDD=5.5V
VIH_{TTL}	High-Level Input Voltage - TTL Inputs	2.2		V	VDD=5.5V
VOL	Low-Level Output Voltage		0.4 0.1	V	IOL = 10 mA IOL = 20 µA
VOH	High-Level Output Voltage	4.2 VDD-0.1		V	IOH = -5 mA IOH = -20 µA
II	Input Leakage Current	-5	5	µA	VSS≤VI≤VDD
IOZ	Output Leakage Current	-10	10	µA	VSS≤VO≤VDD Output=high Z
TAVQV	Address Access Time - Read (-55 to 125°C)		25	ns	(3)
TAVWH	Address Valid to End of Write Time (-55 to125°C)		25	ns	(3)

(1) For timing diagrams and Absolute Maximum Ratings see the HX6856 data sheet.

(2) Worst case operating conditions: VDD=4.5 V to 5.5 V, TA=-55°C to +125°C, total dose through $1x10^6$ rad(SiO_2) unless noted otherwise

(3) Input levels are VIL/VIH=0.5/VDD-0.5 V (CMOS) or VIL/VIH=0/3 V (TTL), input rise and fall times <5ns, input and output timing reference =VDD/2 V (CMOS) or 1.5 V (TTL), capacitive output loading=50pF

ORDERING INFORMATION

H	X	6828/1	A	S	H	Z	C
SOURCE H=HONEYWELL	**PROCESS** X=SIMOX	**PART NUMBER/ PINOUT OPTION** 1=Std Pinout 2=Optional Pinout	**PACKAGE DESIGNATION** A=40-Lead Flat Pack without capacitors B=40-Lead Flat Pack with capacitors	**SCREEN LEVEL** C=Brass Board S=Modified Class S (1)	**RADIATION HARDNESS** H=1E6 rad(SiO_2)	**SOFT ERROR RATE (2)** Z=<1E-10 upsets/bit-day - = Brass Board	**INPUT BUFFER TYPE** C=CMOS Level

(1) Refer to the HX6856 data sheet for Honeywell screening procedures.
(2) SER spec. indicates worst case, high temperature (125°C), post-total dose performance.

Honeywell

Helping You Control Your World

900098
5/93