GD54/74HC240, GD54/74HCT240

OCTAL INVERTING 3-STATE BUFFERS

General Description

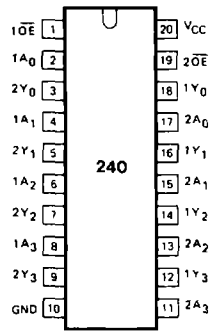
These devices are identical in pinout to the 54/74LS240 They contain eight inverting buffers with two active low enables. Each enable independently controls 4 buffers. These octal inverting buffers/line drivers/line receivers are designed to be used with 3-state memory address drivers, clock drivers, and other bus-oriented systems. Refer to the other devices for similar functionality:

HC/HCT 241 Noninverting, active-low & active-high enables.

HC/HCT 244 Noninverting, active-low enables.

These devices are characterized for operation over wide temperature ranges to meet industry and military specifications.

Pin Configuration



Suffix-Blank Plastic Dual In Line Package
Suffix-J Ceramic Dual In Line Package
Suffix-D Small Outline Package

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 15 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
  for HCT 4.5 to 5.5 olts
- Low input current: 1μA Max.
- Low quiescent current: 80μA Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Function Table

INPUTS		OUTPUT
n$\overline{OE}$	nA_n	nY_n
L	L	H
L	H	L
H	X	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

Logic Diagram

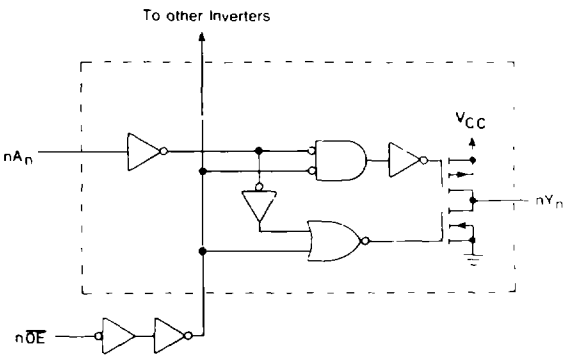


Fig. 1 Logic diagram (one gate)

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{CC}	DC Supply voltage		−0.5	+7	V
I_{IK} I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		|20|	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		|35|	mA
I_{CC}	DC V_{CC} or GND current			|70|	mA
T_{stg}	Storage temperature range		−65	150	°C
P_D	Power dissipation per package	above +70°C: *derate linearly with 8mW/K*		500	mW
T_L	Lead temperature	At distance 1/16 ± 1/32 in from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC		LIMITS MIN	LIMITS MAX	UNITS
Supply-Voltage Range V_{CC}	GD54 74HC Types	2	6	V
	GD54 74HCT Types	4.5	5.5	
DC Input or Output Voltage V_I, V_O		0	V_{CC}	V
Operating Temperature T_A	GD74 Types	−40	+85	°C
	GD54 Types	−55	+125	
Input Rise and Fall times t_r, t_f	GD54 74HC Types at 2V		1000	ns
	at 4.5V		500	
	at 6V		400	
	GD54 74HCT Types at 4.5V		500	

Logic Diagram

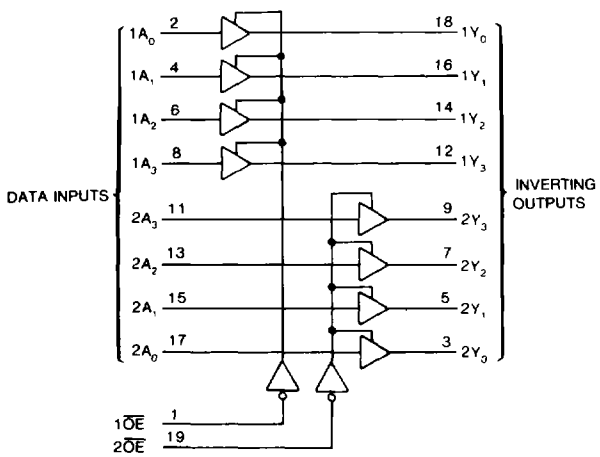


Fig. 2 Logic diagram

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION		V_{CC} (V)	T_A=25°C			GD74HC240		GD54HC240		UNIT
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{IH}	HIGH level input Voltage			2 0 4 5 6 0	1 5 3 15 4 2			1 5 3 15 4 2		1 5 3 15 4 2		V
V_{IL}	LOW level input voltage			2 0 4 5 6 0			0 3 0 9 1 2		0 3 0 9 1 2		0 3 0 9 1 2	V
V_{OH}	HIGH level output voltage	V_{IN}=V_{IH} or V_{IL}	I_{OH}=−20μA	2 0 4 5 6 0	1 9 4 4 5 9	2 0 4 5 6.0		1 9 4 4 5 9		1 9 4 4 5 9		V
			I_{OH}=−6mA I_{OH}=−7 8mA	4 5 6 0	3 98 5 48	4 3 5.2		3 84 5 34		3 7 5 2		
V_{OL}	LOW level output voltage	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2 0 4 5 6 0			0 1 0 1 0 1		0 1 0 1 0.1		0 1 0 1 0 1	V
			I_{OL}=6mA I_{OL}=7 8mA	4 5 6 0		0 17 0.15	0 26 0.26		0 33 0 33		0 4 0 4	
$\|I_{IN}\|$	Input leakage Current	V_{IN}=V_{CC} or GND		6 0			0.1		1 0		1 0	μA
I_{OZ}	Three-State leakage current	V_{IN}=V_{IH} or V_{IL}	V_O=V_{CC} or GND	6 0		0 01	0 5		5 0		10 0	μA
I_{CC}	Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{out}=0μA		6 0			8		80		160	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION		V_{CC} (V)	T_A=25°C			GD74HCT240		GD54HCT240		UNIT
					MIN	TYP.	MAX.	MIN	MAX	MIN	MAX	
V_{IH}	HIGH level input Voltage			4 5 to 5 0	2 0			2 0		2 0		V
V_{IL}	LOW level input voltage			4 5 to 5 5			0 8		0.8		0 8	V
V_{OH}	HIGH level output voltage	V_{IN}=V_{IH} or V_{IL}	I_{OH}=−20μA	4 5	4 4	4 5		4 4		4 4		V
			I_{OH}=−6mA	4 5	3 98	4 3		3 84		3 7		
V_{OL}	LOW level output voltage	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	4 5			0 1		0 1		0 1	V
			I_{OL}=6mA	4 5		0 17	0 26		0.33		0 4	
$\|I_{IN}\|$	Input leakage Current	V_{IN}=V_{CC} or GND		5 5			0 1		1 0		1 0	μA
I_{OZ}	Three-State leakage current	V_{IN}=V_{IH} or V_{IL}	V_O=V_{CC} or GND	5 5		0 01	0.5		5 0		10.0	μA
I_{CC}	Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{out}=0μA		5.5			8		80		160	μA

AC Characteristics for HC: $t_r = t_f = 6ns$ $C_L = 50$ pF

SYMBOL	PARAMETER	V_{CC} (V)	$T_A = 25°C$			GD74HC240		GD54HC240		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} / t_{PHL}	Propagation Delay Time nA_n to nY_n	2.0		30	100		120		140	ns
		4.5		9	18		24		28	
		6.0		8	16		20		25	
t_{PZH}/ t_{PZL}	3-state Output Enable Time $n\overline{OE}$ to nY_n	2.0		36	140		180		210	ns
		4.5		12	28		36		42	
		6.0		10	26		32		36	
t_{PLZ}/ t_{PHZ}	3-state Output Disable Time $n\overline{OE}$ to nY_n	2.0		35	140		180		210	ns
		4.5		10	28		36		42	
		6.0		9	26		32		36	
t_{TLH} / t_{THL}	Output Transition Time	2.0		15	60		75		90	ns
		4.5		6	12		15		18	
		6.0		5	10		13		15	

AC Characteristics for HC: $t_r = t_f = 6ns$ $C_L = 50$ pF

SYMBOL	PARAMETER	V_{CC} (V)	$T_A = 25°C$			GD74HCT240		GD54HCT240		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} / t_{PHL}	Propagation Delay Time nA_n to nY_n	4.5		12	22		26		30	ns
t_{PZH}/ t_{PZL}	3-state Output Enable Time $n\overline{OE}$ to nY_n	4.5		18	30		38		45	ns
t_{PLZ}/ t_{PHZ}	3-state Output Disable Time $n\overline{OE}$ to nY_n	4.5		15	25		32		38	ns
t_{TLH} / t_{THL}	Output Transition Time	4.5		7	12		15		18	ns

AC Waveforms

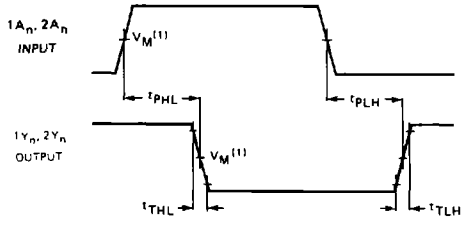


Fig. 3 Waveforms showing the ($1A_n$, $2A_nA$) to output ($1Y_n$, $2Y_n$) propagation delays and the output transition times.

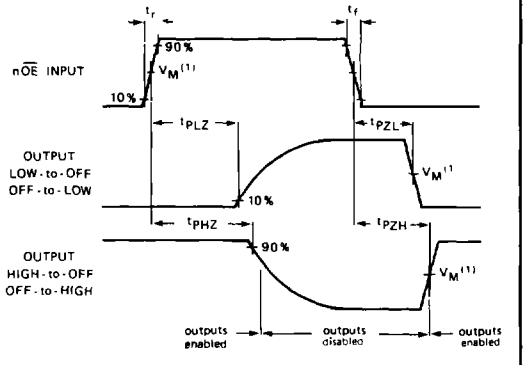


Fig. 4 Waveforms showing the 3-state enable and disable times.