TDC1141 Monolithic Digital To Analog Converter
10 Bit, 50Msps, 12ns Settling Time

The TDC1141 is an ECL compatible, 10-bit monolithic D/A converter capable of converting digital data into an analog current or voltage at data rates in excess of 50 Mega-samples-per second (Msps).

The analog circuitry has been optimized for dynamic performance, with very low glitch energy. The output is able to drive a 50Ω load with 1V output levels while maintaining large spurious-free-dynamic range.

Data registers are incorporated on the TDC1141. This eliminates data skew encountered with external registers and latches and minimizes the glitches that can adversely affect many applications.

Features

- 10-Bit Resolution
- 50 Msps Data Rate
- ECL Inputs
- Very Low Glitch With No Track And Hold Circuit Needed
- Dual +4dBm (1V Into 50Ω) Outputs Make Output Amplifiers Unnecessary In Many Applications

Applications

- Direct Digital RF Signal Generation
- Test Signal Generation
- Arbitrary Waveform Synthesis
- Broadcast And Studio Video
- High-Resolution A/D Converters

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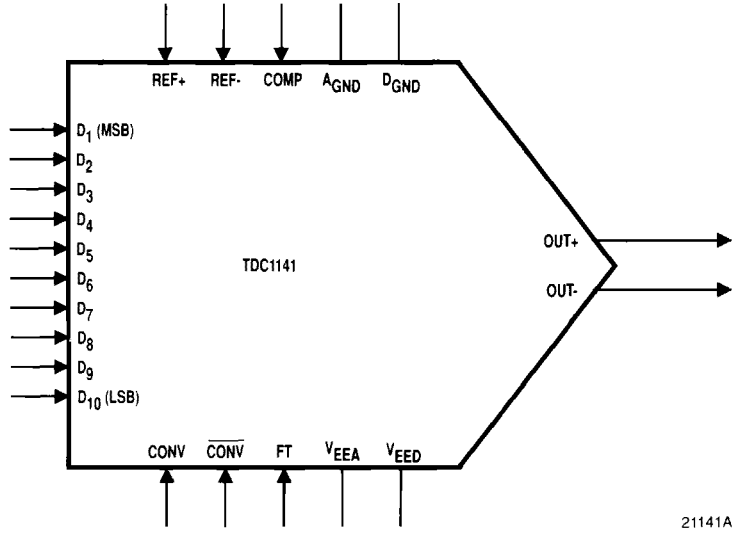
Interface Diagram



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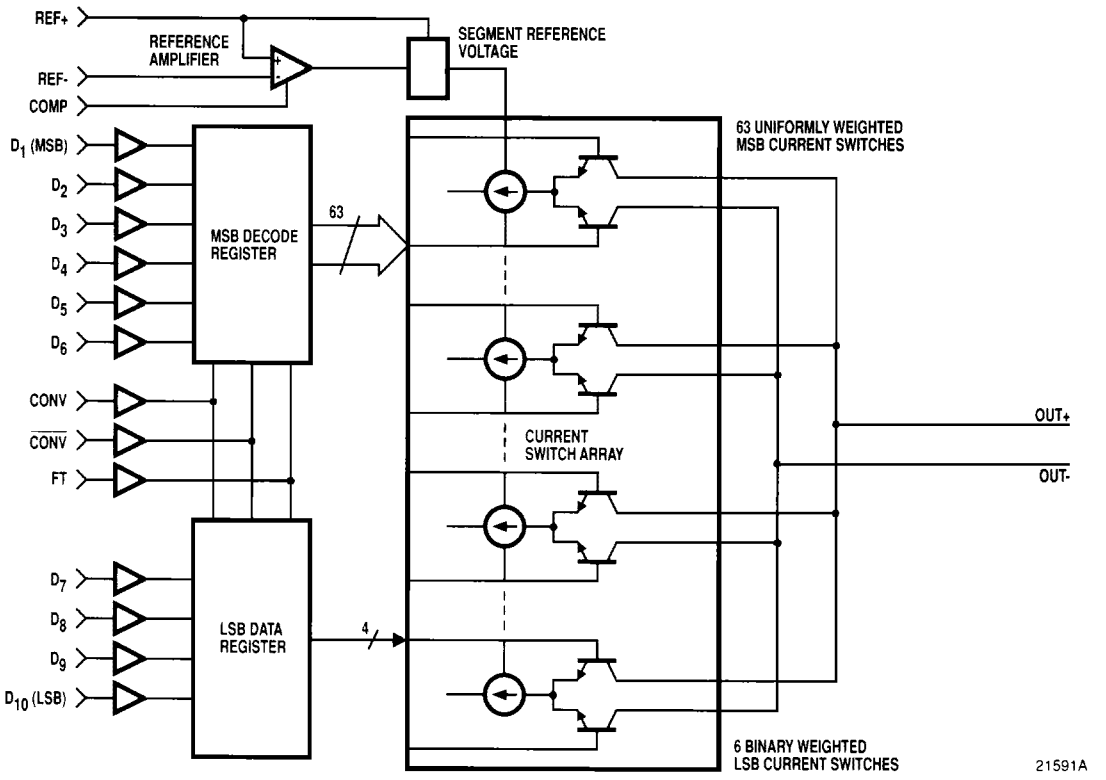
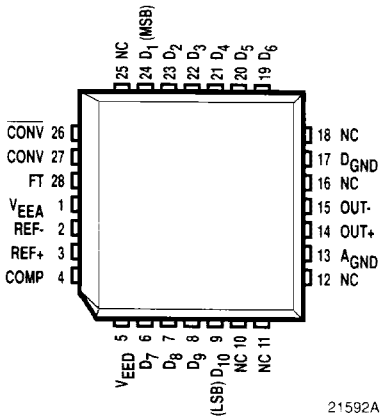
Functional Block Diagram



Pin Assignments



28 Leaded Plastic Chip Carrier – R3

Functional Description

General Description

The TDC1141 consists of five major circuit sections: the LSB data register, the MSB decode block, the decoded MSB register, the current switch array, and the reference amplifier. All data bits are registered just before the current switches to minimize the temporal skew that would generate glitches.

Power and Grounds

The TDC1141 requires a single –5.2V power supply. This supply is divided into analog (V_{EEA}) and digital (V_{EED}) supply pins which should be decoupled from each other. An example of this decoupling is shown in the *Typical Interface Circuit*. The 0.1µF decoupling capacitors should be placed as close as possible to the power pins. The

inductors are simple ferrite beads and are neither critical in value nor always required.

Reference and Compensation

The TDC1141 has two reference inputs: REF+ and REF–. These are the inverting and noninverting inputs of the internal reference amplifier. An externally generated reference voltage is applied to the REF– pin. Current flows into the REF+ pin through an external current setting resistor (R_{REF}). This current is the reference current (I_{REF}) which serves as an internal reference for the current source array. The output current for an input code N from OUT+ is related to I_{REF} through the following relationship:

$$I_{OUT} = N \times \frac{I_{REF}}{16}$$

Where N is the input code to the D/A converter

This means that with an I_{REF} that is nominally 625μA, the full-scale output is 40mA, which will drive a 50Ω load in parallel with a 50Ω transmission line (25Ω load total) with a 1V peak to peak signal. The impedance seen by the REF– and REF+ pins should be approximately equal so that the effect of amplifier input bias current is minimized.

The internal reference amplifier is externally compensated to ensure stability. A 0.1μF capacitor should be connected between the COMP pin and V_{EEA}.

Digital Inputs

All digital inputs including the FT, CONV and Data Inputs are compatible with ECL logic. Input registers are provided on the data input lines to minimize the effect of glitching caused by data skew.

Clock and Feedthrough Control

The TDC1141 requires a differential ECL clock signal (CONVert and $\overline{\text{CONV}}$ert). Even though complementary operation is preferred, a single-ended signal may be used if either unused CONV input is biased at a DC voltage midway between the active input's V_{IH} and V_{IL} levels.

Data is synchronously entered on the rising edge of CONV (the falling edge of $\overline{\text{CONV}}$). The CONV input is ignored in the Feedthrough (FT = HIGH) mode.

The Feedthrough (FT) pin is normally held LOW, in which case the TDC1141 operates in a clocked mode (the output changes only after a clock rising edge). An internal pull-down resistor is provided, and this pin may be left open for clocked operation. For certain applications, such as high-precision successive approximation A/D converters, output delay may be more important than glitch performance. In these cases, the FT pin may be brought HIGH, which makes the input registers transparent. This allows the analog output to change immediately and asynchronously in response to the digital input, without the need for a clock.

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Analog Outputs

Two simultaneous and complementary analog outputs are provided. Both of these outputs are full-power current sources. By loading the current source outputs with a resistive load, they may be used as voltage outputs. OUT+ provides a 0 to –40mA output current (0 to –1V when terminated in 25Ω) as the input code varies from 00 0000 0000 to 11 1111 1111. OUT– varies in a complementary manner from –40 to 0mA (–1 to 0V when terminated with 25Ω) over the same code range. (See the *Input Coding Table*.) The output current is proportional to the reference current and the input code.

No Connect

These pins have no internal connection and should be left open for optimal performance.

Package Interconnections

Signal Type	Signal Name	Function	Value	R3 Package Pins
Power	A_{GND}	Analog Ground	0.0V	13
	D_{GND}	Digital Ground	0.0V	17
	V_{EEA}	Analog Supply Voltage	–5.2V	1
	V_{EED}	Digital Supply Voltage	–5.2V	5
Reference	REF–	Reference Voltage Input	–1.0V	2
	REF+	Reference Current Input	–625µA	3
	COMP	Compensation Capacitor	0.1µF, see text	4
Data Inputs	D_1 (MSB)	Most Significant Bit	ECL	24
	D_2		ECL	23
	D_3		ECL	22
	D_4		ECL	21
	D_5		ECL	20
	D_6		ECL	19
	D_7		ECL	6
	D_8		ECL	7
	D_9		ECL	8
	D_{10} (LSB)	Least Significant Bit	ECL	9
Feedthrough	FT	Feedthrough Mode control	ECL	28
Convert	CONV	Convert (Clock) Input	ECL	27
	$\overline{CONV}$	Convert Complement	ECL	26
Analog Output	OUT+	Analog Output	0 to 40mA	14
	OUT–	Analog Output	40 to 0mA	15
No Connect	NC	No Internal Connection	Open	10,11,12,16,18,25

Input Coding Table[1]

Input Data MSB LSB	OUT+ (mA)	V_{OUT+}(mV)	OUT– (mA)	V_{OUT-}(mV)
00 0000 0000	0.000	0.00	40.000	–1000.00
00 0000 0001	0.039	–0.97	39.961	–998.05
00 0000 0010	0.078	–1.95	39.922	–998.05
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
0111 1111 11	19.961	–499.03	20.000	–500.00
1000 0000 00	20.000	–500.00	19.961	–499.03
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
1111 1111 01	39.922	–998.05	0.078	–1.95
1111 1111 10	39.961	–999.03	0.039	–0.97
1111 1111 11	40.000	–1000.00	0.000	0.0

Note: 1. I_{REF} = 625µA, R_{LOAD} = 25Ω

Figure 1. Timing Diagram

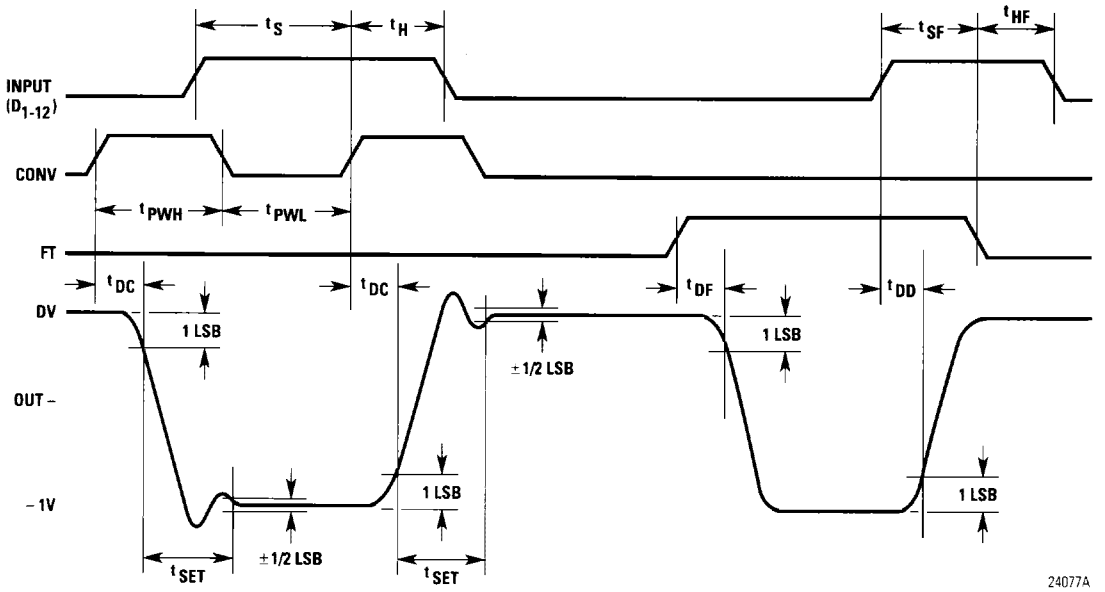

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Figure 2. Equivalent Input Circuit (Data and FT)

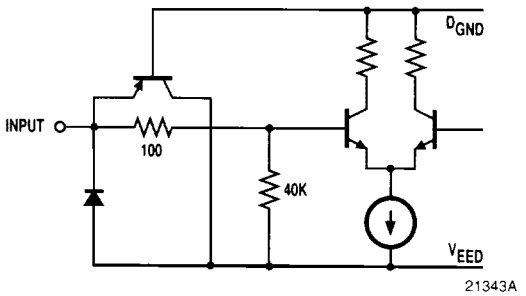


Figure 3. Equivalent Input Circuit (CONV and $\overline{\text{CONV}}$)

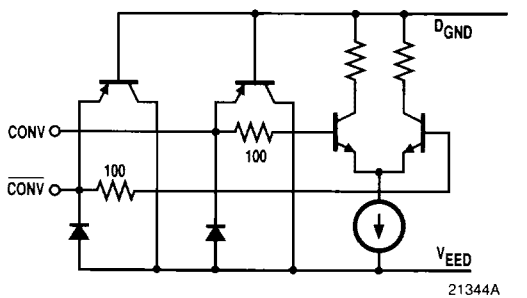


Figure 4. Equivalent Reference and Output Circuits

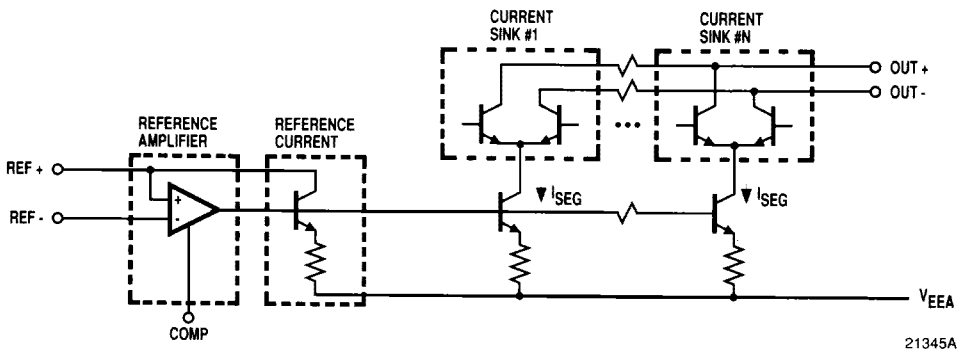


Figure 5. Standard Test Load

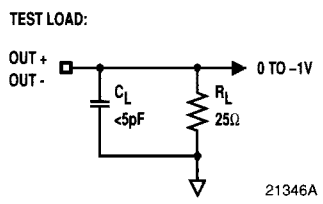
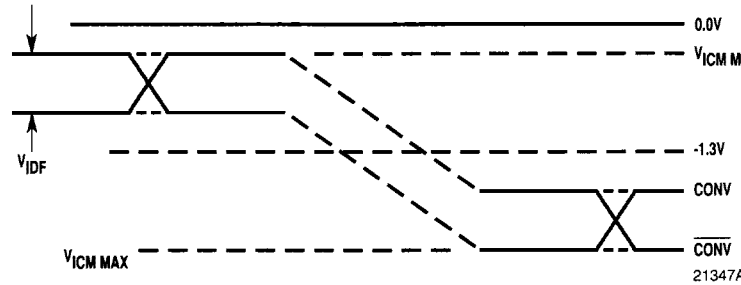


Figure 6. CONV and $\overline{CONV}$ Switching Levels



Absolute maximum ratings (beyond which the device may be damaged)[1]

Supply Voltages

V_{EEA}	(Measured to A_{GND})	−7.0 to +0.5V
V_{EEA}	(Measured to V_{EED})	−50 to +50mV
V_{EED}	(Measured to D_{GND})	−7.0 to +0.5V
A_{GND}	(Measured to D_{GND})	−0.5 to +0.5V

Inputs

CONV, $\overline{CONV}$, FT, $D_{1\text{-}12}$ (Measured to D_{GND})[2]	V_{EED} to +0.5V
REF+, REF-, Applied Voltage (Measured to A_{GND})[2]	V_{EEA} to +0.5V
REF+, REF−, Current, Externally Forced[3,4]	±3mA

Outputs

OUT+, OUT−, Applied Voltage (Measured to A_{GND})[2]	−2.0 to +2.0V
OUT+, OUT−, Current, Externally Forced[3,4]	+50mA
Short-Circuit Duration (Single Output to GND)	unlimited

Temperature

Operating, ambient	
(Plastic Package)	−20 to +90°C
(Ceramic Package)	−60 to +150°C
Junction	
(Plastic Package)	+140°C
(Ceramic Package)	+200°C
Lead, Soldering (10 Seconds)	+300°C
Storage	−65 to +150°C

Notes:
1. Absolute maximum ratings are limiting values applied individually while other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied. Device performance and reliability are guaranteed only if the Operating Conditions are not exceeded.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter		Temperature Range: Standard Min	Standard Nom	Standard Max	Units
F_S	Clock Frequency	0		50	Msps
V_{EED}	Negative Supply Voltage (Measured to D_{GND})	–4.9	–5.2	–5.5	V
V_{EEA}	Negative Supply Voltage (Measured to A_{GND})	–4.9	–5.2	–5.5	V
V_{AGND}	Analog Ground Voltage (Measured to D_{GND})	–0.1	0.0	0.1	V
V_{EEA}	Negative Supply Voltage (Measured to V_{EED})[1]	–20	0	20	mV
t_{PWL}	CONV Pulse Width LOW ($F_S \geq 40$ Msps)	10.5			ns
	CONV Pulse Width LOW ($F_S < 40$ Msps)	11			ns
t_{PWH}	CONV Pulse Width HIGH ($F_S \geq 40$ Msps)	8			ns
	CONV Pulse Width HIGH ($F_S < 40$ Msps)	9			ns
t_S	Setup Time, Data to CONV	17			ns
t_H	Hold Time	0			ns
t_{SF}	Setup Time, Data to FT	7			ns
t_{HF}	Hold Time, Data to FT	24			ns
V_{IL}	Input Voltage, Logic LOW			–1.55	V
V_{IH}	Input Voltage, Logic HIGH	–1.05			V
V_{REF}	Reference Voltage (REF–)	–0.7	–1.0	–1.3	V
I_{REF}	Reference Current (REF+)	400	625	700	µA
C_C	Compensation Capacitor	0.01	0.1		µF
T_A	Ambient Temperature, Still Air	0		70	°C

Note: 1. A common power supply isolated with ferrite bead inductors is recommended for V_{EEA} and V_{EED}. This is shown in the *Typical Interface Circuits*.

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range: Standard Min	Standard Max	Units
$I_{EEA}+I_{IEED}$		$V_{EEA}=V_{EED}$=Max,static T_A=0 to 70°C		–180	mA
		T_A=70°C		–150	mA
C_{REF}	Reference Input Capacitance			15	pF
C_I	Digital Input Capacitance			15	pF
V_{OC}	Compliance Voltage		–1.2	1.2	V
R_O	Output Resistance		12		kΩ
C_O	Output Capacitance			45	pF
I_O	Full-Scale Output Current	I_{REF}=625µA	40		mA
I_{IL}	Input Current, Logic LOW	V_{EE}=Max, V_I=0.4V	–10	200	µA
I_{IH}	Input Current, Logic HIGH	V_{EE}=Max, V_I=2.4V	–10	200	µµA

Switching characteristics

Parameter		Test Conditions	Temperature Range (Standard) Min	Typ	Max	Units
t_{DC}	Clock to Output Delay	V_{EEA}, V_{EED}=Min, FT=LOW			20	ns
t_{DD}	Data to Output Delay	V_{EEA}, V_{EED}=Min, FT=HIGH			25	ns
t_{DF}	FT to Output Delay	V_{EEA}, V_{EED}=Min			30	ns
t_R	Risetime[1]	90% to 10% of FSR, FT=LOW		2	4	ns
t_F	Falltime[1]	10% to 90% of FSR, FT=LOW		2	4	ns
t_{SET}	Settling Time, Voltage	FT=LOW, Full-Scale Voltage transition on I_{OUT} to 0.1% FSR		12	20	ns

Note 1. Clocked Mode

System performance characteristics

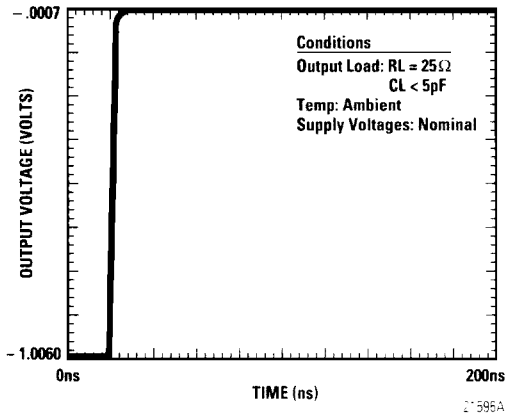
Parameter		Test Conditions	Temperature Range (Standard) Min	Typ	Max	Units
E_{LD}	Differential Linearity Error	V_{EEA}, V_{EED}, I_{REF} = Nom[1]				
		TDC1141			±0.1	%
		TDC1141-1			±0.05	%
E_{LI}	Integral Linearity Error	V_{EEA}, V_{EED}, I_{REF} = Nom[1]				
		TDC1141			±0.1	%
		TDC1141-1			±0.05	%
V_{OS}	REF+ to REF– Offset Voltage		–10		+10	mV
I_B	REF- Input Bias Current			5	µA	
E_G	Absolute Gain Error	V_{EEA}, V_{EED}, I_{REF} = Nom	–5		5	%
I_{OF}	Output Offset Current	V_{EEA}, V_{EED}= Max, D_{1-12} = LOW	–5		+5	µA
PSRR	Power Supply Rejection Ratio	V_{EEA}, V_{EED}, I_{REF} = Nom[2]			–50	dB
PSS	Power Supply Sensitivity	V_{EEA}, V_{EED} = ±4%, I_{REF} = Nom			–140	µA/V
G_A	Peak Glitch Area				40	pV– sec

Note 1. OUT– connected to A_{GND}, OUT+ driving virtual ground

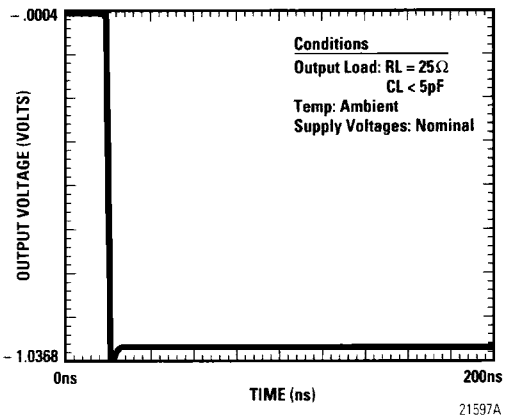
2. 120Hz, 600mV p-p ripple on V_{EE} and V_{CC}

Typical Performance Curves (Typical Settling Time Characersitics)

A. Full-Scale Output Transition, Rising Edge



B. Full-Scale Output Transition, Falling Edge



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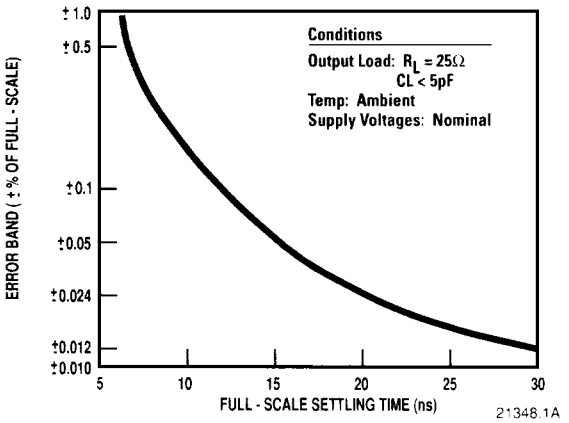
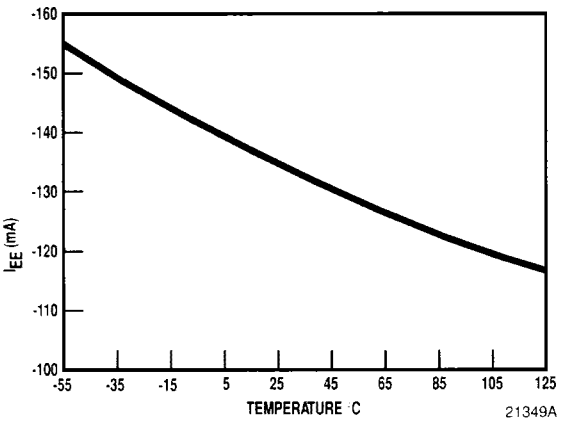
C. Typical Settling Time vs. Settling Accuracy



D. Typical Supply Current vs. Temperature



Applications Information

There are three major D/A architectures: segmented, weighted current sources, and R-2R. In segmentated D/A converters there is one current source for each possible output level. The current sources are equally weighted and for an input code of N, N current sources are turned on. An N bit segmented D/A has 2^N current sources. A weighted current source D/A has one current source for each bit of input with a binary weighting for the current sources. In an R-2R D/A, there is one current source per bit, and a resistor network which scales the current sources to have a binary weighting.

When transitioning from a code of 0111111111 to 1000000000, both the R-2R D/A and Binary weighted D/A are turning some current sources on while turning others off. If the timing is not perfect, there is a moment where all current sources are either on or off, resulting in a glitch. In a segmented architecture, 511 of the current sources remain on, and one more is turned on to increment the output with no possibility of a glitch.

The TDC1141 uses a hybrid architecture with the 6 MSBs segmented, and the 4 LSBs from a R-2R network. The result is a converter which has very low glitch energy, and a moderate die size.

Layout, Power and Grounding

The layout of grounds in any system is an important design consideration. Separate analog and digital grounds are provided on the TDC1141. All ground pins should be connected to a common low-noise, low-impedance groundplane. This groundplane should be common for the TDC1141 and all of its immediate interface circuitry, which includes all of the reference circuitry, the output load circuitry, and all of the power supply decoupling components.

The digital driving logic should use a separate system ground, and this ground should be connected (typically through a ferrite bead inductor) to the analog groundplane in only one place. The analog and digital grounds may be connected in other ways if required by the user's system grounding plan, however, the voltage differential between the A_{GND} and D_{GND} pins must be held to within ±0.1 Volt.

Output Termination

The recommended output termination is 25Ω. This can be provided by placing a 50Ω source resistor between the output pin and ground, then driving a 50Ω transmission line. With this load, the output voltage range of the converter is 0 to −1.0V. If a load is capacitively coupled to the TDC1141, it is recommended that a 25Ω load at DC, as seen by the TDC1141, continue to be maintained. The output voltage should be kept within the output compliance voltage range, V_{OC}, as specified in the ***Electrical Characteristics Table***, or the accuracy may be impaired.

See ***Figure 8*** for a suggested circuit for achieving a bipolar output voltage range. Optimum DC linearity is obtained by using a differential output either with a balun, or an operational amplifier in the differential mode. If it is desired that the TDC1141 be operated in a single ended fashion, the unused output should be connected directly to ground as is shown in ***Figure 9***. The CONV signal provided to the TDC1141 must be as free from clock jitter as possible. Clock jitter is the random cycle-to-cycle variation in clock period. CONV clock jitter will effectively appear at the output as phase noise. A value of 10ps or less for clock jitter is recommended for the highest performance applications. Ordinary crystal oscillators are satisfactory. High-performance synthesizers, such as the HP8662, used to trigger a precision pulse generator, are also satisfactory, although not as jitter free as a crystal oscillator.

Driving a 75Ω Transmission line

The TDC1141 has been optimized to operate with a reference current of 625μA. Significantly increasing or decreasing this current may degrade the performance of the device. If it is desired that the device drive a 37.5Ω load (75Ω source termination driving 75Ω transmission line) rather than the 25Ω suggested load, then V_{REF} should be held at 1V and I_{REF} reduced to 417μA. This will result in a 1V p-p voltage being generated at the DAC output.

Figure 7. Typical Interface Circuit with Balun Output

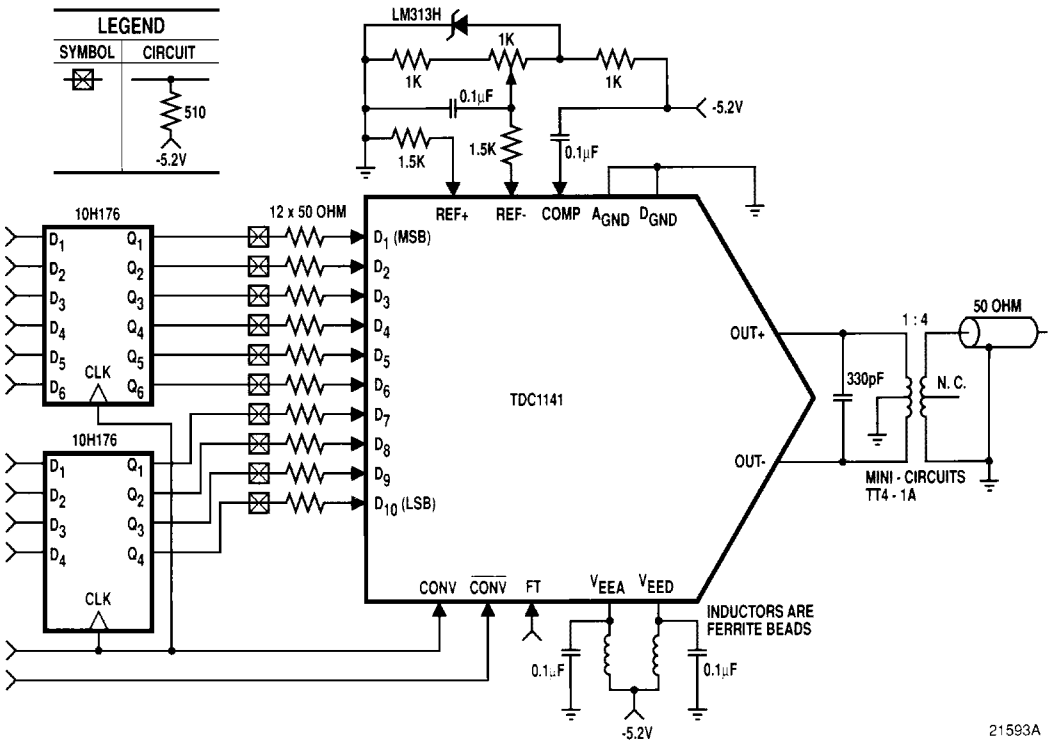


Figure 8. Typical Interface Circuit with Bipolar, Differential Mode Operational Amplifier Output

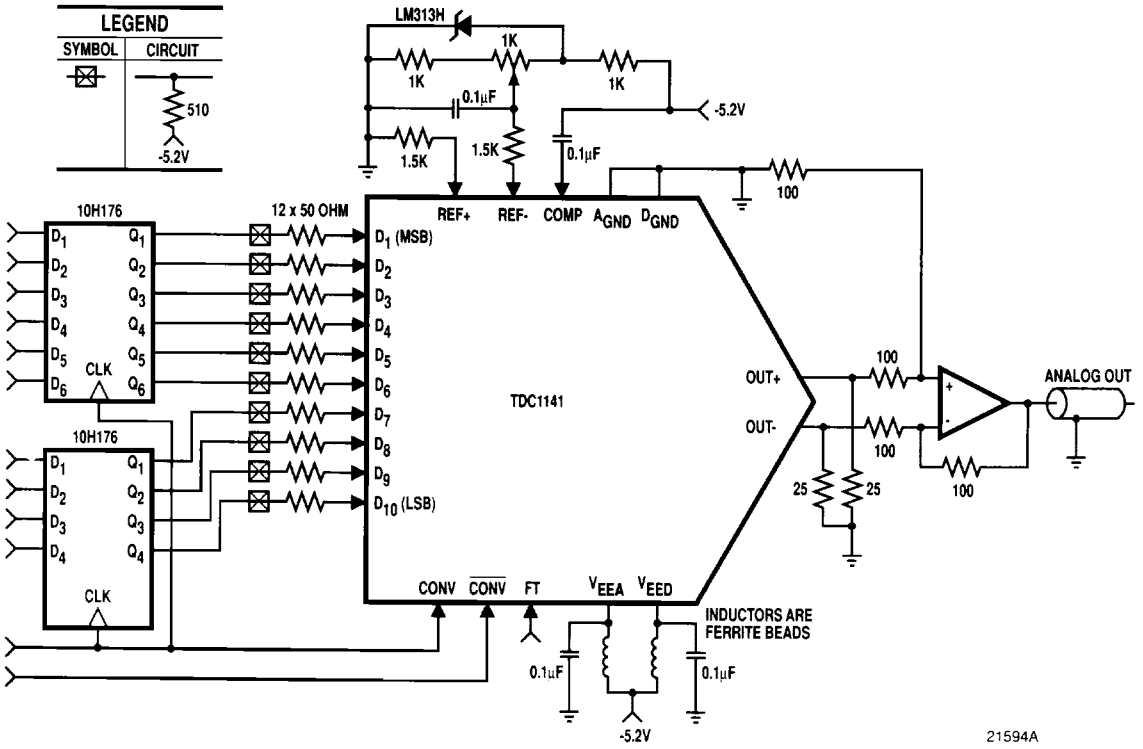
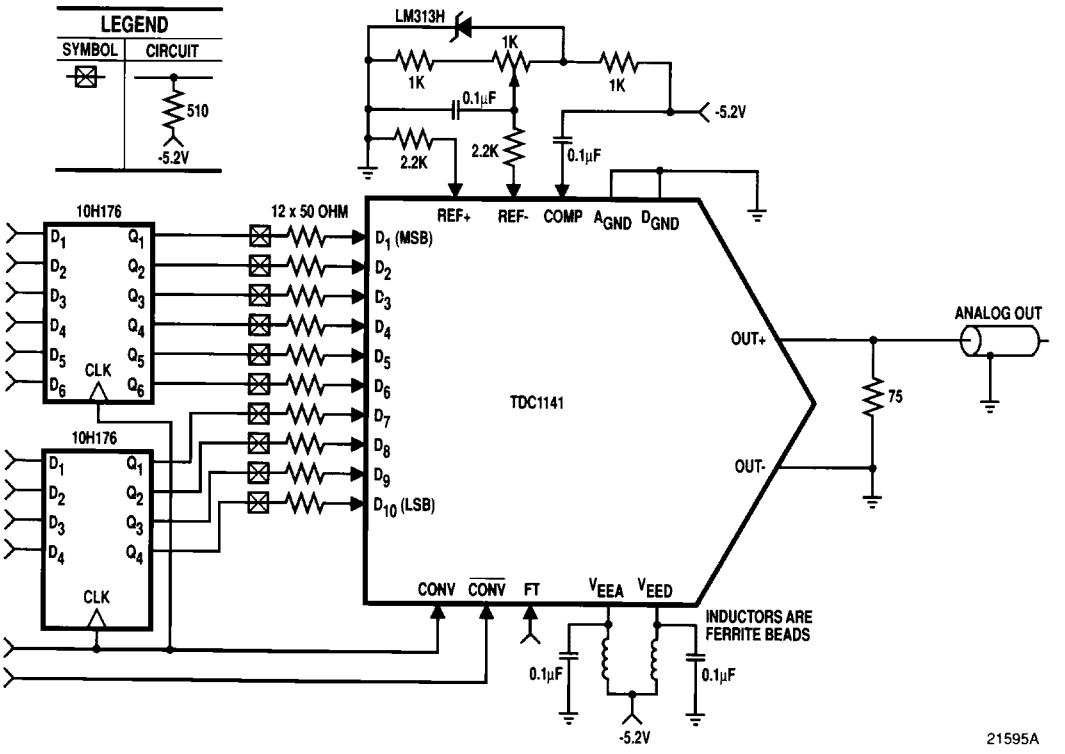


Figure 9. Typical Interface Circuit with Resistive Load Output



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Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TDC1141R3C	T_A=0°C to 70°C	Commercial	Plastic Chip Carrier	1141R3C
TDC1141R3C1	T_A=0°C to 70°C	Commercial	Plastic Chip Carrier	1141R3C-1