High-Speed CMOS 64Kx4 SRAM with Separate I/O

QS86444
QS86449
ADVANCE INFORMATION

FEATURES/BENEFITS

- High Speed Access and Cycle times
- 15ns/20ns/25ns Commercial
- 20ns/25ns/35ns Military
- TTL compatible I/O
- Low Standby current
- 6-Transistor cell for high reliability
- Ideal for reliable,dense memory systems
- Available in 28-pin DIPs, 28-pin 300 mil
- Low power, high-speed QCMOS™ technology
- Military product compliant to MIL-STD-883

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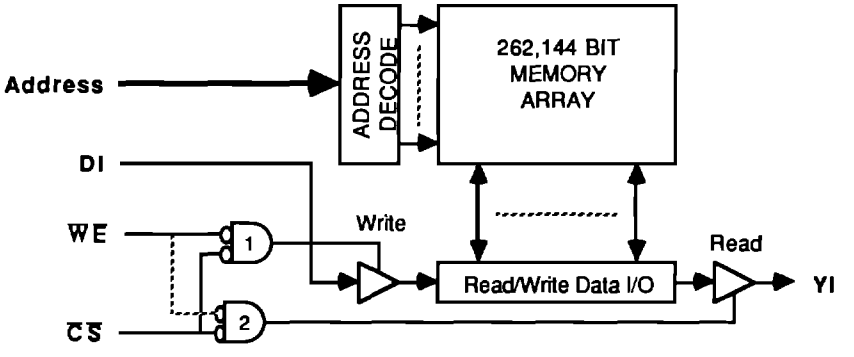
DESCRIPTION

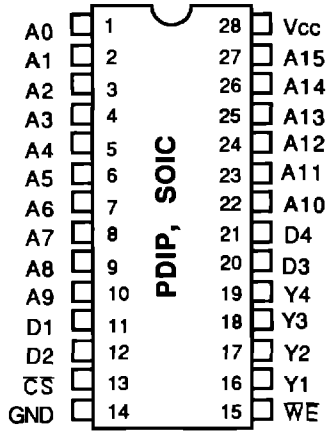
The QS86444 and QS86449 are high-speed 256K SRAMs organized as 64Kx4 with separate read and write data buses. In the 86444, the read data outputs follow the inputs during a write; in the 86449, the outputs are disabled during a write. The 86444 and 86449 are manufactured in a high-performance CMOS process, and they are based on a 6-transistor cell design for high reliability of data retention. Their high-speed access times make them useful in cache data RAM, cache tag RAMs, high-speed scratchpad memories, look-up tables, pipelined DSP and bit-slice systems. Low operating power and excellent latch-up and ESD protection are provided.

FUNCTIONAL BLOCK DIAGRAM



Note:
WE is not connected to Output Enable Gate 2 in the 86444.
WE is connected to Output Enable Gate 2 as shown in the 86449.

PIN CONFIGURATIONS



ALL PINS TOP VIEW