8K x 8 RADIATION-HARDENED STATIC RAM HC6364

FEATURES

RADIATION

- Fabricated using DESC Approved QML 1.2 μm RICMOS™ Process
- Total Dose Hardness through $1x10^6$ rad(SiO_2)
- Neutron Hardness through $1x10^{14}$ cm^{-2}
- Dynamic and Static Transient Upset Hardness through $1x10^9$ rad(Si)/s
- Soft Error Rate Range of $1x10^{-6}$ to $1x10^{-10}$ upsets/bit-day (80°C)
- Dose Rate Survivability through $1x10^{12}$ rad(Si)/s
- Latchup Free

OTHER

- Listed on SMD #5962-38294. Available as MIL-I-38535 QML Class Q and Class V
- Access Time of 25 ns (typical) < 55 ns worst case (-55 to 125 °C)
- Standby Current < 20 μA at 80°C
- Data Retention Mode down to 2.5V
- Asynchronous or Synchronous Operation
- TTL or CMOS Level Input Option
- 36-Pin Flat Pack (0.630 in. x 0.630 in.)
- 28-Pin DIP (MIL-STD-1835, D-10)
- JEDEC Compatible Pin Ordering

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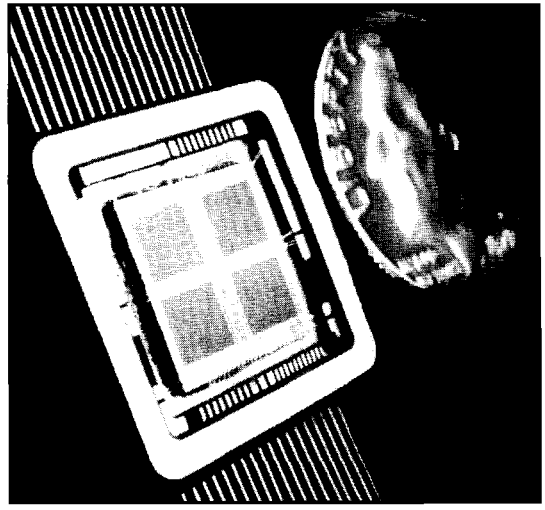
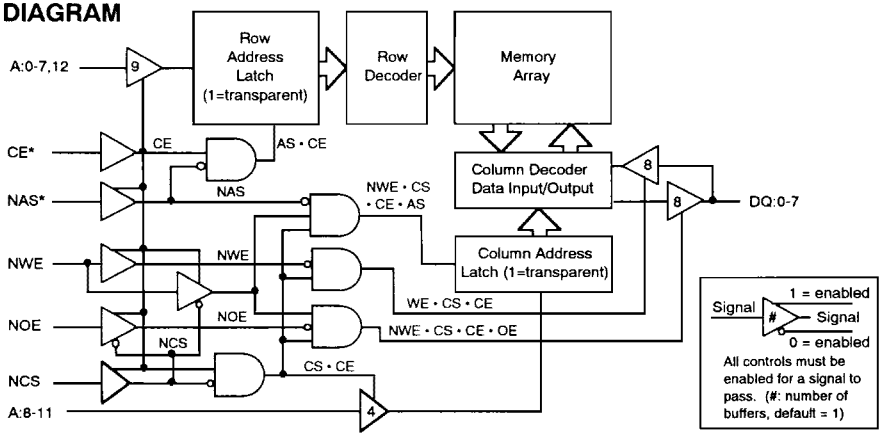
GENERAL DESCRIPTION

The 8K x 8 Radiation-Hardened Static RAM is a high performance 8192 x 8-bit static random access memory with industry-standard functionality. It is fabricated with Honeywell's radiation-hardened CMOS technology, and is designed for use in systems operating in radiation environments. The RAM operates over the full military temperature range and requires only a single 5 V ± 10% power supply. Input levels can be ordered for either TTL or CMOS compatibility. Power consumption is typically 40 mW/MHz in operation, and 5 μW/MHz in the low power disabled mode. The RAM read operation is fully asynchronous, with an associated typical access time of 25 ns.



Honeywell's enhanced RICMOS™ (Radiation Insensitive CMOS) technology is radiation hardened through the use of advanced and proprietary design, layout, and process hardening techniques. The RICMOS™ process is a 5-volt, n-well CMOS technology with a 250 Å gate oxide and a minimum feature size of 1.2 μm. Additional features include two layers of interconnect metalization, a lightly doped drain (LDD) structure for improved short channel reliability, and an epitaxial starting material for latchup-free operation. High resistivity cross-coupled polysilicon resistors have been incorporated for single event upset hardening.

FUNCTIONAL DIAGRAM



SIGNAL DEFINITIONS

A: 0-12 Address input pins (A) which select a particular eight-bit word within the memory array

DQ: 0-7 Bidirectional data pins which serve as data outputs during a read operation and as data inputs during a write operation

NCS Negative chip select, when at a low level, allows a read or write operation. When at a high level it forces the SRAM to a precharge condition and holds the data output drivers in a high impedance state. The input circuits for input pins DQ: 0-7, NOE and A: 8-11 are disabled. The signal propagation path on the remaining enabled inputs is gated off to reduce power, but will contribute DC IDD chip current (IDDSEI) if their input pins are not at VDD or VSS levels. If this signal is not used it must be connected to VSS.

NWE Negative write enable, when at a low level, activates a write operation and holds the data output drivers in a high impedance state. When at a high level, it allows normal read operation.

NOE Negative output enable at a high level holds the data output drivers in a high impedance state. When at a low level, data output driver state is defined by NSC, NWE and CE. If this signal is not used it must be connected to VSS.

NAS* Negative address strobe, when at a low level, maintains on chip address latches in a transparent state allowing the loading of address inputs. When at a high level, it latches the loaded address state. If this signal is not used it must be connected to VSS. NAS can be connected to NCS during normal operation.

CE* Chip enable at a high level allows normal operation. When at a low level it forces the array to a precharge condition, disables the input circuits on all other input pins and holds the data output drivers in a high impedance state. The dynamic and DC IDD chip current contribution from all other input circuits caused by input pins transitioning and/or not at VDD or VSS levels is eliminated. If this signal is not used it must be connected to VDD.

TRUTH TABLE

NCS	CE*	NWE	NOE	NAS*	MODE	DQ
L	H	H	L	X	Read	Data Out
L	H	L	X	X	Write	Data In
H	H	X	XX	X	Deselected	High Z
XX	L	XX	XX	XX	Disabled	High Z

* Optional pinouts. NAS only available in 36-lead flat pack.

Notes
X: VI=VIH or VIL
XX: VSS≤VI≤VDD
NAS=L: Address latches are transparent.
NAS=H: Address latches are closed.
NOE=H: High Z output state maintained for NCS=X, CE=X, NWE=X, or NAS=X.

RADIATION-HARDENED CHARACTERISTICS

Total Ionizing Radiation Dose

The RAM will meet all stated functional and electrical specifications after a total ionizing radiation dose of $1x10^6$ rad(SiO_2) applied at T = 25°C. All electrical and timing performance parameters will remain within specifications after rebound at VDD = 5.5 V and T =125°C extrapolated to ten years of operation. Total dose hardness is assured by wafer level testing of process monitor transistors and RAM product using 10 keV X-ray radiation. Transistor gate threshold shift correlations have been made between 10 keV X-rays applied at a dose rate of $1x10^5$ rad(SiO_2)/min at T = 25°C and gamma rays (Cobalt 60 source) to ensure that wafer level X-ray testing is consistent with standard military radiation test environments.

Transient Pulse Ionizing Radiation

The RAM is capable of writing, reading, and retaining stored data during and after exposure to a transient ionizing radiation pulse of ≤1 μs duration up to $1x10^9$ rad(Si)/s, when applied under recommended operating conditions. To ensure validity of all specified performance parameters before, during, and after radiation (timing degradation during transient pulse radiation is ≤10%), it is suggested that a minimum of 0.8 μF per part of stiffening capacitance be placed between the package (chip) VDD and VSS, with a maximum inductance between the package (chip) and stiffening capacitance of 0.7 nH per part. If there are no operate-through or valid stored data requirements, the capacitance specification can be reduced to a minimum of 0.1 μF per part. A packaging option is available for mounting a small amount of supply decoupling capacitance underneath the package body.

The RAM will meet any functional or electrical specification after exposure to a radiation pulse of ≤ 50 ns duration up to $1x10^{12}$ rad(Si)/s, when applied under recommended operating conditions. Note that the current conducted during the pulse by the RAM inputs, outputs, and power supply may significantly exceed the normal operating levels. The application design must accommodate these effects.

Neutron Radiation

The RAM will meet any functional or timing specification after a total neutron fluence of up to $1x10^{14}$ cm^{-2} applied under recommended operating or storage conditions. This assumes an equivalent neutron energy of 1 MeV.

Soft Error Rate

The RAM is capable of soft error rate (SER) performance ranging from $1x10^{-6}$ to $1x10^{-10}$ upsets/bit-day at T = 80°C, under recommended operating conditions. This hardness level is defined by the Adams 10% worst case cosmic ray environment. A trade-off exists between soft error rate and write time performance over the operating temperature range. Detailed performance trade-off information is provided in the section Soft Error Rate and Write Time Performance Characteristics.

Latchup

The RAM will not latch up due to any of the above radiation exposure conditions, when applied under recommended operating conditions. Fabrication with the RICMOS™ p-epi on p+ substrate process and use of proven design techniques such as double guardbanding ensure latchup immunity.

RADIATION-HARDNESS RATINGS (1)

Parameter	Limits (2)	Units	Test Conditions
Total Dose	≥$1x10^6$	rad(SiO_2)	TA=25°C
Transient Dose Rate Upset (3)	≥$1x10^9$	rad(Si)/s	Pulse width≤1 μs
Transient Dose Rate Survivability	≥$1x10^{12}$	rad(Si)/s	Pulse width≤50 ns, X-ray, VDD=6.5 V, TA=25°C
Soft Error Rate (4)	<$1x10^{-10}$	upsets/bit-day	TA=80°C, Adams 10% worst case environment
Neutron Fluence	≥$1x10^{14}$	N/cm^2	1 MeV equivalent energy, Unbiased, TA=25°C

(1) Device will not latch up due to any of the specified radiation exposure conditions.

(2) Operating conditions (unless otherwise specified): VDD=4.5 V to 5.5 V, TA=-55°C to +125°C

(3) Suggested stiffening capacitance specifications for optimum dose rate upset performance are stated above.

(4) SER and write time performance trade-offs over the operating temperature range are shown later in this data sheet.

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Parameter		Rating Min	Rating Max	Units
VDD	Positive Supply Voltage (referenced to VSS)		-0.5	7.0	V
VPIN	Voltage on Any Pin (referenced to VSS)		-0.5	VDD+0.5	V
TSTORE	Storage Temperature (Zero Bias)		-65	150	°C
TSOLDER	Soldering Temperature • Time			270•5	°C•s
PD	Total Package Power Dissipation (2)			2.5	W
IOUT	DC or Average Output Current			25	mA
VPROT	Electrostatic Discharge Protection Voltage (3)			4000	V
ΘJC	Thermal Resistance (Junction-to-Case)	36 FP		2	°C/W
		28 DIP		10	
TJ	Junction Temperature			175	°C

(1) Stresses in excess of those listed above may result in permanent damage to the HC6364. These are stress ratings only, and operation at these levels is not implied. Frequent or extended exposure to absolute maximum conditions may affect device reliability.
(2) RAM power dissipation due to IDDS and IDDOP, plus RAM output driver power dissipation due to external loading must not exceed this value.
(3) Class 3 electrostatic discharge (ESD) input protection voltage per MIL-STD-883, Method 3015.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Description Min	Description Typ	Description Max	Units
VDD	Supply Voltage (referenced to VSS)	4.5	5.0	5.5	V
TA	Ambient Temperature	-55	25	125	°C
VPIN	Voltage on Any Pin (referenced to VSS)	-0.3		VDD+0.3	V

CAPACITANCE (1)

Symbol	Parameter	Typical	Worst Case Min	Worst Case Max	Units	Test Conditions
CI	Input Capacitance	7		9	pF	VI=VDD or VSS, f=1 MHz
CO	Output Capacitance	12		14	pF	VIO=VDD or VSS, f=1 MHz

(1) This parameter is tested during initial device characterization only.

DATA RETENTION CHARACTERISTICS

Symbol	Parameter	Typical (1)	Worst Case (2) Min	Worst Case (2) Max	Units	Test Conditions
VDR	Data Retention Voltage (3)		2.5		V	NCS=VDR VI=VDR or VSS
IDR	Data Retention Current	20		300	µA	NCS=VDD=VDR VI=VDR or VSS
TCDR	Chip Deselect to Data Retention Mode Time (5)		0		ns	Timing References: NCS= 2.4 V or CE=0.4 V to VDD=4.75 V
TR	Recovery Time (4) (5)			TAVAVR	ns	

(1) Typical operating conditions: TA= 25°C, pre-radiation
(2) Worst case operating conditions: TA= -55°C to +125°C, total dose through $1x10^6$ rad(SiO_2)
(3) To maintain valid data storage during transient radiation, VDD must be held within the recommended operating range.
(4) Read cycle time
(5) This parameter is tested during initial device characterization only.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Typical (1)	Worst Case (2) Min	Worst Case (2) Max	Units	Test Conditions (3)
IDDSB1	Static Supply Current	10		450	µA	IO = 0 Inputs Stable
IDDSB2	Static Supply Current with Chip Disabled	10		450	µA	VSS≤ VI≤VDD IO = 0 , CE = VIL (4)
IDDSEIH	Static Supply Current per Enabled Input*	6		30	µA	VIH = VDD-0.5V, CE = VIH (4)
IDDSEIL	Static Supply Current per Enabled Input*	6		30	µA	VIL = 0.5V, CE = VIH (4)
IDDOPW	Dynamic Supply Current, Selected (Write)	7		8	mA	f=1 MHz IO=0 CE=VIH NCS=NAS=VIL (5)
IDDOPR	Dynamic Supply Current, Selected (Read)	5		6	mA	f=1 MHz IO=0 CE=VIH NCS=NAS=VIL (5)
IDDOP1	Dynamic Supply Current, Deselected	0.8		1.0	mA	f=1 MHz IO=0 NAS=VIL NCS=CE=VIH (5)
IDDOP2	Dynamic Supply Current, Disabled	1		20	µA	f=1 MHz IO=0 CE=VIL (5)
IDDOP3	Dynamic Supply Current, Addresses Latched	0.25		0.4	mA	f=1 MHz IO=0 NCS=CE=NAS=VIH (5)
II	Input Leakage Current	0.05	-5	5	µA	VSS≤VI≤VDD
IOZ	Output Leakage Current	0.1	-10	10	µA	VSS≤VIO≤VDD Output=high Z
VIL	Low-Level Input Voltage (TTL) (CMOS)	1.3		0.8 0.3*VDD	V	March Pattern VDD=4.5V
VIH	High-Level Input Voltage (TTL) (CMOS)	1.7	2.2 0.7*VDD		V	March Pattern VDD=5.5V
VOL	Low-Level Output Voltage	0.2		0.4 0.1	V	IOL = 10 mA IOL = 20 µA VDD=4.5V
VOH	High-Level Output Voltage	4.4	4.2 VDD-0.1		V	IOH = -5 mA IOH = -20 µA VDD=4.5V

(1) Typical operating conditions: VDD = 5.0 V,TA = 25°C, pre-radiation

(2) Worst case operating conditions: VDD = 4.5 V to 5.5 V, TA = -55°C to +125°C, total dose through $1x10^6$ rad(SiO_2)

(3) Input High = VIH ≥ VDD - 0.3 Volt, Input Low = VIL ≤ 0.3 Volt

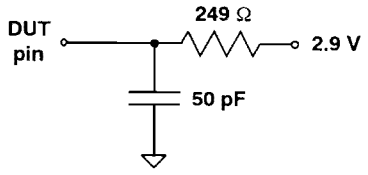
(4) Guaranteed but not tested

(5) All inputs switching, DC average current

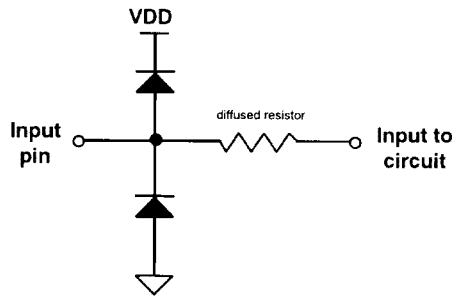
* ENABLED INPUT PINS TRUTH TABLE

CE	NCS	NWE	# of enabled input pins
H	L	L	27
H	L	H	19
H	H	X	13
L	X	X	1

X: VIN = VIH OR VIL



EQUIVALENT LOAD CIRCUIT

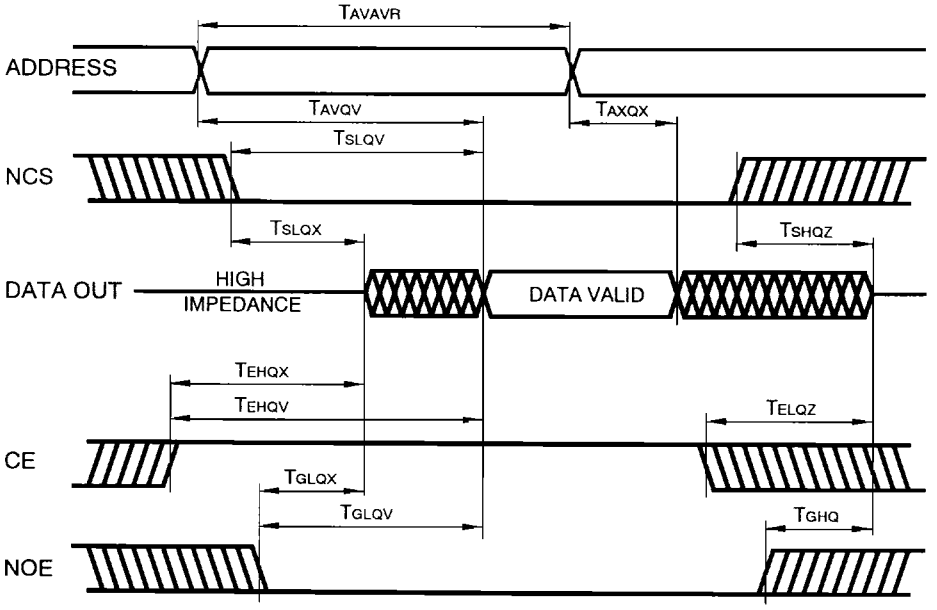


EQUIVALENT ESD PROTECTION CIRCUIT

READ CYCLE AC TIMING CHARACTERISTICS (1)

Symbol	Parameter	Typical (2)	Worst Case (3)				Units
			0 to 80 °C		-55 to 125 °C		
			Min	Max	Min	Max	
TAVAVR	Address Read Cycle Time	27	45		55		ns
TAVQV	Address Access Time	25		45		55	ns
TAXQX	Address Change to Output Invalid Time	15	5		5		ns
TSLQV	Chip Select Access Time	21		45		55	ns
TSLQX	Chip Select Output Enable Time	6	0		0		ns
TSHQZ	Chip Select Output Disable Time	10		20		20	ns
TEHQV	Chip Enable Access Time	30		45		55	ns
TEHQX	Chip Enable Output Enable Time	11	0		0		ns
TELQZ	Chip Enable Output Disable Time	11		25		25	ns
TGLQV	Output Enable Access Time	11		15		15	ns
TGLQX	Output Enable Output Enable Time	7	0		0		ns
TGHQZ	Output Enable Output Disable Time	10		15		15	ns

(1) Test conditions: input switching levels VIL/VIH=0.0 V/3.0 V for TTL input buffers, and VIL/VIH=0.5 V/VDD-0.5 V for CMOS input buffers, input rise and fall times <5 ns, capacitive output loading=50 pF. Timing reference levels are shown in the Tester AC Timing Characteristics table.
(2) Typical operating conditions: VDD=5.0 V, TA=25°C, pre-radiation
(3) Worst case operating conditions: VDD=4.5 V to 5.5 V, total dose through 1x10^6 rad(SiO_2)
The -55 to 125 °C values are tested and the 0 to 80 °C values are extrapolated.

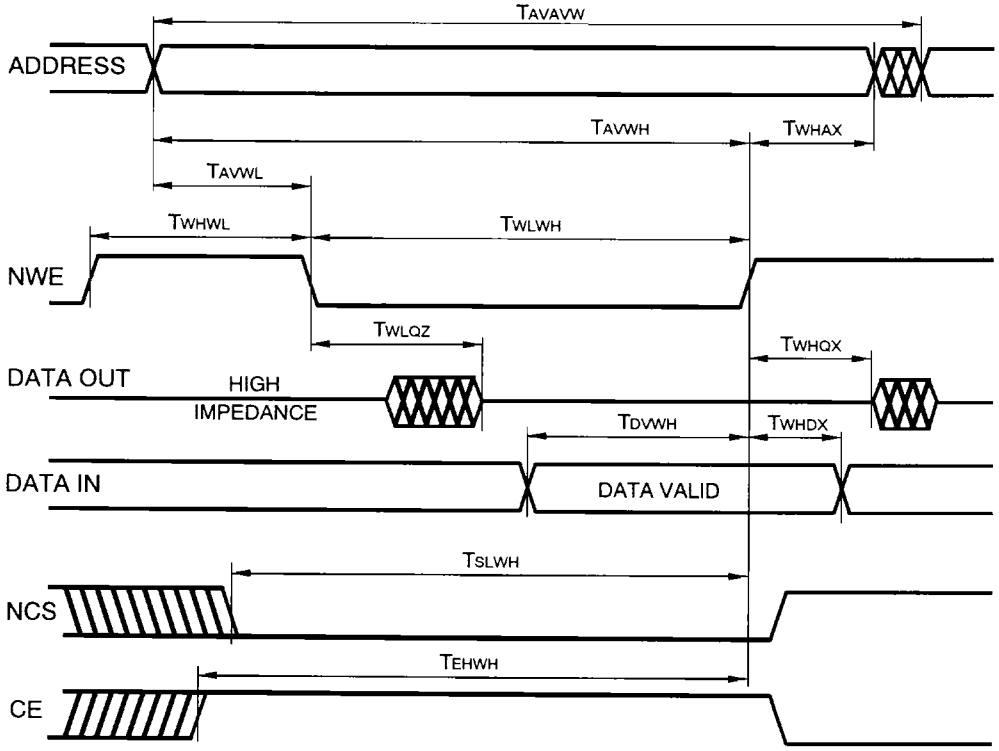


(NAS = low, NWE = high)

WRITE CYCLE AC TIMING CHARACTERISTICS (1,2)

Symbol	Parameter	Typical	Worst Case (4)				Units
			0 to 80 °C		-55 to 125 °C		
		(3)	Min	Max	Min	Max	
TAVAVW	Write Cycle Time	25	50		55		ns
TWLWH	Write Enable Write Pulse Width	22	40		45		ns
TSLWH	Chip Select to End of Write Time	21	40		45		ns
TDVWH	Data Valid to End of Write Time	26	40		45		ns
TAVWH	Address Valid to End of Write Time	23	40		45		ns
TWHDX	Data Hold Time after End of Write Time	0	0		0		ns
TAVWL	Address Valid Setup to Start of Write Time	0	0		0		ns
TWHAX	Address Valid Hold after End of Write Time	0	0		0		ns
TWLQZ	Write Enable Output Disable Time	9		15		15	ns
TWHQX	Write Enable Output Enable Time	6	0		0		ns
TWHWL	Write Enable Write Disable Pulse Width	5	5		5		ns
TEHWH	Chip Enable to End of Write Time	27	45		50		ns

(1) Test conditions: input switching levels VIL/VIH=0.0 V/3.0 V for TTL input buffers, and VIL/VIH=0.5 V/VDD-0.5 V for CMOS input buffers, input rise and fall times <5 ns, capacitive output loading=50 pF. Timing reference levels are shown in the Tester AC Timing Characteristics table.
(2) All write time parameters reflect an SER part type C.
(3) Typical operating conditions: VDD=5.0 V, TA=25°C, pre-radiation
(4) Worst case operating conditions: VDD=4.5 V to 5.5 V, total dose through $1x10^6$ rad(SiO_2)
The -55 to 125 °C values are tested and the 0 to 80 °C values are extrapolated.



(NAS = low)

DYNAMIC ELECTRICAL CHARACTERISTICS

Read Cycle

The RAM is asynchronous in operation, allowing the read cycle to be controlled by address, chip select (NCS), or chip enable (CE) (refer to Read Cycle timing diagram). To perform a valid read operation, both chip select and output enable (NOE) must be low and chip enable and write enable (NWE) must be high. The output drivers can be controlled independently by the NOE signal. Consecutive read cycles can be executed with NCS held continuously low, and/or with CE held continuously high.

For an address activated read cycle, NCS must be valid prior to, coincident with, or within (TAVQV minus TSLQV) time following the activating address edge transition(s). CE must be valid a minimum of (TEHQV minus TAVQV) time prior to the activating address edge transition(s). Any amount of toggling or skew between address edge transitions is permissible; however, data outputs will become valid TAVQV time following the latest occurring address edge transition. The minimum address activated read cycle time is TAVAVR. When the RAM is operated at the minimum address activated read cycle time, the data outputs will remain valid on the RAM I/O until TAVQX time following the next sequential address transition.

To control a read cycle with NCS, all addresses must be valid at least (TAVQV minus TSLQV) time prior to the enabling NCS edge transition. CE must be valid a minimum of (TEHQV minus TSLQV) time prior to the enabling NCS edge transition. Address or CE edge transitions can occur later than the specified setup times to NCS; however, the valid data access time will be delayed. Any address edge transition which occurs during the time when NCS is low will initiate a new read access, and data outputs will not become valid until TAVQV time following the address edge transition. Data outputs will enter a high impedance state TSHQZ time following a disabling NCS edge transition.

To control a read cycle with CE, all addresses and NCS must be valid prior to or coincident with the enabling CE edge transition. Address or NCS edge transitions can occur later than the specified setup times to CE; however, the valid data access time will be delayed. Any address edge transition which occurs during the time when CE is high will initiate a new read access, and data outputs will not become valid until TAVQV time following the address edge transition. Data outputs will enter a high impedance state TELQZ time following a disabling CE edge transition.

The address strobe (NAS) control signal can be used to internally latch address inputs, thereby allowing an external address change to occur without corruption of the valid data output from the previous read access. This feature can be used to operate the RAM with reduced dynamic power or with multiplexed address inputs. If no address latching capabilities are desired, NAS can be held continuously low.

Write Cycle

The write operation is synchronous with respect to the address bits and control is governed by write enable (NWE), chip select (NCS), or chip enable (CE) edge transitions (refer to Write Cycle timing diagrams). To perform a write operation, both NWE and NCS must be low, and CE must be high. When NCS and NWE are simultaneously driven low, the data output lines (DQ) will remain in the high impedance state. Consecutive write cycles can be performed with NWE or NCS held continuously low, or CE held continuously high. At least one of the control signals must transition to the opposite state between consecutive write operations.

To write data into the RAM, NWE and NCS must be held low and CE must be held high for at least TWLWH/TSLSH/TEHEL time. Any amount of edge skew between the signals can be tolerated, and any one of the control signals can initiate or terminate the write operation. For consecutive write operations, write pulses must be separated by the minimum specified TWHWL/TSHSL/TELEH time. Address inputs must be valid at least TAVWL/TAVSL/TAVEH time before the enabling NWE/NCS/CE edge transition, and must remain valid during the entire write time. A valid data overlap of write pulse width time of TDVWH/TDVSH/TDVEL, and an address valid to end of write time of TAVWH/TAVSH/TAVEL also must be provided for during the write operation. Hold times for address inputs and data inputs with respect to the disabling NWE/NCS/CE edge transition must be a minimum of TWHAX/TSHAX/TELAX time and TWHDX/TSHDX/TELDX time, respectively. The minimum write cycle time is TAVAVW.

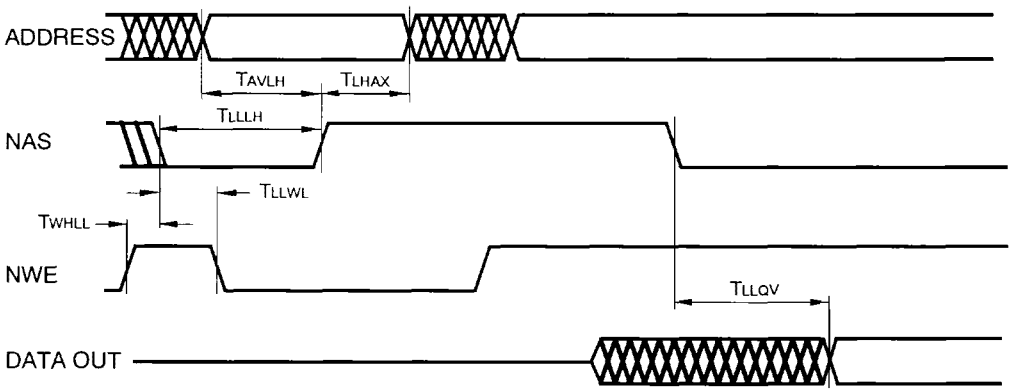
The address strobe (NAS) control signal can be used to internally latch address inputs, thereby allowing an external address change to occur without corruption of the in-progress write operation. This feature can be used to operate the RAM with reduced dynamic power or with multiplexed address inputs. If no address latching capabilities are desired, NAS can be held continuously low. Timing specifics for NAS latching operations are shown below.

Write cycle timing parameters listed in the Write Cycle Characteristics table reflect a soft error rate performance level of $1x10^{-7}$ upsets/bit-day. Performance curves illustrating soft error rate and write time performance are shown later in this data sheet.

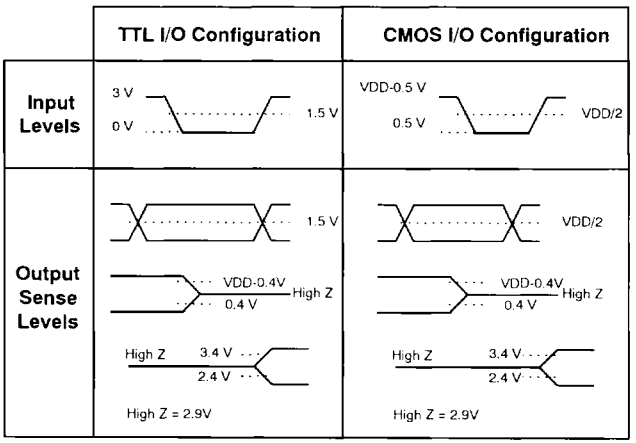
NAS CYCLE AC ELECTRICAL CHARACTERISTICS (1)

Symbol	Parameter	Typical (2)	Worst Case (3) 0 to 80 °C Min	Worst Case (3) 0 to 80 °C Max	Worst Case (3) -55 to 125 °C Min	Worst Case (3) -55 to 125 °C Max	Units
TAVLH	Address Setup to Address Strobe Time	0	15		15		ns
TLHAX	Address Hold after Address Strobe Time	4	20		20		ns
TLLLH	Address Strobe Pulse Width	5	20		20		ns
TLLWL	Address Strobe Setup to Start of Write	0	15		15		ns
TWHLL	Address Strobe Hold after End of Write	0	3		3		ns
TLLQV	Address Strobe Access Time	26		45		55	ns

(1) Test conditions: input switching levels VIL/VIH=0.0 V/3.0 V for TTL input buffers, and VIL/VIH=0.5 V/VDD-0.5 V for CMOS input buffers, input rise and fall times <5 ns, capacitive output loading=50 pF. Timing reference levels are shown in the Tester AC Timing Characteristics table.
(2) Typical operating conditions: VDD=5.0 V, TA=25°C, pre-radiation
(3) Worst case operating conditions: VDD=4.5 V to 5.5 V, total dose through $1x10^6$ rad(SiO_2)
The -55 to 125 °C values are tested and the 0 to 80 °C values are extrapolated.

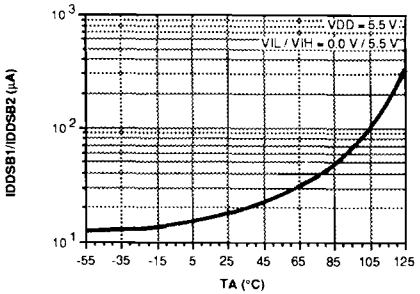


TESTER AC TIMING CHARACTERISTICS

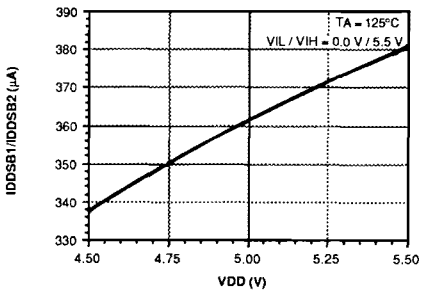


TYPICAL PRE-RAD DC AND AC ELECTRICAL PERFORMANCE CHARACTERISTICS

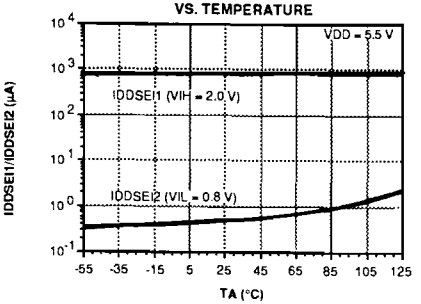
STANDBY CURRENT VS. TEMPERATURE



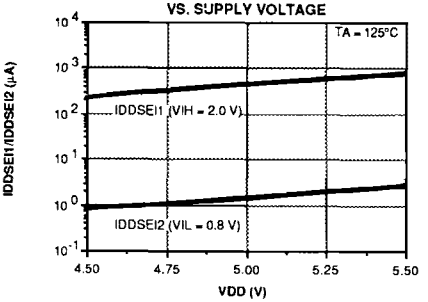
STANDBY CURRENT VS. SUPPLY VOLTAGE



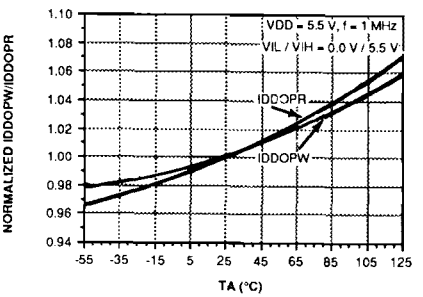
SUPPLY CURRENT CONTRIBUTIONS PER ENABLED INPUT VS. TEMPERATURE



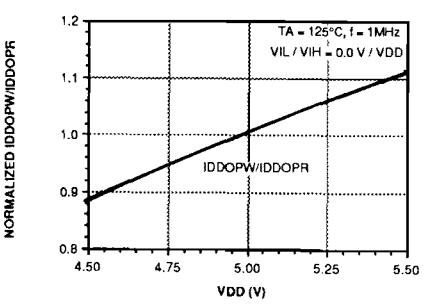
SUPPLY CURRENT CONTRIBUTIONS PER ENABLED INPUT VS. SUPPLY VOLTAGE



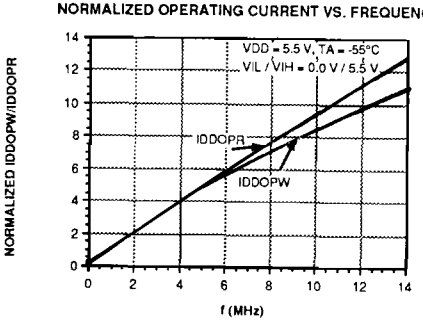
NORMALIZED OPERATING CURRENT VS. TEMPERATURE



NORMALIZED OPERATING CURRENT VS. SUPPLY VOLTAGE

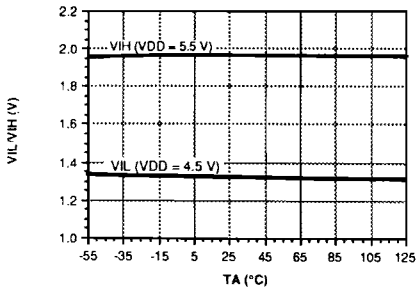


NORMALIZED OPERATING CURRENT VS. FREQUENCY

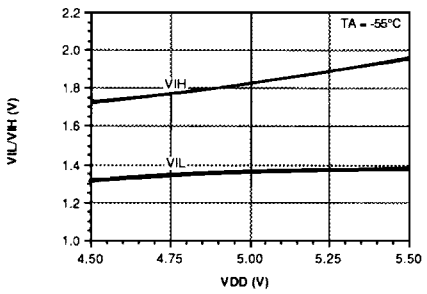


TYPICAL PRE-RAD DC AND AC ELECTRICAL PERFORMANCE CHARACTERISTICS

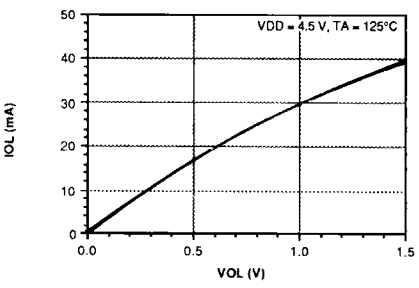
LOW/HIGH INPUT VOLTAGE LEVELS VS. TEMPERATURE



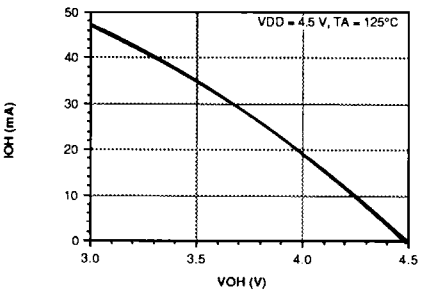
LOW/HIGH INPUT VOLTAGE LEVELS VS. SUPPLY VOLTAGE



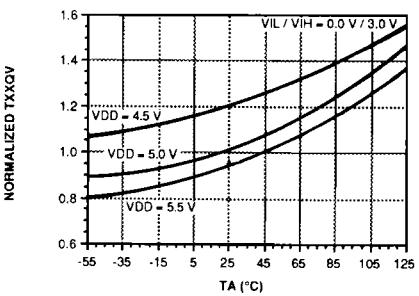
OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE



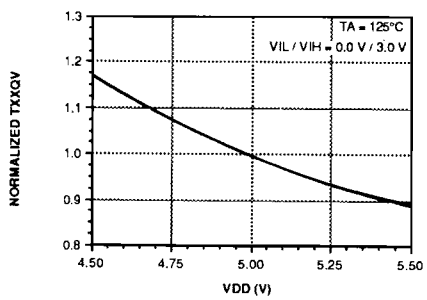
OUTPUT SOURCE CURRENT VS. OUTPUT VOLTAGE



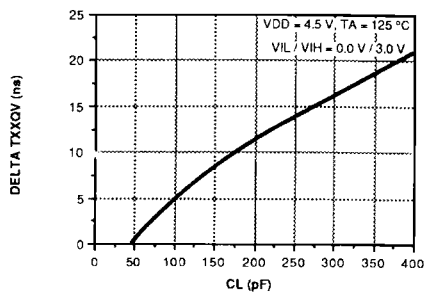
NORMALIZED READ ACCESS TIME VS. TEMPERATURE



NORMALIZED READ ACCESS TIME VS. SUPPLY VOLTAGE



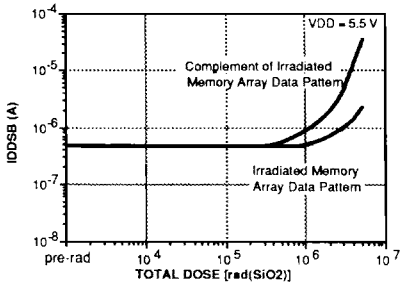
READ ACCESS TIME DELTA VS. LOAD CAPACITANCE



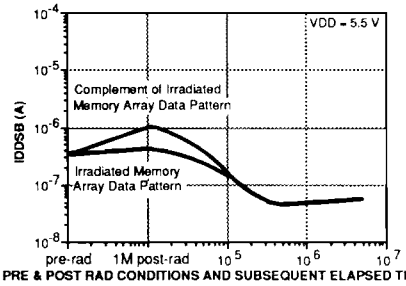
3

TYPICAL TOTAL DOSE AND REBOUND PERFORMANCE CHARACTERISTICS (1)

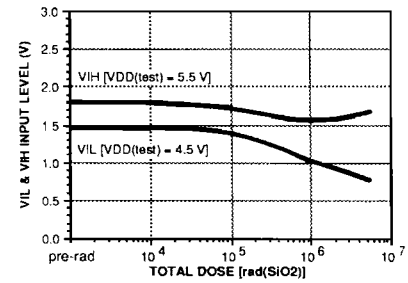
STANDBY CURRENT VS. TOTAL DOSE (2)



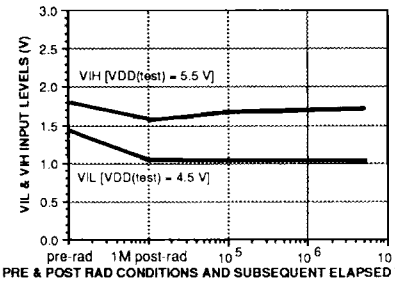
STANDBY CURRENT REBOUND RESPONSE (2, 3)



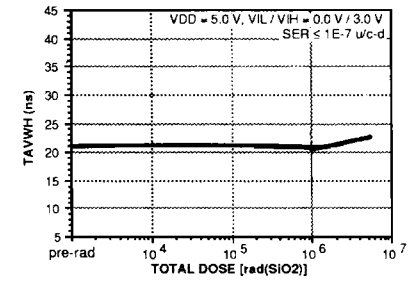
LOW & HIGH INPUT VOLTAGE LEVELS VS. TOTAL DOSE (2)



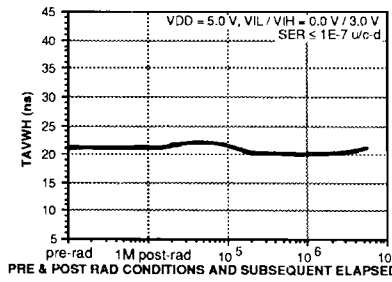
LOW & HIGH INPUT VOLTAGE LEVELS REBOUND RESPONSE (2, 3)



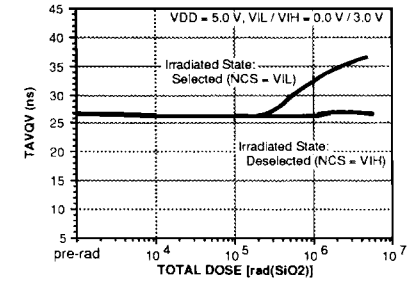
ADDRESS VALID TO END OF WRITE TIME VS. TOTAL DOSE (2)



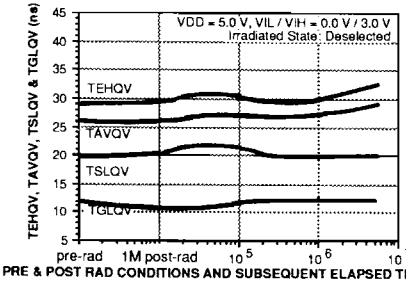
ADDRESS VALID TO END OF WRITE TIME REBOUND RESPONSE (2, 3)



READ ACCESS TIME VS. TOTAL DOSE (2, 4)



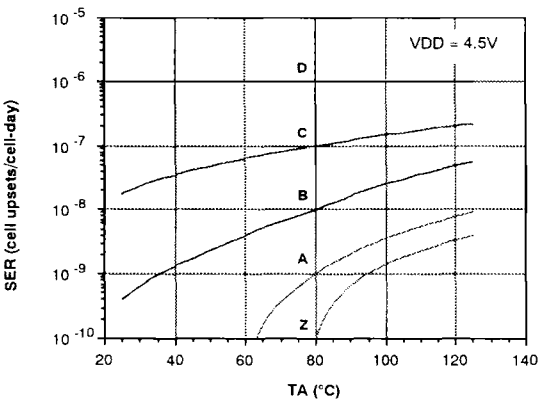
READ ACCESS TIME REBOUND RESPONSE (2, 3)



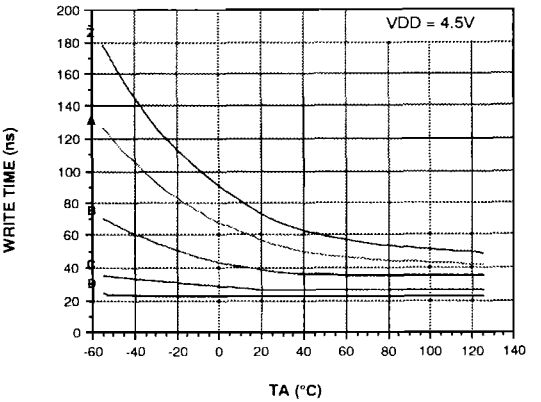
(1) Radiation source: ARACOR System [10 keV X-ray, $1x10^5$ rad(SiO_2)/min]. Studies show the device response between ARACOR and Cobalt-60 to be within 10%.
(2) Irradiation conditions: TA=25°C, VDD=5.5 V. Test conditions: TA=25°C
(3) Rebound conditions: VDD=unbiased and TA=25°C for Time < $9x10^4$ s; VDD=5.5 V and TA=125°C for Time ≥ $9x10^4$ s
(4) Post-rad read access time increases when irradiated state is selected and static (not cycling).

SOFT ERROR RATE AND WRITE TIME PERFORMANCE CHARACTERISTICS

SOFT ERROR RATE VS. TEMPERATURE



WRITE TIME VS. TEMPERATURE*



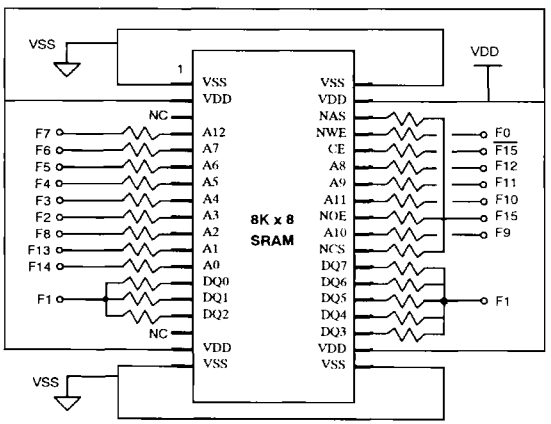
WORST CASE SER PERFORMANCE AT 80°C
ADAMS 10% ENVIRONMENT

Z: 1.0x10^{-10} upsets/bit-day
A: 1.0x10^{-9} upsets/bit-day
B: 1.0x10^{-8} upsets/bit-day
C: 1.0x10^{-7} upsets/bit-day
D: 1.0x10^{-6} upsets/bit-day

TYPICAL WRITE TIME (TAVWH)
PERFORMANCE AT 0°C

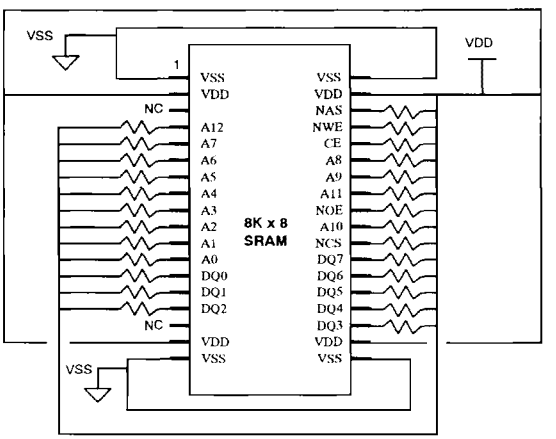
Z: 90 ns
A: 68 ns
B: 43 ns
C: 30 ns
D: 23 ns

* Associated write times are TWLWH, TSLWH, and TDVWH. TEHWH write time behaves in a similar manner.



DYNAMIC BURN-IN DIAGRAM

VDD = 5.5 ± 0.5V, R ≤ 10 KΩ, VIH = VDD, VIL = VSS
Ambient Temperature ≥ 125 °C, F0 ≥ 100 KHz Sq Wave
Frequency of F1 = F0/2, F2 = F0/4, F3 = F0/8, etc.



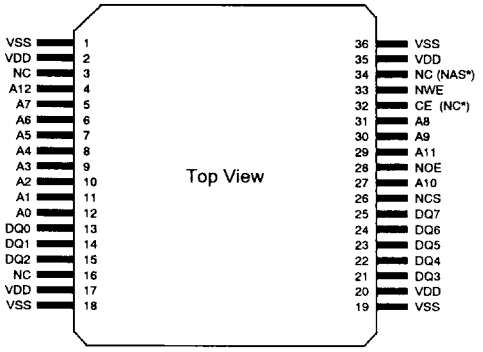
STATIC BURN-IN DIAGRAM

VDD = 5.5 ± 0.5V, R ≤ 10 KΩ
Ambient Temperature ≥ 125 °C

PACKAGING

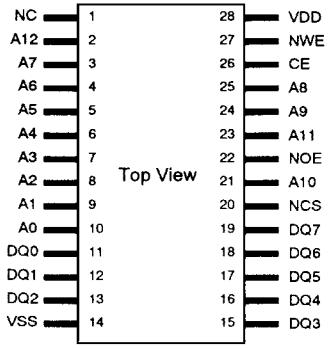
The 8K x 8 SRAM is offered in a custom 36-lead flat pack or 28-lead DIP. Both packages are constructed of multilayer ceramic (Al_2O_3) and contains internal power and ground planes. Optional capacitors can be mounted to the packages to maximize supply noise decoupling and increase board packing density. The capacitors attach directly to the internal package power and ground planes. This design minimizes resistance and inductance of the bond wire and package, both of which are critical in a transient radiation environment. All NC pins must be connected to either VDD, VSS or an active driver to prevent charge build up in the radiation environment.

36-LEAD FLAT PACK PINOUT



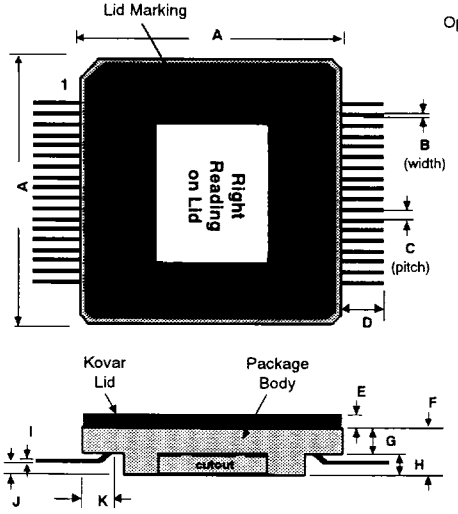
* Optional package pin configuration (NC = no connect)

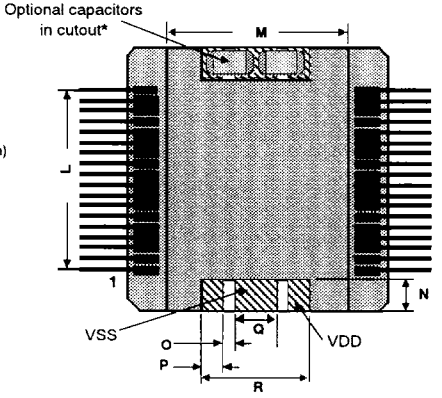
28-LEAD DIP PINOUT



(NC = no connect)

36-LEAD FLAT PACK





All dimensions in inches

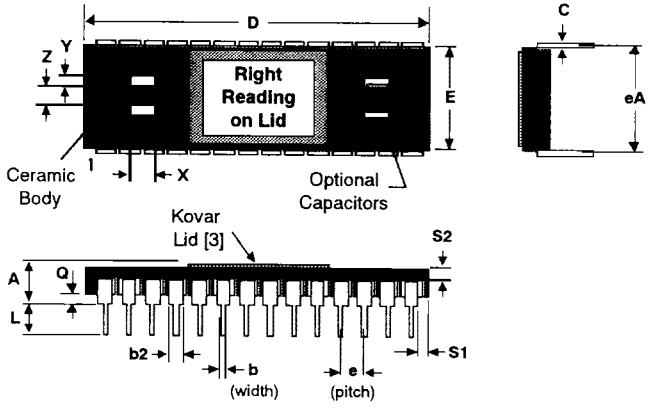
A	0.630 ± 0.007	J	0.026 min
B	0.008 ± 0.002	K	0.050 ref
C	0.025 ± 0.002	L	0.425 ± 0.005
D	0.270 min [1]	M	0.480 ± 0.006
E	0.012 ± 0.001	N	0.080 ref
F	0.115 ± 0.010	O	0.030 ref
G	0.065 ± 0.007	P	0.050 ref
H	0.050 ± 0.004	Q	0.100 ref
I	0.0060 ± 0.0015	R	0.260 ref

[1] Parts delivered with leads unformed

36 Lead Flat Pack
Package body: Honeywell #22005907
Kovar lid (solder seal): Honeywell #22006823-043
Package carrier: Honeywell #22007244
Package socket: Honeywell #22016515

*** Contact factory for optional on-package capacitors**

28-LEAD DIP



All dimensions in inches [1]

A	0.175 (max)	L	0.125 to 0.200
b	0.020 ± 0.006	Q	0.015 to 0.060
b2	0.055 ± 0.010	S1	0.005 (min)
c	0.009 to 0.012	S2	0.005 (min)
D	1.400 ± 0.020	X	0.100 ref
E	0.595 ± 0.015	Y	0.050 ref
e	0.100 BSC [2]	Z	0.075 ref
eA	0.600 BSC [2]		

[1] Dimensions meet MIL-STD-1835, Config. C, D-10
[2] BSC - Basic lead Spacing between Centers
[3] Lid tied to VSS

3

ORDERING INFORMATION

H	C	6364/1	X	S	H	C	T

SOURCE
H=HONEYWELL

PROCESS
C=CMOS

PART NUMBER AND PIN CONFIGURATION (4)

PACKAGE DESIGNATION
X=36-Lead Flat Pack without capacitors
Y=36-Lead Flat Pack with capacitors
R=28-Lead DIP without capacitors
S=28-Lead DIP with capacitors
- =Bare Die (No Package)

SCREEN LEVEL
C=Brass Board
S=Modified Class S (1)
Q=QML Class Q
V=QML Class V

RADIATION HARDNESS
H=1x10^6 rad(SiO_2)

SOFT ERROR RATE (2,3)
Z <1x10^{-10} upsets/bit-day
A <1x10^{-9} upsets/bit-day
B <1x10^{-8} upsets/bit-day
C <1x10^{-7} upsets/bit-day
D <1x10^{-6} upsets/bit-day
- = Brass Board

INPUT BUFFER TYPE
T=TTL Level
C=CMOS Level

(1) Refer to Assembly and Screening Procedure section for Honeywell's screening procedures.
(2) Soft error rate (SER) specifications indicate worst case, high temperature (80°C). Performance curves which illustrate the trade-off between SER and write time performance over the operating temperature range are shown earlier in this data sheet.
(3) The Write Cycle timing parameters for SER levels A, B, D, and Z are not included in this data sheet. Contact Honeywell for further information on additional SER and write time pairings.

(4) Optional pin configurations: (NC = no connect)

	36-LEAD FP		28-LEAD DIP	
	PIN 32	PIN 34	PIN 26	PIN 20
HC6364/1	CE	NC	CE	NCS
HC6364/2	CE	NAS	-	-
HC6364/3	NC	NC	-	-
HC6364/4	NC	NAS	-	-

This data sheet contains specifications that are based on production packaged parts.

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