

Description

The μPD431000A is a 131,072-word by 8-bit static RAM fabricated with advanced silicon-gate technology. CMOS peripheral circuits and N-channel memory cells with polysilicon resistors make the μPD431000A a high-speed device that requires very low power and no clock or refreshing.

Minimum standby power is drawn when CE₂ is low, independent of the other inputs' levels. Data retention is guaranteed at a power supply voltage as low as 2 volts. The μPD431000A is available in standard 32-pin plastic DIP, 32-pin plastic miniflat, and 32-pin plastic TSOP packaging.

Features

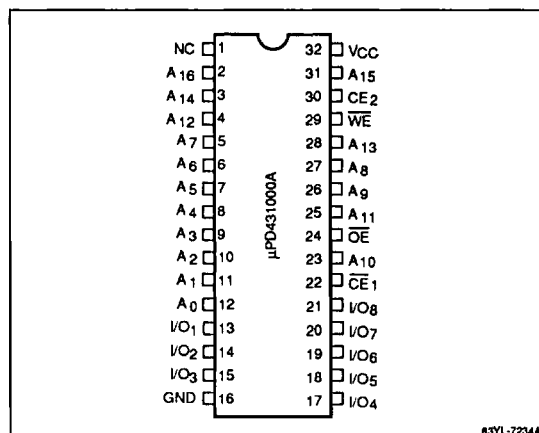
- 131,072-word by 8-bit organization
- Single + 5-volt power supply
- Fully static operation—no clock or refreshing
- TTL-compatible inputs and outputs
- Common I/O using three-state outputs
- Two CE pins and one $\overline{OE}$ pin for easy application
- Data retention current of 1 μA typical
- Data retention voltage of 2 V minimum
- Standard 32-pin plastic DIP, miniflat and TSOP packaging

Pin Identification

Symbol	Function
A ₀ - A ₁₆	Address inputs
I/O ₀ - I/O ₇	Data inputs/outputs
$\overline{CE}_1$, CE ₂	Chip enables 1 and 2
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
GND	Ground
V _{CC}	+ 5-volt power supply
NC	No connection

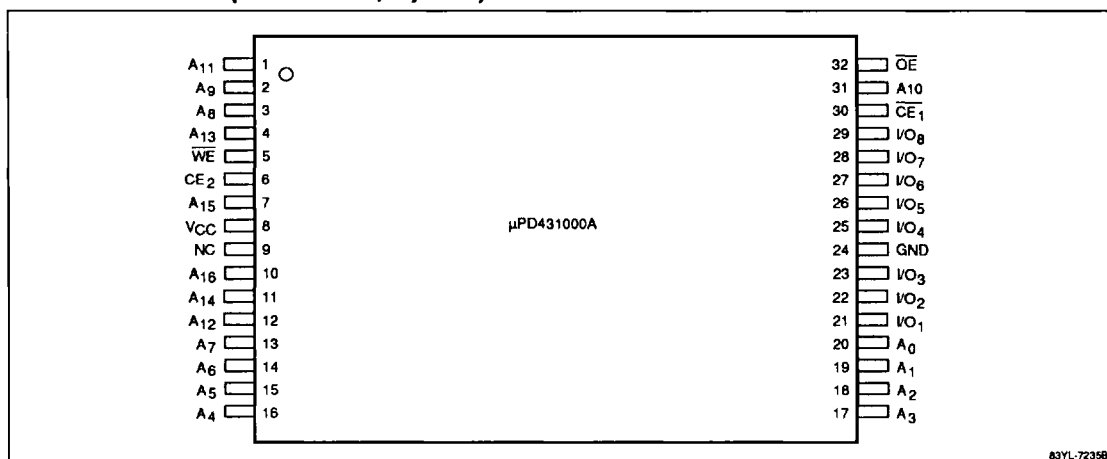
Pin Configurations

32-Pin Plastic DIP or Miniflat

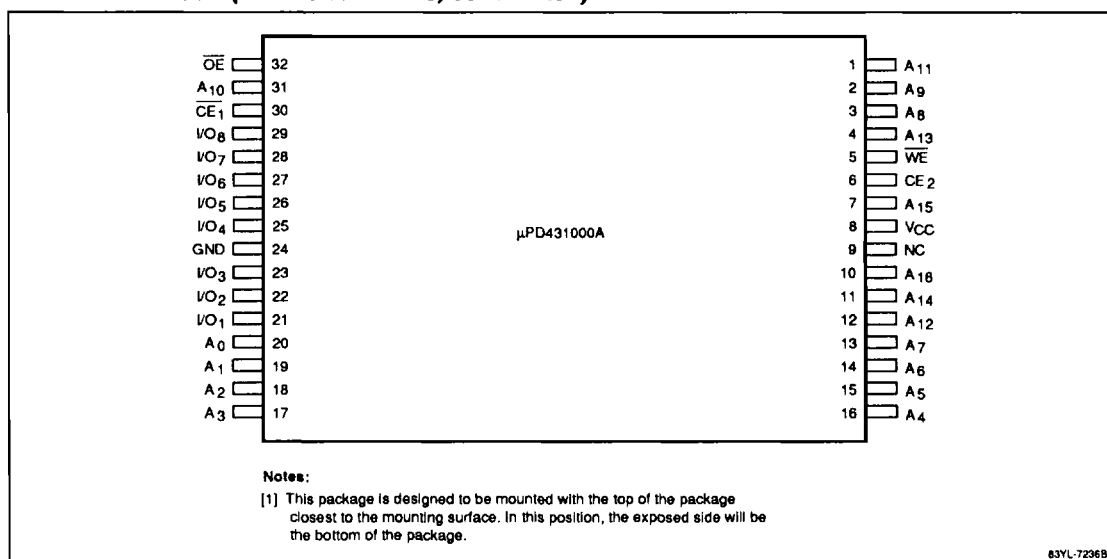


Pin Configurations (cont)

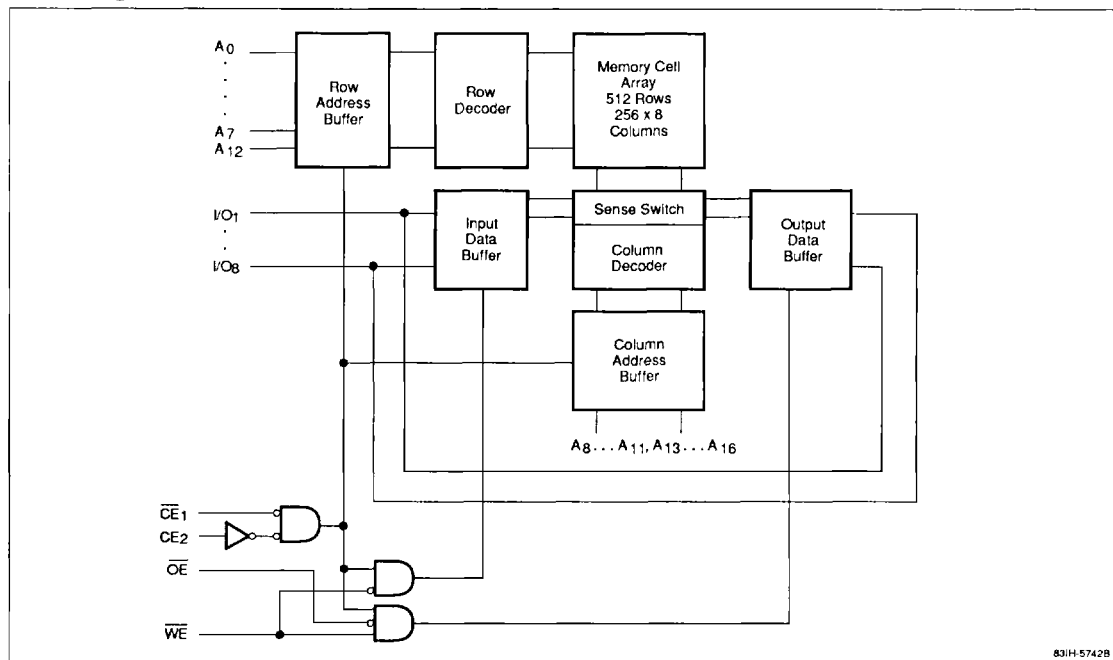
32-Pin Plastic TSOP (normal leads, top view)



32-Pin Plastic TSOP (reverse bent leads, bottom view)



Block Diagram



Absolute Maximum Ratings

Supply voltage, V_{CC} (Note 1)	-0.5 to +7.0 V
Input voltage, V_{IN} (Note 1)	-0.5 to V_{CC} + 0.5 V
Output voltage, V_{VO} (Note 1)	-0.5 to V_{CC} + 0.5 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	-55 to +125°C
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Notes:

(1) - 3.0 V minimum (pulse width = 50 ns).

Capacitance

 $T_A = +25^\circ\text{C}; f = 1\text{ MHz}; V_{IN} \text{ and } V_{OUT} = 0\text{ V}$

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_i			6	pF
Input/output capacitance	$C_{i/o}$			10	pF

Notes:

(1) This parameter is sampled and not 100% tested.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, low	V_{IL}	-0.3		0.8	V
Input voltage, high	V_{IH}	2.2		$V_{CC} + 0.5$	V
Ambient temperature	T_A	0		70	°C

Notes:

(1) - 3.0 V minimum (pulse width = 50 ns).

Truth Table

Function	$\overline{CE}_1$	CE_2	$\overline{OE}$	$\overline{WE}$	I/O	I _{CC}
Not selected	H	X	X	X	High-Z	Standby
Not selected	X	L	X	X	High-Z	Standby
Selected	L	H	H	H	High-Z	Active
Read	L	H	L	H	D _{OUT}	Active
Write	L	H	X	L	D _{IN}	Active

Notes:

(1) $X = \text{don't care.}$

Ordering Information

Part Number	Access Time (max)	I _{SB1} (max)	Package
μPD431000ACZ-70	70 ns	2 mA	32-pin plastic DIP
CZ-85	85 ns		
CZ-10	100 ns		
μPD431000ACZ-70L	70 ns	0.1 mA	
CZ-85L	85 ns		
CZ-10L	100 ns		
μPD431000AGW-70L	70 ns	0.1 mA	32-pin plastic miniflat
GW-85L	85 ns		
GW-10L	100 ns		
μPD431000AGZ-70-KJH	70 ns	2 mA	32-pin plastic TSOP (normal leads)
GZ-85-KJH	85 ns		
GZ-10-KJH	100 ns		
μPD431000AGZ-70L-KJH	70 ns	0.1 mA	
GZ-85L-KJH	85 ns		
GZ-10L-KJH	100 ns		
μPD431000AGZ-70-KKH	70 ns	2 mA	32-pin plastic TSOP (reverse bent leads)
GZ-85-KKH	85 ns		
GZ-10-KKH	100 ns		
μPD431000AGZ-70L-KKH	70 ns	0.1 mA	
GZ-85L-KKH	85 ns		
GZ-10L-KKH	100 ns		

Notes:

- (1) Contact your NEC sales representative for data sheet and product availability for the -LL version of the μPD431000A.

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ± 10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I _{LI}	-1		1	μA	V _{IN} = 0 V to V _{CC}
I/O leakage current	I _{LO}	-1		1	μA	V _{I/O} = 0 V to V _{CC} ; $\overline{CE}_1 = V_{IH}$, or CE ₂ = V _{IL} , or $\overline{OE} = V_{IH}$, or $\overline{WE} = V_{IL}$
Operating supply current	I _{CCA1}		40	70	mA	$\overline{CE}_1 = V_{IL}$; CE ₂ = V _{IH} ; t _{RC} = t _{RC} (min); I _{I/O} = 0 mA
	I _{CCA2}			15	mA	$\overline{CE}_1 = V_{IL}$; CE ₂ = V _{IH} ; I _{I/O} = 0 mA
	I _{CCA3}			10	mA	V _{CE1} ≤ 0.2 V; V _{CE2} ≥ V _{CC} - 0.2 V; t _{RC} or t _{WC} = 1 MHz; V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} - 0.2 V
Standby supply current	I _{SB}			5	mA	$\overline{CE}_1 = V_{IH}$ or CE ₂ = V _{IL} (Note 1)
	I _{SB1}		0.02	2	mA	$\overline{CE}_1$ and CE ₂ ≥ V _{CC} - 0.2 V (Note 2)
	I _{SB2}		0.02	2	mA	CE ₂ ≤ 0.2 V (Note 2)
Output voltage, low	V _{OL}			0.4	V	I _{OL} = 2.1 mA
Output voltage, high	V _{OH}	2.4			V	I _{OH} = -1.0 mA

Notes:

- (1) I_{SB} = 3 mA (max) for -L versions.
 (2) I_{SB1} and I_{SB2} = 0.02 mA (typ) and 0.1 mA (max) for -L versions.

AC Characteristics

$T_A = 0 \text{ to } +70^\circ\text{C}$; $V_{CC} = +5.0 \text{ V} \pm 10\%$

Parameter	Symbol	μPD431000A-70		μPD431000A-85		μPD431000A-10		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max		
Read Operation									
Read cycle time	t _{RC}	70		85		100		ns	
Address access time	t _{AA}		70		85		100	ns	(Note 2)
$\overline{CE}_1$ access time	t _{CO1}		70		85		100	ns	(Note 2)
CE ₂ access time	t _{CO2}		70		85		100	ns	(Note 2)
Output enable to output valid	t _{OE}		35		45		50	ns	(Note 2)
Output hold from address change	t _{OH}	10		10		10		ns	
$\overline{CE}_1$ to output in low-Z	t _{LZ1}	10		10		10		ns	(Note 3)
CE ₂ to output in low-Z	t _{LZ2}	10		10		10		ns	(Note 3)
Output enable to output in low-Z	t _{OLZ}	5		5		5		ns	(Note 3)
$\overline{CE}_1$ to output in high-Z	t _{HZ1}		25		30		35	ns	(Note 3)
CE ₂ to output in high-Z	t _{HZ2}		25		30		35	ns	(Note 3)
Output enable to output in high-Z	t _{OHZ}		25		30		35	ns	(Note 3)
Write Operation									
Write cycle time	t _{WC}	70		85		100		ns	
$\overline{CE}_1$ to end of write	t _{CW1}	60		75		90		ns	
CE ₂ to end of write	t _{CW2}	60		75		90		ns	
Address valid to end of write	t _{AW}	60		75		90		ns	
Address setup time	t _{AS}	0		0		0		ns	
Write pulse width	t _{WP}	55		65		75		ns	
Write recovery time	t _{WR}	5		5		5		ns	
Data valid to end of write	t _{DW}	35		35		40		ns	
Data hold time	t _{DH}	0		0		0		ns	
Write enable to output in high-Z	t _{WHZ}		25		30		35	ns	(Note 3)
Output active from end of write	t _{OW}	5		5		5		ns	(Note 3)

Notes:

(1) Input pulse levels = 0.8 to 2.2 V; input rise and fall times = 5 ns; timing reference levels = 1.5 V.

(2) See figure 1 for output loading.

(3) See figure 2 for output loading.

Figure 1. Output Loading

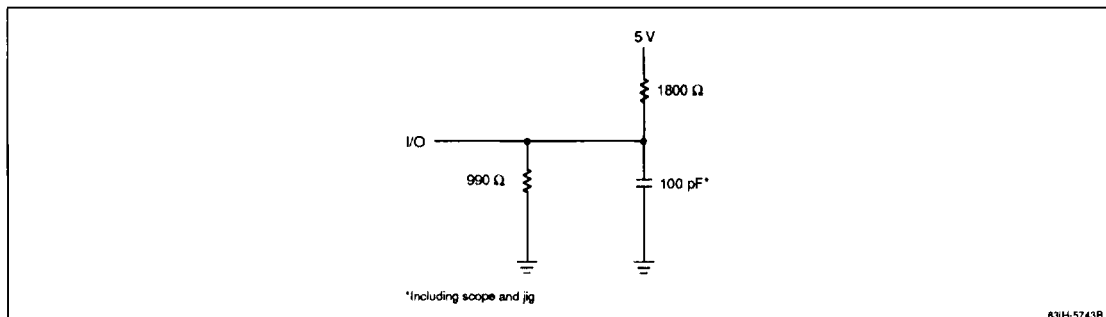
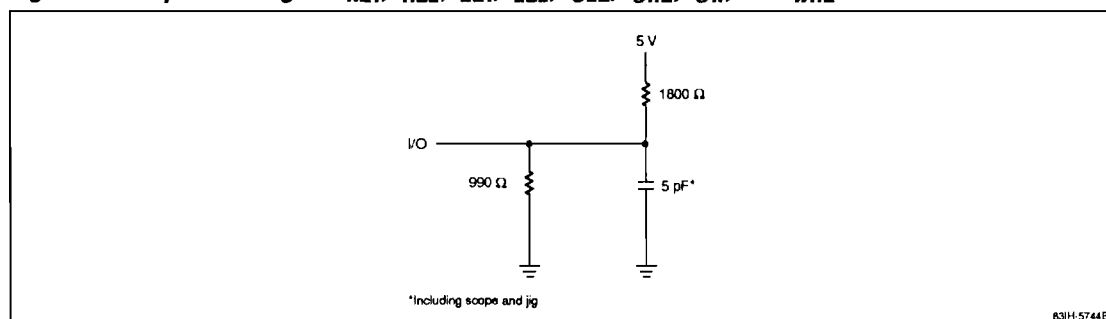


Figure 2. Output Loading for t_{HZ1} , t_{HZ2} , t_{LZ1} , t_{LZ2} , t_{OLZ} , t_{OHZ} , t_{OW} , and t_{WHZ}



Low V_{CC} Data Retention Characteristics (-L Version Only)

$T_A = 0 \text{ to } +70^\circ\text{C}$

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Data retention supply voltage	V_{CCDR1}	2		5.5	V	$\overline{CE}_1 \geq V_{CC} - 0.2 \text{ V}; CE_2 \geq V_{CC} - 0.2 \text{ V}$ or $CE_2 \leq 0.2 \text{ V}$
	V_{CCDR2}	2		5.5	V	$CE_2 \leq 0.2 \text{ V}$
Data retention supply current	I_{CCDR1}		1	50	μA	$V_{CC} = 3.0 \text{ V}; \overline{CE}_1 \geq V_{CC} - 0.2 \text{ V};$ $CE_2 \geq V_{CC} - 0.2 \text{ V}$ or $CE_2 \leq 0.2 \text{ V}$ (Note 1)
	I_{CCDR2}		1	50	μA	$V_{CC} = 3.0 \text{ V}; CE_2 \leq 0.2 \text{ V}$ (Note 1)
Chip deselection to data retention	t_{CDR}	0			ns	
Operation recovery time	t_R	5			ms	

Notes:

(1) At 0 to 40°C , the maximum for I_{CCDR1} and I_{CCDR2} is $15 \mu\text{A}$.

Figure 3. $\overline{CE}_1$ -Controlled Data Retention Timing

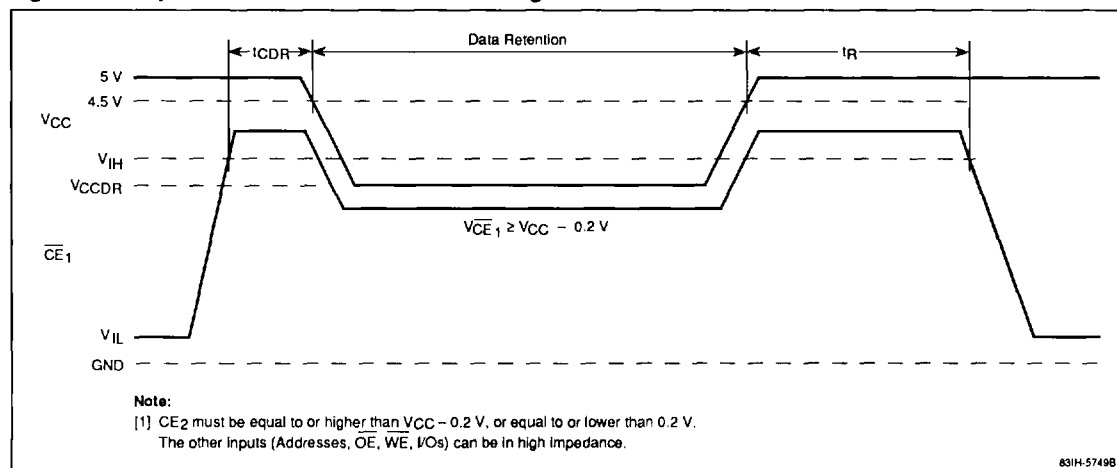
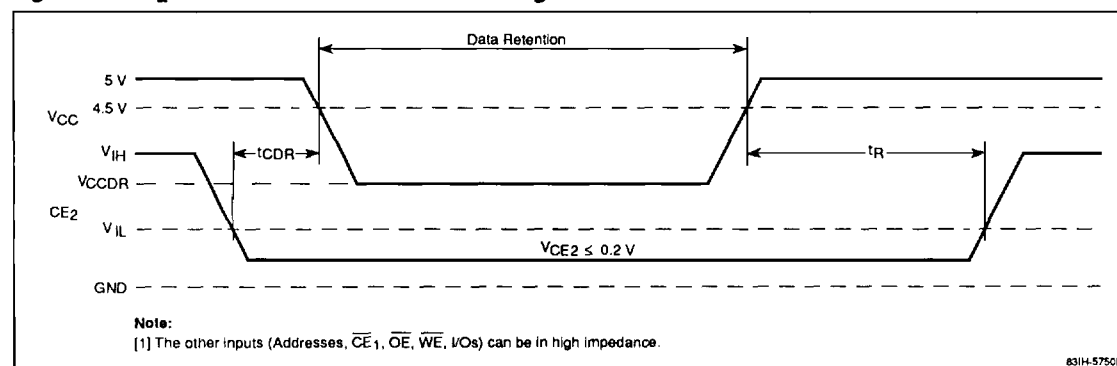
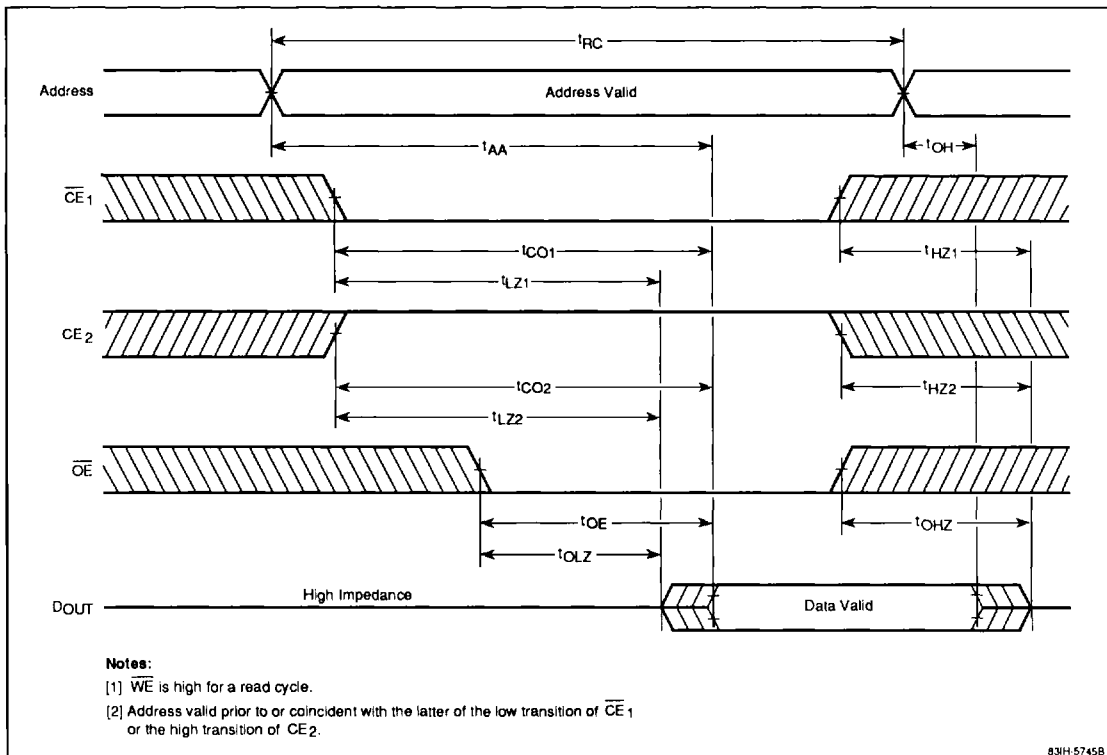


Figure 4. $\overline{CE}_2$ -Controlled Data Retention Timing



Timing Waveforms

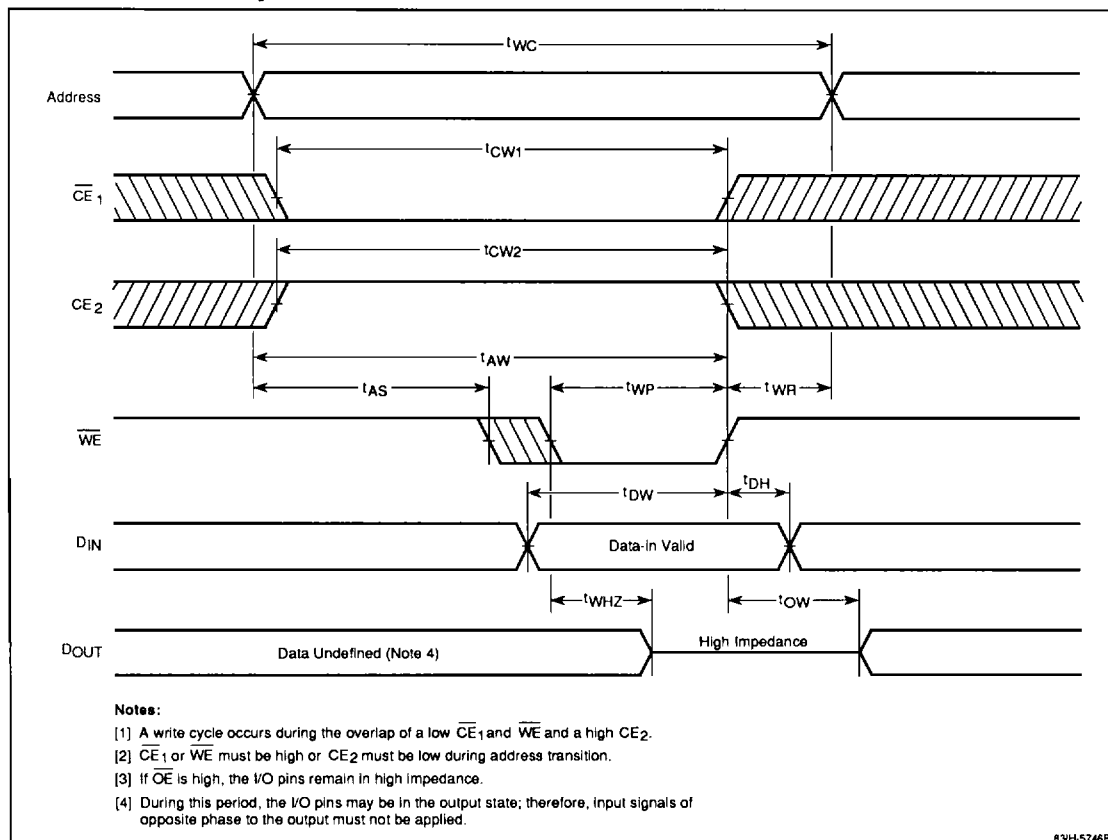
Read Cycle



83H-5745B

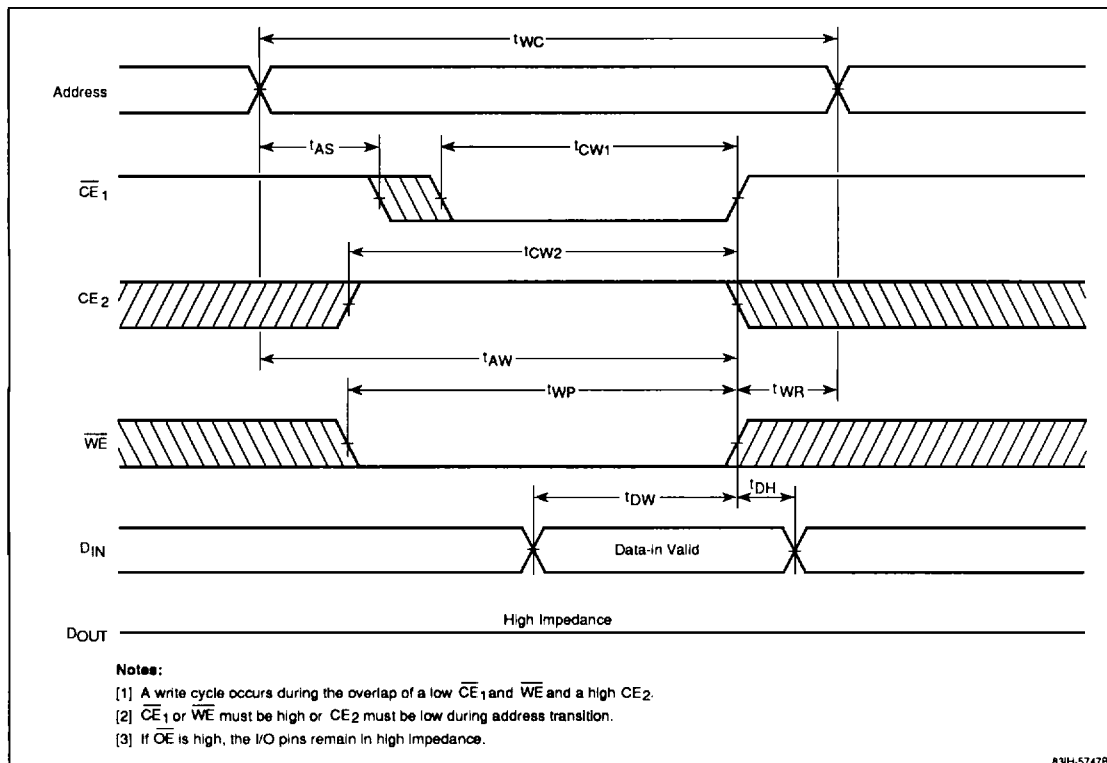
Timing Waveforms (cont)

WE-Controlled Write Cycle



Timing Waveforms (cont)

$\overline{CE}_1$ -Controlled Write Cycle



83H-57476

Timing Waveforms (cont)

CE₂-Controlled Write Cycle

