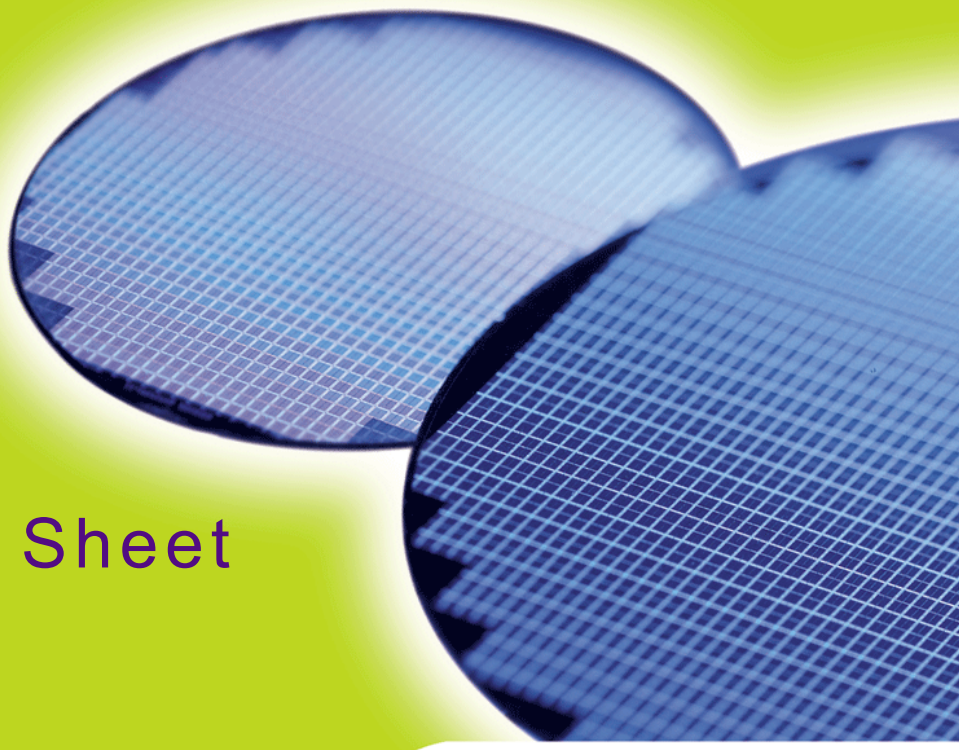
October 2008

IDGV1G-05A1F1C-[40X/45X/50X]

1Gbit x32/x16 GDDR5 SGRAM

EU RoHS compliant



Internet Data Sheet

Rev. 1.01

www.qimonda.com

IDGV1G-05A1F1C-[40X/45X/50X] Revision History:2008-10, Rev. 1.01	
Page	**Subjects (major changes since last revision)**
All	Typos corrected
Previous Revision: Rev. 1.00, 2008-09	
5	Figure1 - Maximum data rate for RDQS mode increased to 3.0 Gbps; PLL-off mode restricted to 4.0 Gbps
Previous Revision: Rev. 0.60, 2008-06	
All	36X speed bin removed
Previous Revision: Rev. 0.50, 2008-05	
All	Adapted Internet version

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1 Overview

1.1 Features

- Monolithic 1Gbit GDDR5 SGRAM (2Mbit x 32 I/O x 16 banks and 4Mbit x 16 I/O x 16 banks)
- x32/x16 mode configuration set at power-up with EDC pin
- Quarter data-rate differential clock inputs CK/$\overline{CK}$ for address and commands
- Two half data-rate differential clock inputs WCK/$\overline{WCK}$, each associated with two data bytes (DQ, $\overline{DBI}$, EDC)
- Single ended interface for data, address and command
- Double Data Rate (DDR) data (WCK)
- Single Data Rate (SDR) command (CK)
- Double Data Rate (DDR) addressing (CK)
- Write data mask function (single/double byte mask) via address bus
- 16 internal banks
- 4 bank groups for t_{CCD} = 3 t_{CK}
- 8n prefetch architecture: 256 bit per array Read or Write access
- Burst Length: 8 only
- Data bus inversion (DBI) and address bus inversion (ABI)
- Input/output PLL on/off mode
- Address training: address input monitoring via DQ pins
- WCK2CK clock training: phase information via EDC pins
- Data read and write training via Read FIFO (FIFO depth = 6)
- Read FIFO pattern preload by LDFF command
- Direct write data load to Read FIFO by WRTR command
- Consecutive read of Read FIFO by RDTR command
- Programmable EDC hold pattern for CDR
- Data Preamble for Read
- Read/Write data transmission integrity secured by cyclic redundancy check (CRC–8)
- Auto Precharge option for each burst access
- Programmable CAS latency: 6 to 20 t_{CK}
- Programmable Write latency: 3 to 7 t_{CK}
- Programmable CRC READ latency: 0 to 2 t_{CK}
- Programmable CRC WRITE latency: 8 to 11 t_{CK}
- Digital t_{RAS} lockout
- RDQS mode on EDC pin
- Data output mode for Vendor ID, density and FIFO depth
- Low Power modes
- On-chip temperature sensor with read-out
- Auto refresh and self refresh modes
- 32ms data retention (8k cycles)
- Automatic temperature sensor controlled self refresh rate
- On-die termination (ODT): nom. values of 60 Ω or 120 Ω
- Pseudo open drain (POD–15) compatible outputs (40 Ω pulldown, 60 Ω pullup)
- ODT and output driver strength auto-calibration with external resistor ZQ pin (120 Ω)
- Programmable termination and driver strength offsets
- Selectable external or internal VREF for data inputs; programmable offsets for internal VREF
- Separate external VREF for address / command inputs
- Boundary Scan function with SEN pin
- Mirror function with MF pin
- V_{DD} 1.5V +/- 0.045 V
- V_{DDQ} 1.5V +/- 0.045 V
- PG-TFBGA 170
- RoHS Compliant Product[1)]

1) RoHS Compliant Product: Restriction of the use of certain hazardous substances (RoHS) in electrical and electronic equipment as defined in the directive 2002/95/EC issued by the European Parliament and of the Council of 27 January 2003. These substances include mercury, lead, cadmium, hexavalent chromium, polybrominated biphenyls and polybrominated biphenyl ethers.

green Product

TABLE 1
Ordering Information

Part Number[1)]	Organization	Max. Data Rate (Gbps/pin)	Package
IDGV1G-05A1F1C – 40X IDGV1G-05A1F1C – 45X IDGV1G-05A1F1C – 50X	×32 / x16	4.0 4.5 5.0	PG-TFBGA 170

1) I: Qimonda Identifier, D: DRAM, GV: GDDR5, 1G: 1Gbit, 0: 1 x CS, 5: x32, A1: 1st node, F1: FBGA, C: Commercial 0° - 85/95°C

1.2 Description

The Qimonda GDDR5 SGRAM is a high speed dynamic random-access memory designed for applications requiring high bandwidth. It contains 1,073,741,824 bits and is internally configured as a 16-bank DRAM.

The GDDR5 SGRAM uses a 8n prefetch architecture and DDR interface to achieve high-speed operation. It can be configured to operate in x32 mode or x16 (clamshell) mode. The mode is detected during device initialization. The GDDR5 interface transfers two 32 bit wide data words per WCK clock cycle to/from the I/O pins. Corresponding to the 8n prefetch a single write or read access consists of a 256 bit wide, two CK clock cycle data transfer at the internal memory core and eight corresponding 32 bit wide one-half WCK clock cycle data transfers at the I/O pins.

The GDDR5 SGRAM operates from a differential clock CK and $\overline{CK}$. Commands are registered at every rising edge of CK. Addresses are registered at every rising edge of CK and every rising edge of $\overline{CK}$.

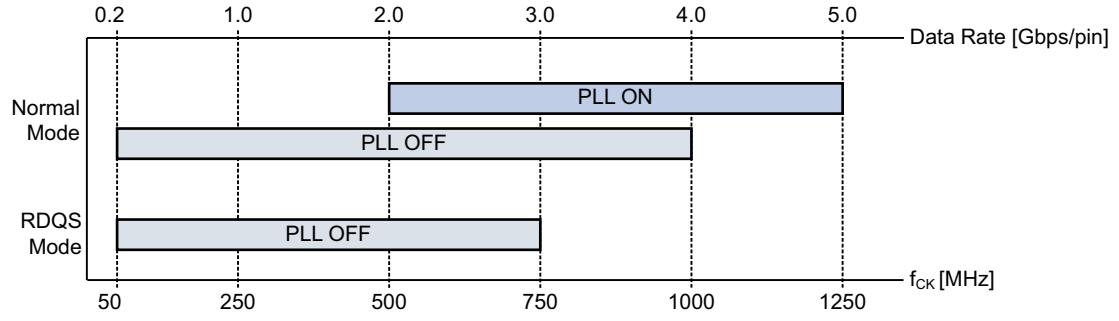
GDDR5 replaces the pulsed strobes (WDQS & RDQS) used in previous DRAMs such as GDDR4 with a free running differential forwarded clock (WCK/$\overline{WCK}$) with both input and output data registered and driven respectively at both edges of the forwarded WCK.

Read and write accesses to the GDDR5 SGRAM are burst oriented; accesses start at a selected location and continue for a total of eight data words. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command and the next rising $\overline{CK}$ edge are used to select the bank and the row to be accessed. The address bits registered coincident with the READ or WRITE command and the next rising $\overline{CK}$ edge are used to select the bank and the column location for the burst access.

1.3 Operating Frequency Ranges

Figure 1 provides an overview of the operating frequency ranges for PLL-on and PLL-off operation in normal and RDQS modes. See for a complete list of AC timing parameters, for PLL-on and PLL-off operation. PLL-off mode is supported for all frequencies. It requires the same interface trainings to be performed.

FIGURE 1
Operating Modes and Frequency Ranges



2 Configuration

2.1 Signal Description

TABLE 2
Signal Description

Signal	Type	Detailed Function
CK, $\overline{CK}$	Input	**Clock:** CK and $\overline{CK}$ are differential clock inputs. Command inputs are latched on the rising edge of CK. Address inputs are latched on the rising edge of CK and the rising edge of $\overline{CK}$. All latencies are referenced to CK. CK and $\overline{CK}$ are externally terminated.
WCK01, $\overline{WCK01}$, WCK23, $\overline{WCK23}$	Input	**Data Clocks:** WCK and $\overline{WCK}$ are differential clocks used for WRITE data capture and READ data output. WCK01/$\overline{WCK01}$ is associated with DQ0-DQ15, $\overline{DBI0}$, $\overline{DBI1}$, EDC0 and EDC1. WCK23/$\overline{WCK23}$ is associated with DQ16-DQ31, $\overline{DBI2}$, $\overline{DBI3}$, EDC2 and EDC3. WCK clocks operate at nominally twice the CK clock frequency.
$\overline{CKE}$	Input	**Clock Enable:** $\overline{CKE}$ LOW activates and $\overline{CKE}$ HIGH deactivates internal clock, device input buffers and output drivers. Taking $\overline{CKE}$ HIGH provides Precharge Power-Down and Self Refresh operations (all banks idle), or Active Power-Down (row active in any bank). $\overline{CKE}$ is synchronous for Power-Down entry and exit and for Self Refresh entry and exit. CKE must be maintained LOW throughout READ and WRITE accesses. Input buffers excluding CK, $\overline{CK}$, $\overline{CKE}$, WCK01, $\overline{WCK01}$, WCK23, $\overline{WCK23}$ are disabled during Power-Down. Input buffers excluding $\overline{CKE}$ are disabled during Self Refresh. The value of $\overline{CKE}$ latched at power-up with $\overline{RESET}$ going HIGH determines the termination value of the address and command inputs.
$\overline{CS}$	Input	**Chip Select:** $\overline{CS}$ LOW enables, and $\overline{CS}$ HIGH disables the command decoder. All commands are masked when $\overline{CS}$ is registered HIGH, but internal command execution continues. $\overline{CS}$ provides for individual device selection on memory channels with multiple memory devices. $\overline{CS}$ is considered part of the command code.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	**Command inputs:** $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ (along with $\overline{CS}$) define the command to be entered.
BA0 - BA3	Input	**Bank Address inputs:** BA0-BA3 select to which internal bank an ACTIVE, READ, WRITE or PRECHARGE command is being applied. BA0-BA3 also determine which Mode Register is accessed with a MODE REGISTER SET command. BA0-BA3 are sampled with the rising edge of CK.
A0 - A11	Input	**Address inputs:** A0-A11 provide the row address for ACTIVE commands. A0-A5(A6) provide the column address and A8 defines the auto precharge function for READ and WRITE commands, to select one location out of the memory array in the respective bank. The address inputs also provide the op-code during a MODE REGISTER SET command, and the data bits during LDFF commands. A8-A11 are sampled with the rising edge of CK and A0-A7 are sampled with the rising edge of $\overline{CK}$.
DQ0 - DQ31	I/O	**Data Input/Output:** 32 bit data bus
$\overline{DBI0}$ - $\overline{DBI3}$	I/O	**Data bus inversion:** $\overline{DBI0}$ is associated with DQ0-DQ7, $\overline{DBI1}$ with DQ8-DQ15, $\overline{DBI2}$ with DQ16-DQ23, and $\overline{DBI3}$ with DQ24-DQ31.

Signal	Type	Detailed Function
EDC0 - EDC3	Output	**Error Detection Code:** The calculated CRC data is transmitted on these pins. Used also for x16 mode detection, EDC hold pattern and RDQS function. EDC0 is associated with DQ0-DQ7, EDC1 with DQ8-DQ15, EDC2 with DQ16-DQ23, and EDC3 with DQ24-DQ31.
$\overline{\text{ABI}}$	Input	**Address bus inversion**
ZQ	-	**Impedance Reference:** external reference pin for auto-calibration
$\overline{\text{RESET}}$	Input	**Reset:** $\overline{\text{RESET}}$ is a V_{DDQ} CMOS input. $\overline{\text{RESET}}$ LOW asynchronously initiates a full chip reset. With $\overline{\text{RESET}}$ LOW all ODTs are disabled.
MF	Input	**Mirror Function:** MF is a V_{DDQ} CMOS input. Must be tied to Power or Ground.
SEN	Input	**Scan Enable**: SEN is a V_{DDQ} CMOS input. Must be tied to Ground when not in use.
V_{REFC}	Supply	**Reference voltage** for command and address inputs.
V_{REFD}	Supply	**Reference voltage** for DQ and $\overline{\text{DBI}}$ inputs.
V_{DD}, V_{SS}	Supply	Power and Ground for the internal logic.
V_{DDQ}, V_{SSQ}	Supply	Isolated power and ground for the input and output buffers.
NC	-	Not Connected.

2.2 Ballout and Mirror Function Mode

The GDDR5 SGRAM provides a mirror function (MF) pin to change the physical location of command, address, data and WCK pins and assist in routing devices back to back. The pins affected by this Mirror Function mode are listed in **Table 3**. **Figure 2** and **Figure 3** show the ballouts for non-mirrored (MF=0) and mirrored (MF=1) modes.

TABLE 3
Ball Assignment with Mirror Function

Ball	Signal		Ball	Signal		Ball	Signal		Ball	Signal		Ball	Signal	
	MF=0	MF=1		MF=0	MF=1		MF=0	MF=1		MF=0	MF=1		MF=0	MF=1
A2	DQ1	DQ25	G3	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	T4	DQ26	DQ2	H11	BA0 A2	BA2 A4	E13	DQ13	DQ21
B2	DQ3	DQ27	L3	$\overline{\text{CAS}}$	$\overline{\text{RAS}}$	U4	DQ24	DQ0	K11	BA2 A4	BA0 A2	F13	DQ15	DQ23
C2	EDC0	EDC3	A4	DQ0	DQ24	D5	$\overline{\text{WCK01}}$	$\overline{\text{WCK23}}$	M11	DQ22	DQ14	M13	DQ23	DQ15
D2	$\overline{\text{DBI0}}$	$\overline{\text{DBI3}}$	B4	DQ2	DQ26	H5	A9 A1	A11 A6	N11	DQ20	DQ12	N13	DQ21	DQ13
E2	DQ5	DQ29	D4	WCK01	WCK23	K5	A11 A6	A9 A1	T11	DQ18	DQ10	P13	$\overline{\text{DBI2}}$	$\overline{\text{DBI1}}$
F2	DQ7	DQ31	E4	DQ4	DQ28	P5	$\overline{\text{WCK23}}$	$\overline{\text{WCK01}}$	U11	DQ16	DQ8	R13	EDC2	EDC1
M2	DQ31	DQ7	F4	DQ6	DQ30	H10	BA3 A3	BA1 A5	G12	$\overline{\text{CS}}$	$\overline{\text{WE}}$	T13	DQ19	DQ11
N2	DQ29	DQ5	H4	A10 A0	A8 A7	K10	BA1 A5	BA3 A3	L12	$\overline{\text{WE}}$	$\overline{\text{CS}}$	U13	DQ17	DQ9
P2	$\overline{\text{DBI3}}$	$\overline{\text{DBI0}}$	K4	A8 A7	A10 A0	A11	DQ8	DQ16	A13	DQ9	DQ17			
R2	EDC3	EDC0	M4	DQ30	DQ6	B11	DQ10	DQ18	B13	DQ11	DQ19			
T2	DQ27	DQ3	N4	DQ28	DQ4	E11	DQ12	DQ20	C13	EDC1	EDC2			
U2	DQ25	DQ1	P4	WCK23	WCK01	F11	DQ14	DQ22	D13	$\overline{\text{DBI1}}$	$\overline{\text{DBI2}}$			

Functions within the GDDR5 SGRAM that refer to external signals are transparent with respect to Mirror Function mode, meaning that the signal names shown in the respective functional description apply both to mirrored (MF=1) and non-mirrored (MF=0) modes. The referenced package pin is determined by the Mirror Function mode the devices is configured to.

FIGURE 2
Ballout, MF = 0 (Top View)

1	2	3	4	5		10	11	12	13	14
V_{SSQ}	DQ1	V_{SSQ}	DQ0	NC	A	VREFD	DQ8	V_{SSQ}	DQ9	V_{SSQ}
V_{DDQ}	DQ3	V_{DDQ}	DQ2	V_{SS}	B	V_{SS}	DQ10	V_{DDQ}	DQ11	V_{DDQ}
V_{SSQ}	EDC0	V_{SSQ}	V_{SSQ}	V_{DD}	C	V_{DD}	V_{SSQ}	V_{SSQ}	EDC1	V_{SSQ}
V_{DDQ}	$\overline{DBI0}$	V_{DDQ}	WCK01	$\overline{WCK01}$	D	V_{SS}	V_{DD}	V_{DDQ}	$\overline{DBI1}$	V_{DDQ}
V_{SSQ}	DQ5	V_{SSQ}	DQ4	V_{DDQ}	E	V_{DDQ}	DQ12	V_{SSQ}	DQ13	V_{SSQ}
V_{DDQ}	DQ7	V_{DDQ}	DQ6	V_{SSQ}	F	V_{SSQ}	DQ14	V_{DDQ}	DQ15	V_{DDQ}
V_{DD}	V_{DDQ}	$\overline{RAS}$	V_{DD}	V_{SS}	G	V_{SS}	V_{DD}	$\overline{CS}$	V_{DDQ}	V_{DD}
V_{SS}	V_{SSQ}	V_{DDQ}	A10 A0	A9 A1	H	BA3 A3	BA0 A2	V_{DDQ}	V_{SSQ}	V_{SS}
MF	$\overline{RESET}$	$\overline{CKE}$	$\overline{ABI}$	NC	J	SEN	$\overline{CK}$	CK	ZQ	VREFC
V_{SS}	V_{SSQ}	V_{DDQ}	A8 A7	A11 A6	K	BA1 A5	BA2 A4	V_{DDQ}	V_{SSQ}	V_{SS}
V_{DD}	V_{DDQ}	$\overline{CAS}$	V_{DD}	V_{SS}	L	V_{SS}	V_{DD}	$\overline{WE}$	V_{DDQ}	V_{DD}
V_{DDQ}	DQ31	V_{DDQ}	DQ30	V_{SSQ}	M	V_{SSQ}	DQ22	V_{DDQ}	DQ23	V_{DDQ}
V_{SSQ}	DQ29	V_{SSQ}	DQ28	V_{DDQ}	N	V_{DDQ}	DQ20	V_{SSQ}	DQ21	V_{SSQ}
V_{DDQ}	$\overline{DBI3}$	V_{DDQ}	WCK23	$\overline{WCK23}$	P	V_{SS}	V_{DD}	V_{DDQ}	$\overline{DBI2}$	V_{DDQ}
V_{SSQ}	EDC3	V_{SSQ}	V_{SSQ}	V_{DD}	R	V_{DD}	V_{SSQ}	V_{SSQ}	EDC2	V_{SSQ}
V_{DDQ}	DQ27	V_{DDQ}	DQ26	V_{SS}	T	V_{SS}	DQ18	V_{DDQ}	DQ19	V_{DDQ}
V_{SSQ}	DQ25	V_{SSQ}	DQ24	NC	U	VREFD	DQ16	V_{SSQ}	DQ17	V_{SSQ}

= pin is OFF when configured to x16 mode

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FIGURE 3
Ballout, MF = 1 (Top View)

1	2	3	4	5		10	11	12	13	14
V_{SSQ}	DQ25	V_{SSQ}	DQ24	NC	A	VREFD	DQ16	V_{SSQ}	DQ17	V_{SSQ}
V_{DDQ}	DQ27	V_{DDQ}	DQ26	V_{SS}	B	V_{SS}	DQ18	V_{DDQ}	DQ19	V_{DDQ}
V_{SSQ}	EDC3	V_{SSQ}	V_{SSQ}	V_{DD}	C	V_{DD}	V_{SSQ}	V_{SSQ}	EDC2	V_{SSQ}
V_{DDQ}	$\overline{DBI3}$	V_{DDQ}	WCK23	$\overline{WCK23}$	D	V_{SS}	V_{DD}	V_{DDQ}	$\overline{DBI2}$	V_{DDQ}
V_{SSQ}	DQ29	V_{SSQ}	DQ28	V_{DDQ}	E	V_{DDQ}	DQ20	V_{SSQ}	DQ21	V_{SSQ}
V_{DDQ}	DQ31	V_{DDQ}	DQ30	V_{SSQ}	F	V_{SSQ}	DQ22	V_{DDQ}	DQ23	V_{DDQ}
V_{DD}	V_{DDQ}	$\overline{CAS}$	V_{DD}	V_{SS}	G	V_{SS}	V_{DD}	$\overline{WE}$	V_{DDQ}	V_{DD}
V_{SS}	V_{SSQ}	V_{DDQ}	A8 A7	A11 A6	H	BA1 A5	BA2 A4	V_{DDQ}	V_{SSQ}	V_{SS}
MF	$\overline{RESET}$	$\overline{CKE}$	$\overline{ABI}$	NC	J	SEN	$\overline{CK}$	CK	ZQ	VREFC
V_{SS}	V_{SSQ}	V_{DDQ}	A10 A0	A9 A1	K	BA3 A3	BA0 A2	V_{DDQ}	V_{SSQ}	V_{SS}
V_{DD}	V_{DDQ}	$\overline{RAS}$	V_{DD}	V_{SS}	L	V_{SS}	V_{DD}	$\overline{CS}$	V_{DDQ}	V_{DD}
V_{DDQ}	DQ7	V_{DDQ}	DQ6	V_{SSQ}	M	V_{SSQ}	DQ14	V_{DDQ}	DQ15	V_{DDQ}
V_{SSQ}	DQ5	V_{SSQ}	DQ4	V_{DDQ}	N	V_{DDQ}	DQ12	V_{SSQ}	DQ13	V_{SSQ}
V_{DDQ}	$\overline{DBI0}$	V_{DDQ}	WCK01	$\overline{WCK01}$	P	V_{SS}	V_{DD}	V_{DDQ}	$\overline{DBI1}$	V_{DDQ}
V_{SSQ}	EDC0	V_{SSQ}	V_{SSQ}	V_{DD}	R	V_{DD}	V_{SSQ}	V_{SSQ}	EDC1	V_{SSQ}
V_{DDQ}	DQ3	V_{DDQ}	DQ2	V_{SS}	T	V_{SS}	DQ10	V_{DDQ}	DQ11	V_{DDQ}
V_{SSQ}	DQ1	V_{SSQ}	DQ0	NC	U	VREFD	DQ8	V_{SSQ}	DQ9	V_{SSQ}

= pin is OFF when configured to x16 mode

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2.3 Addressing

The GDDR5 SGRAM uses a DDR address scheme to reduce pins required on the GDDR5 SGRAM as shown in **Table 4**. The address should be provided to the GDDR5 SGRAM in two parts; the first half is latched on the rising edge of CK along with the command pins such as $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$; the second half is latched on the rising edge of $\overline{CK}$.

The use of DDR addressing allows all address values to be latched in at the same rate as the SDR commands. All addresses related to command access have been positioned for latching on the initial rising edge for faster decoding.

TABLE 4
Address Pairs

Clock Edge	Address Inputs							
Rising CK	A8	A11	BA1	BA2	BA3	BA0	A9	A10
Rising $\overline{CK}$	A7	A6	A5	A4	A3	A2	A1	A0

Two addressing schemes are supported for x32 mode and x16 mode, which differ only in the number of valid column addresses, as shown in **Table 5**.

TABLE 5
Addressing Scheme

	32Mx32	64Mx16
Row Address	A0-A11	A0-A11
Column addresses	A0-A5	A0-A6
Number of Banks	16	16
Bank address	BA0-BA3	BA0-BA3
Autoprecharge	A8	A8
Refresh	8K/32 ms	8K/32 ms
Refresh period	3.9 µs	3.9 µs
Page size	2 KB	2 KB
Bank Groups	4	4

2.4 Commands

TABLE 6
Command Truth Table

Operation	Code	$\overline{CKE}$ n-1	$\overline{CKE}$ n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA3-BA0	A11	A10	A8	A6-A7, A9	A0-A5 (A6)	Note
Device Deselect	DESEL	L	L	H	X	X	X	X	X	X	X	X	X	1)2)8)
No Operation	NOP	L	L	L	H	H	H	X	X	X	X	X	X	1)2)8)
Mode Register Set	MRS	L	L	L	L	L	L	MRA	OPCODE					1)2)3)
Bank Activate	ACT	L	L	L	L	H	H	BA	Row Address					1)2)4)
Read	RD	L	L	L	H	L	H	BA	L	L	L	X	CA	1)2)5)9)
Read with Autoprecharge	RDA	L	L	L	H	L	H	BA	L	L	H	X	CA	1)2)5)
Load FIFO	LDFF	L	L	L	H	L	H	BST	H	L	L	DATA		1)2)7)
Read Training	RDTR	L	L	L	H	L	H	X	H	H	L	X	X	1)2)
Write	WR	L	L	L	H	L	L	BA	L	L	L	X	CA	1)2)5)
Write with Autoprecharge	WRA	L	L	L	H	L	L	BA	L	L	H	X	CA	1)2)5)
Write with Single Byte Mask	WSM	L	L	L	H	L	L	BA	L	H	L	X	CA	1)2)5)
Write with Autoprecharge, Single Byte Mask	WSMA	L	L	L	H	L	L	BA	L	H	H	X	CA	1)2)5)
Write with Double Byte Mask	WDM	L	L	L	H	L	L	BA	H	L	L	X	CA	1)2)5)
Write with Autoprecharge, Double Byte Mask	WDMA	L	L	L	H	L	L	BA	H	L	H	X	CA	1)2)5)
Write Training	WRTR	L	L	L	H	L	L	X	H	H	L	X	X	1)2)
Precharge	PRE	L	L	L	L	H	L	BA	X	X	L	X	X	1)2)
Precharge All	PREALL	L	L	L	L	H	L	X	X	X	H	X	X	1)2)
Refresh	REF	L	L	L	L	L	H	X	X	X	X	X	X	1)6)
Power Down Mode Entry	PDE	L	H	H	X	X	X	X	X	X	X	X	X	1)
				L	H	H	H							
Power Down Mode Exit	PDX	H	L	H	X	X	X	X	X	X	X	X	X	1)
				L	H	H	H							
Self Refresh Entry	SRE	L	H	L	L	L	H	X	X	X	X	X	X	1)6)
Self Refresh Exit	SRX	H	L	H	X	X	X	X	X	X	X	X	X	1)
				L	H	H	H							

1) H = logic H level; L = logic L level; X = Don't Care. Signal may be H or L, but not floating
2) Addresses shown are logical addresses; physical addresses are inverted when address bus inversion (ABI) is activated and $\overline{ABI}$=L
3) BA0-BA3 provide the Mode Register address (MRA), A0-A11 the opcode to be loaded
4) BA0-BA3 provide the bank address (BA), A0-A11 provide the row address (RA)
5) BA0-BA3 provide the bank address, A0-A5 (A6) provide the column address (CA); no sub-word addressing within a burst of 8
6) This command is REFRESH when CKE(n) = L, and Self Refresh Entry when CKE(n) is H
7) BA0-BA3 and CA are used to select burst location (BST) and data respectively
8) DESELECT and NO OPERATION are functionally interchangeable
9) In address training mode READ is decoded from the command pins only with RAS = H, CAS = L, WE = H

3 Mode Registers

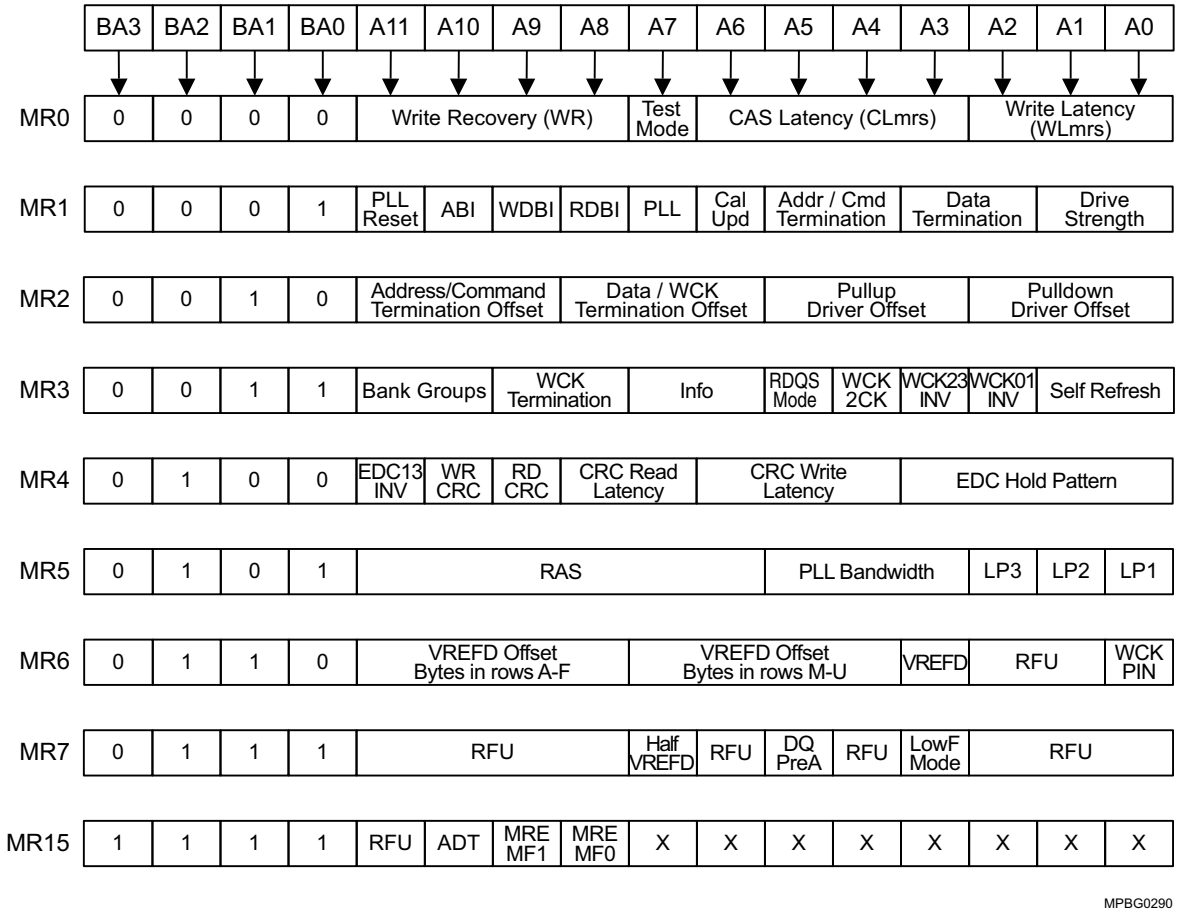
The Mode Registers define the specific mode of operation. MR0 to MR7 and MR15 are defined as shown in the overview in **Figure 4**. MR8 to MR14 are not used.

All Mode Registers are programmed via the MODE REGISTER SET (MRS) command and will retain the stored information until they are reprogrammed or a subsequent reset. Mode Registers must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time t_{MRD} before initiating any subsequent operation. Violating either of these requirements will result in unspecified operation.

All Mode Registers are initialized upon reset with all 0's (exception: MR4, bits A0-A3: '1111'). However, the user shall program all Mode Registers to the desired values e.g upon device initialization.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result. RFU bits are reserved for future use and must be programmed to 0.

FIGURE 4
Mode Registers Overview



4 Electrical Characteristics

4.1 Absolute Maximum Ratings

TABLE 7
Absolute Maximum Ratings

Parameter	Symbol	Ratings		Unit
		Min.	Max.	
Device supply voltage	V_{DD}	-0.5	2.0	V
Output buffer supply voltage	V_{DDQ}	-0.5	2.0	V
Input Voltage	V_{IN}	-0.5	2.0	V
Output Voltage	V_{OUT}	-0.5	2.0	V
Storage Temperature	T_{STG}	-55	+150	°C
Junction Temperature	T_J	—	+125	°C
Short Circuit Output Current	I_{OUT}	—	50	mA

Attention: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of these specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

4.2 Operation Conditions

TABLE 8
DC Operating Conditions

Parameter [1]	Symbol	POD-15			Unit	Notes
		Min.	Typ.	Max.		
Device supply voltage	V_{DD}	1.455	1.5	1.545	V	2)
Output supply voltage	V_{DDQ}	1.455	1.5	1.545	V	2)
Reference voltage for DQ/$\overline{\text{DBI}}$ inputs	V_{REFD}	0.69 * V_{DDQ}		0.71 * V_{DDQ}	V	3)4)
Reference voltage for DQ/$\overline{\text{DBI}}$ inputs	V_{REFD2}	0.49 * V_{DDQ}		0.51 * V_{DDQ}	V	3)4)5)
Reference voltage for command and address inputs	V_{REFC}	0.69 * V_{DDQ}		0.71 * V_{DDQ}	V	6)
Input logic high voltage for address/command inputs	$V_{IHA(DC)}$	V_{REFC} + 0.15		—	V	
Input logic low voltage for address/command inputs	$V_{ILA(DC)}$	—		V_{REFC} - 0.15	V	
Input logic high voltage for DQ/$\overline{\text{DBI}}$ inputs with V_{REFD}	$V_{IHD(DC)}$	V_{REFD} + 0.1		—	V	
Input logic low voltage for DQ/$\overline{\text{DBI}}$ inputs with V_{REFD}	$V_{ILD(DC)}$	—		V_{REFD} - 0.1	V	
Input logic high voltage for DQ/$\overline{\text{DBI}}$ inputs with V_{REFD2}	$V_{IHD2(DC)}$	V_{REFD2} + 0.3		—	V	
Input logic low voltage for DQ/$\overline{\text{DBI}}$ inputs with V_{REFD2}	$V_{ILD2(DC)}$	—		V_{REFD2} - 0.3	V	
Input logic high voltage for $\overline{\text{RESET}}$, SEN + MF inputs	V_{IHR}	V_{DDQ} - 0.5		—	V	
Input logic low voltage for $\overline{\text{RESET}}$, SEN + MF inputs	V_{ILR}	—		0.3	V	
Input logic high voltage for EDC1/2 (x16 mode detect)	V_{IHX}	V_{DDQ} - 0.3		—	V	7)
Input logic low voltage for EDC1/2 (x16 mode detect)	V_{ILX}	—		0.3	V	7)
CK, $\overline{\text{CK}}$, WCK and $\overline{\text{WCK}}$ single ended input voltage	V_{INCK}	- 0.3		V_{DDQ} + 0.3	V	
Clock input mid-point voltage	$V_{MP(DC)}$	V_{REFC} - 0.1		V_{REFC} + 0.1	V	8)9)10)11)
CK/$\overline{\text{CK}}$ DC input differential voltage	$V_{IDCK(DC)}$	0.22		—	V	9)11)12)
WCK/$\overline{\text{WCK}}$ DC input differential voltage	$V_{IDWCK(DC)}$	0.2		—	V	9)13)14)
Input leakage current (any input 0 V ≤ V_{IN} ≤ V_{DDQ}; all other pins not under test = 0 V)	I_{IL}	-5		+5	µA	15)
Output leakage current (DQs are disabled; 0 V ≤ V_{OUT} ≤ V_{DDQ})	I_{OZ}	-5		+5	µA	
Output logic low voltage	$V_{OL(DC)}$	—		0.62	V	
External resistor value	ZQ	115	120	125	Ω	

1) 0°C ≤ Tc ≤ 95°C. All voltages are measured at the package pins.
2) GDDR5 SGRAMs are designed to tolerate PCB designs with separate V_{DDQ} and V_{DD} power regulators.
3) AC noise in the system is estimated at 50mV peak-to-peak for the purpose of DRAM design.
4) Source of reference voltage and control of Reference voltage for DQ and $\overline{\text{DBI}}$ pins is determined by VREFD, Half VREFD and VREFD Offset Mode Registers.
5) VREFD Offsets are not supported with V_{REFD2}.
6) External V_{REFC} is to be provided by the controller as there is no alternative supply.
7) V_{IHX} and V_{ILX} define the input voltage levels for the receiver that detects x32 mode or x16 mode with $\overline{\text{RESET}}$ going HIGH..
8) This provides a minimum of 0.95V and a maximum of 1.15V, and is always 70% of V_{DDQ} with POD-15. DRAM timings relative to CK cannot be guaranteed if these limits are exceeded. .
9) For AC operations, all DC clock requirements must be satisfied as well.

10) The value of V_{IXCK} and V_{IXWCK} is expected to equal 70% of V_{DDQ} for the transmitting device and must track variations of the DC level of the same.
11) The CK and $\overline{CK}$ input reference level (for timing referenced to CK and $\overline{CK}$) is the point at which CK and $\overline{CK}$ cross.
12) V_{IDCK} is the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$.
13) The WCK and $\overline{WCK}$ input reference level (for timing referenced to WCK and $\overline{WCK}$) is the point at which WCK and $\overline{WCK}$ cross.
14) V_{IDWCK} is the magnitude of the difference between the input level on WCK and the input level on $\overline{WCK}$.
15) I_{IL} and I_{OL} are measured with ODT off.

TABLE 9
AC Operating Conditions

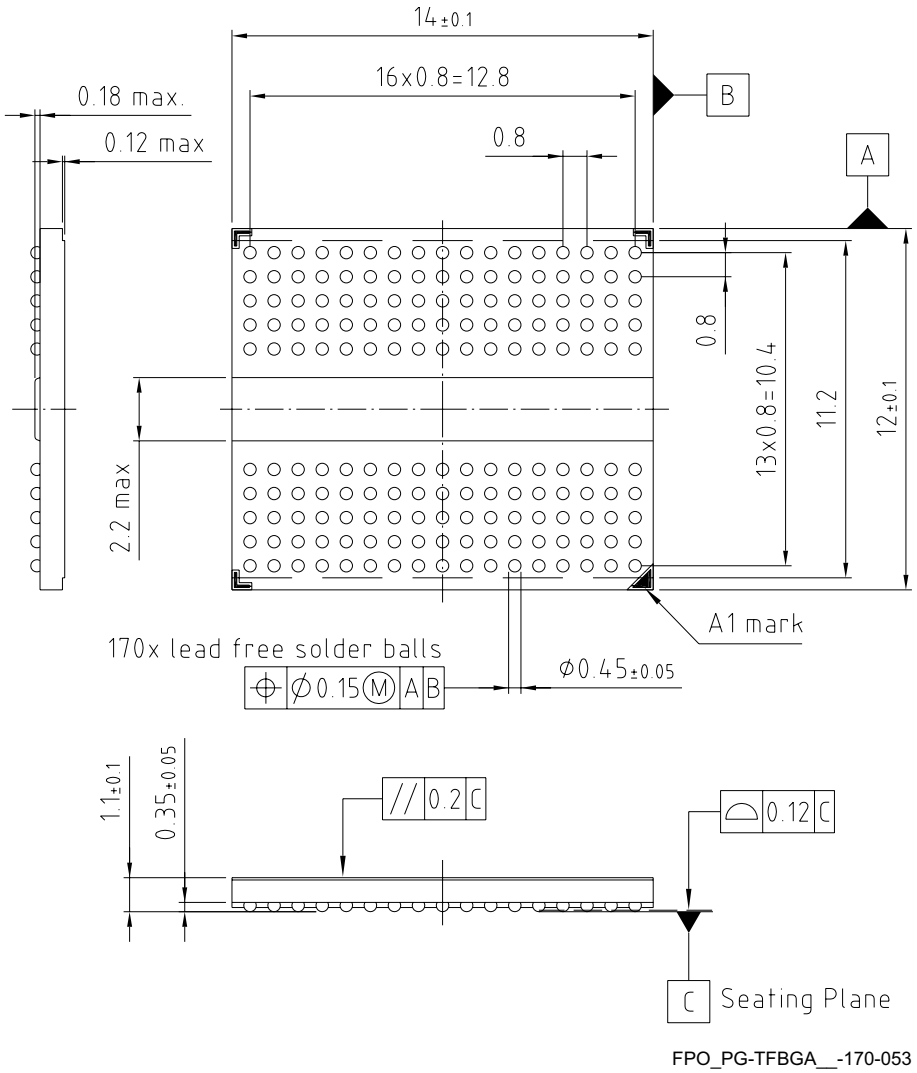
Parameter [1)2)]	Symbol	POD-15			Unit	Notes
		Min.	Typ.	Max.		
Input logic high voltage for address/command inputs	$V_{IHA(AC)}$	V_{REFC} + 0.2		—	V	
Input logic low voltage for address/command inputs	$V_{ILA(AC)}$	—		V_{REFC} - 0.2	V	
Input logic high voltage for DQ/$\overline{DBI}$ inputs with V_{REFD}	$V_{IHD(AC)}$	V_{REFD} + 0.15		—	V	
Input logic low voltage for DQ/$\overline{DBI}$ inputs with V_{REFD}	$V_{ILD(AC)}$	—		V_{REFD} - 0.15	V	
Input logic high voltage for DQ/$\overline{DBI}$ inputs with V_{REFD2}	$V_{IHD2(AC)}$	V_{REFD} + 0.4		—	V	
Input logic low voltage for DQ/$\overline{DBI}$ inputs with V_{REFD2}	$V_{ILD2(AC)}$	—		V_{REFD} - 0.4	V	
CK/$\overline{CK}$ input differential voltage	$V_{IDCK(AC)}$	0.4		—	V	3)4)
WCK/$\overline{WCK}$ input differential voltage	$V_{IDWCK(AC)}$	0.3		—	V	5)6)
CK/$\overline{CK}$ input crossing point voltage	$V_{IXCK(AC)}$	V_{REFC} - 0.12		V_{REFC} + 0.12	V	3)7)
WCK/$\overline{WCK}$ input crossing point voltage	$V_{IXWCK(AC)}$	V_{REFD} - 0.1		V_{REFD} + 0.1	V	5)7)

1) 0°C ≤ Tc ≤ 95°C. All voltages are measured at the package pins.
2) For optimum performance it is recommended that signal swings are larger than shown in the table.
3) The CK and $\overline{CK}$ input reference level (for timing referenced to CK and $\overline{CK}$) is the point at which CK and $\overline{CK}$ cross.
4) V_{IDCK} is the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$.
5) The WCK and $\overline{WCK}$ input reference level (for timing referenced to WCK and $\overline{WCK}$) is the point at which WCK and $\overline{WCK}$ cross..
6) V_{IDWCK} is the magnitude of the difference between the input level on WCK and the input level on $\overline{WCK}$.
7) The value of V_{IXCK} and V_{IXWCK} is expected to equal 70% of V_{DDQ} for the transmitting device and must track variations of the DC level of the same.

5 Package

5.1 Package Outline

FIGURE 5
Package Outline



List of Illustrations

List of Tables

Contents

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