HN58S65A Series

64 k EEPROM (8-kword × 8-bit)
Ready/$\overline{\text{Busy}}$ Function

REJ03C0152-0100Z
(Previous ADE-203-691A(Z) Rev.0.3)
Rev. 1.00
Feb.03.2004

Description

Renesas Technology's HN58S65A series is an electrically erasable and programmable ROM organized as 8192-word × 8-bit. It has realized high speed, low power consumption and high reliability by employing advanced MNOS memory technology and CMOS process and circuitry technology. They also have a 64-byte page programming function to make their write operations faster.

Features

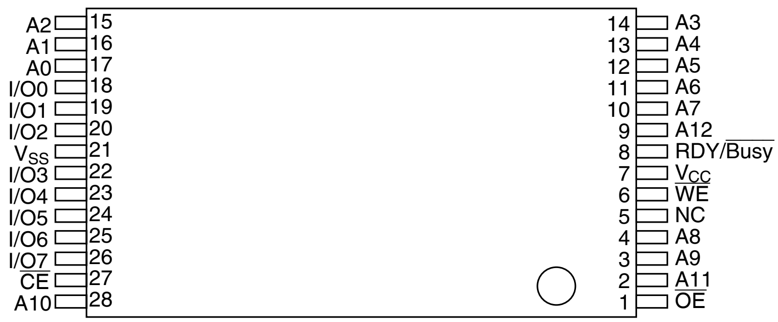
- Single supply: 2.2 to 3.6 V
- Access time: 150 ns (max)
- Power dissipation
  — Active: 10 mW/MHz (typ)
  — Standby: 36 µW (max)
- On-chip latches: address, data, $\overline{\text{CE}}$, $\overline{\text{OE}}$, $\overline{\text{WE}}$
- Automatic byte write: 15 ms (max)
- Automatic page write (64 bytes): 15 ms (max)
- Ready/$\overline{\text{Busy}}$
- $\overline{\text{Data}}$ polling and Toggle bit
- Data protection circuit on power on/off
- Conforms to JEDEC byte-wide standard
- Reliable CMOS with MNOS cell technology
- 10^5 erase/write cycles (in page mode)
- 10 years data retention
- Software data protection
- Industrial versions (Temperature range: – 40 to + 85°C) are also available.
- There are also lead free products.

Ordering Information

Type No.	Access time	Package
HN58S65AT-15	150 ns	28-pin plastic TSOP(TFP-28DB)
HN58S65AT-15E	150 ns	28-pin plastic TSOP(TFP-28DBV) Lead free

Pin Arrangement

HN58S65AT Series

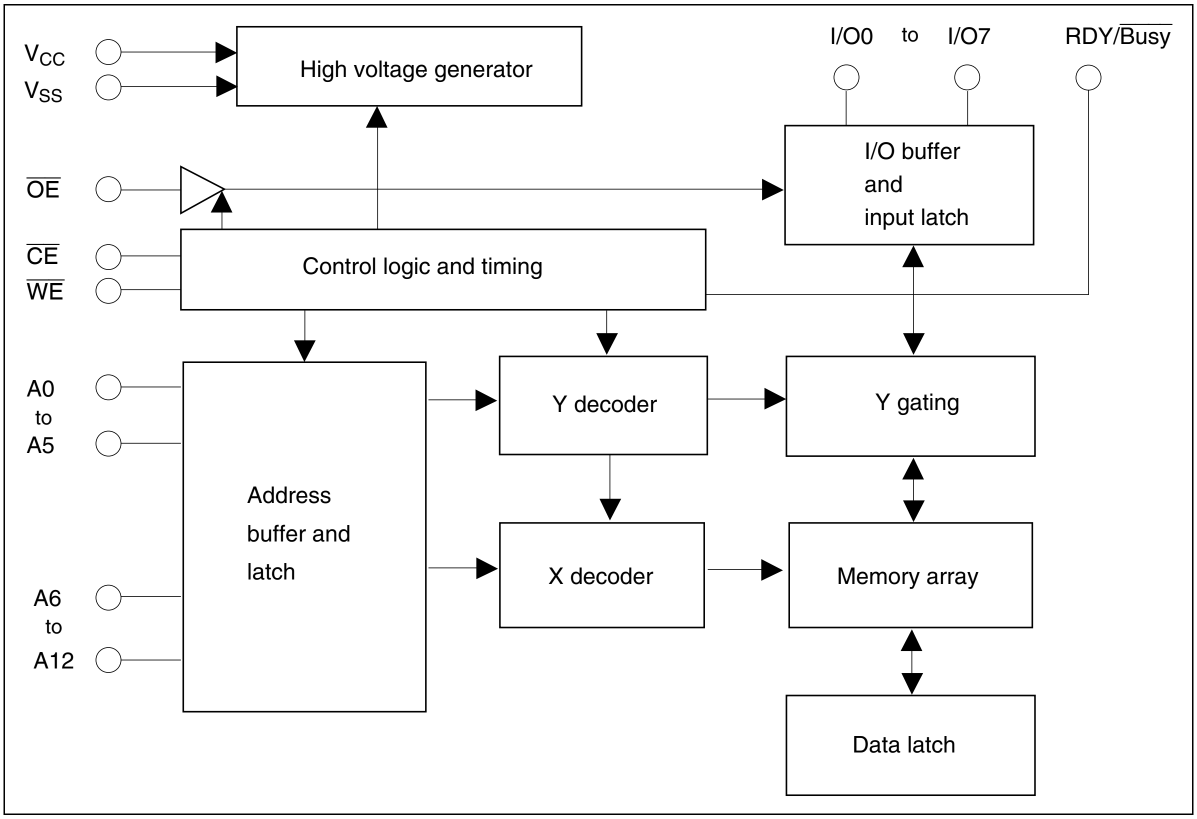


(Top view)

Pin Description

Pin name	Function
A0 to A12	Address input
I/O0 to I/O7	Data input/output
$\overline{OE}$	Output enable
$\overline{CE}$	Chip enable
$\overline{WE}$	Write enable
V_{CC}	Power supply
V_{SS}	Ground
RDY/$\overline{Busy}$	Ready busy
NC	No connection

Block Diagram



Operation Table

Operation	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	RDY/$\overline{Busy}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	High-Z	Dout
Standby	V_{IH}	×*[1]	×	High-Z	High-Z
Write	V_{IL}	V_{IH}	V_{IL}	High-Z to V_{OL}	Din
Deselect	V_{IL}	V_{IH}	V_{IH}	High-Z	High-Z
Write Inhibit	×	×	V_{IH}	—	—
	×	V_{IL}	×	—	—
$\overline{Data}$ Polling	V_{IL}	V_{IL}	V_{IH}	V_{OL}	Dout (I/O7)

Notes: 1. × : Don't care

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Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Power supply voltage relative to V_{SS}	V_{CC}	–0.6 to +7.0	V
Input voltage relative to V_{SS}	Vin	–0.5*[1] to +7.0*[3]	V
Operating temperature range *[2]	Topr	0 to +70	°C
Storage temperature range	Tstg	–55 to +125	°C

Notes: 1. Vin min : –3.0 V for pulse width ≤ 50 ns.
2. Including electrical characteristics and data retention.
3. Should not exceed V_{CC} + 1.0 V.

Recommended DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	2.2	3.0	3.6	V
	V_{SS}	0	0	0	V
Input voltage	V_{IL}	–0.3*[1]	—	0.4	V
	V_{IH}	V_{CC} × 0.7	—	V_{CC} + 0.3*[2]	V
Operating temperature	Topr	0	—	+70	°C

Notes: 1. V_{IL} min: –1.0 V for pulse width ≤ 50 ns.
2. V_{IH} max: V_{CC} + 1.0 V for pulse width ≤ 50 ns.

DC Characteristics (Ta = 0 to + 70°C, V_{CC} = 2.2 to 3.6 V)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	I_{LI}	—	—	2	µA	V_{CC} = 5.5 V, Vin = 5.5 V
Output leakage current	I_{LO}	—	—	2	µA	V_{CC} = 5.5 V, Vout = 5.5/0.4 V
Standby V_{CC} current	I_{CC1}	—	1 to 2	3.5	µA	$\overline{CE}$ = V_{CC}
	I_{CC2}	—	—	500	µA	$\overline{CE}$ = V_{IH}
Operating V_{CC} current	I_{CC3}	—	—	6	mA	Iout = 0 mA, Duty = 100%, Cycle = 1 µs at V_{CC} = 3.6 V
		—	—	12	mA	Iout = 0 mA, Duty = 100%, Cycle = 150 ns at V_{CC} = 3.6 V
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 1.0 mA
Output high voltage	V_{OH}	V_{CC} × 0.8	—	—	V	I_{OH} = –100 µA

Capacitance (Ta = +25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance	Cin*[1]	—	—	6	pF	Vin = 0 V
Output capacitance	Cout*[1]	—	—	12	pF	Vout = 0 V

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to + 70°C, V_{CC} = 2.2 to 3.6 V)

Test Conditions

- Input pulse levels : 0.4 V to 2.4 V (V_{CC} = 2.7 to 3.6 V), 0.4 V to 1.9 V (V_{CC} = 2.2 to 2.7 V)
- Input rise and fall time : ≤ 5 ns
- Input timing reference levels : 0.8, 1.8 V
- Output load : 1TTL Gate +100 pF
- Output reference levels : 1.5 V, 1.5 V (V_{CC} = 2.7 to 3.6 V)
  1.1 V, 1.1 V (V_{CC} = 2.2 to 2.7 V)

Read Cycle

		HN58S65A			
		-15			
Parameter	Symbol	Min	Max	Unit	Test conditions
Address to output delay	t_{ACC}	—	150	ns	$\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$
$\overline{CE}$ to output delay	t_{CE}	—	150	ns	$\overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$
$\overline{OE}$ to output delay	t_{OE}	10	80	ns	$\overline{CE} = V_{IL}$, $\overline{WE} = V_{IH}$
Address to output hold	t_{OH}	0	—	ns	$\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$
$\overline{OE}$ ($\overline{CE}$) high to output float*[1]	t_{DF}	0	80	ns	$\overline{CE} = V_{IL}$, $\overline{WE} = V_{IH}$

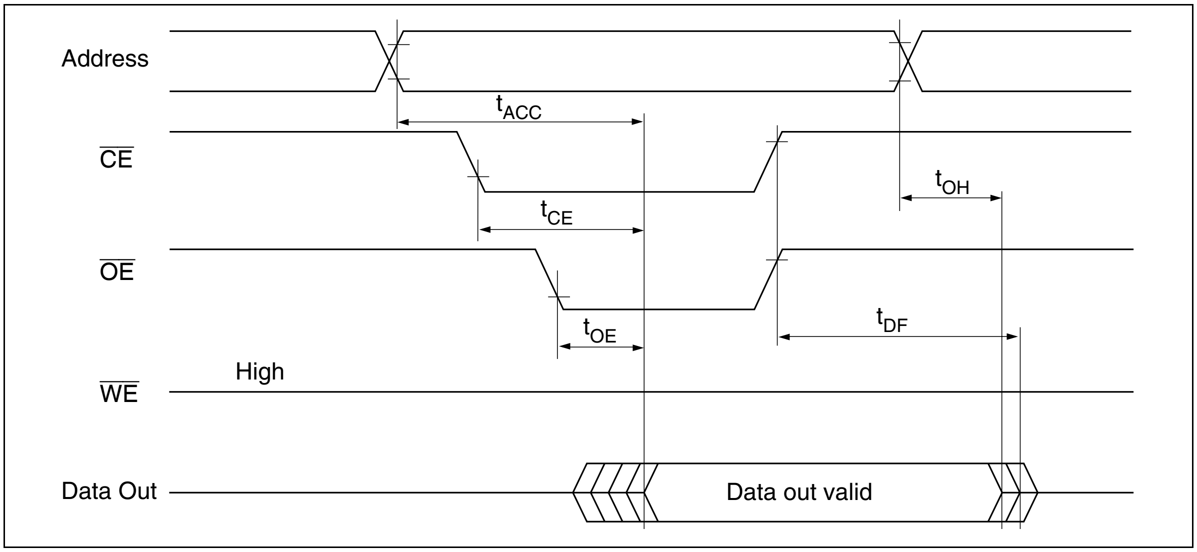
Write Cycle

Parameter	Symbol	Min*[2]	Typ	Max	Unit	Test conditions
Address setup time	t_{AS}	0	—	—	ns	
Address hold time	t_{AH}	150	—	—	ns	
$\overline{CE}$ to write setup time ($\overline{WE}$ controlled)	t_{CS}	0	—	—	ns	
$\overline{CE}$ hold time ($\overline{WE}$ controlled)	t_{CH}	0	—	—	ns	
$\overline{WE}$ to write setup time ($\overline{CE}$ controlled)	t_{WS}	0	—	—	ns	
$\overline{WE}$ hold time ($\overline{CE}$ controlled)	t_{WH}	0	—	—	ns	
$\overline{OE}$ to write setup time	t_{OES}	0	—	—	ns	
$\overline{OE}$ hold time	t_{OEH}	0	—	—	ns	
Data setup time	t_{DS}	150	—	—	ns	
Data hold time	t_{DH}	0	—	—	ns	
$\overline{WE}$ pulse width ($\overline{WE}$ controlled)	t_{WP}	200	—	—	ns	
$\overline{CE}$ pulse width ($\overline{CE}$ controlled)	t_{CW}	200	—	—	ns	
Data latch time	t_{DL}	200	—	—	ns	
Byte load cycle	t_{BLC}	0.4	—	30	µs	
Byte load window	t_{BL}	100	—	—	µs	
Write cycle time	t_{WC}	—	—	15*[3]	ms	
Time to device busy	t_{DB}	120	—	—	ns	
Write start time	t_{DW}	0*[4]	—	—	ns	

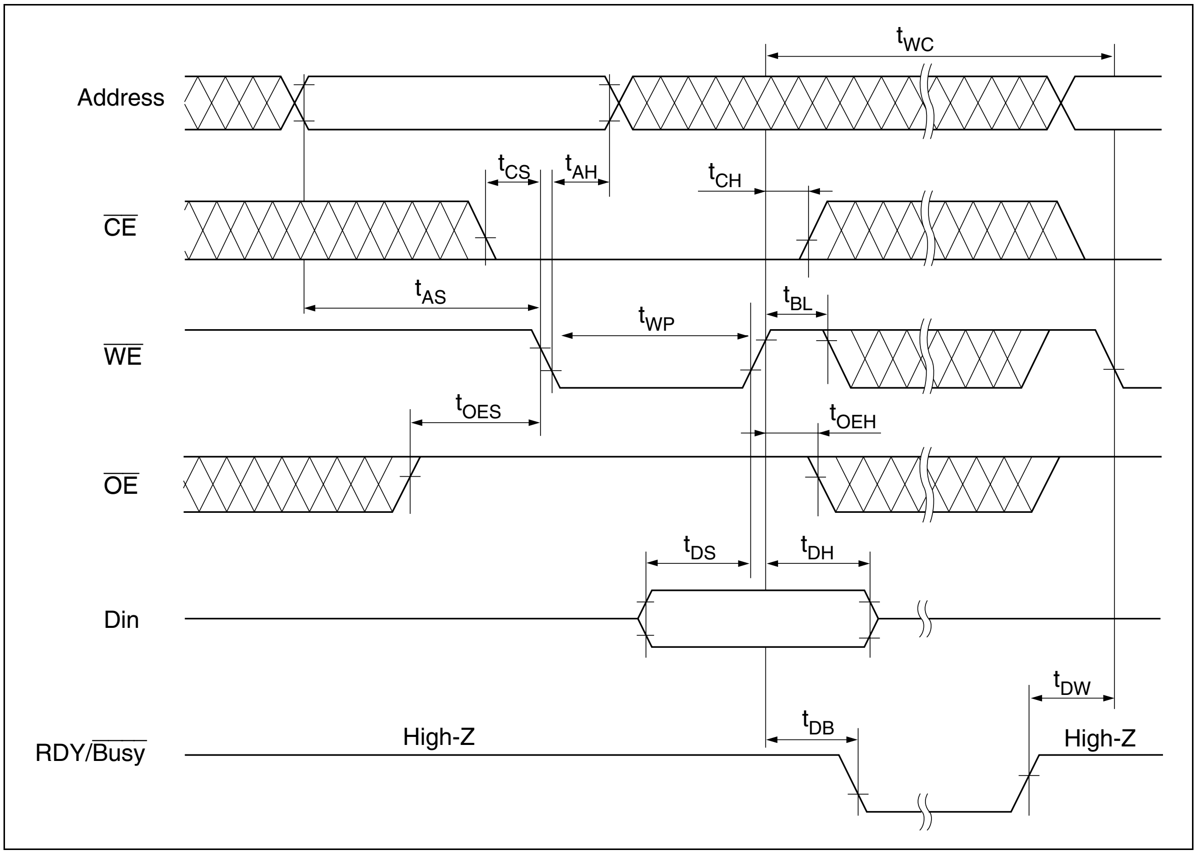
Notes:
1. t_{DF} is defined as the time at which the outputs achieve the open circuit conditions and are no longer driven.
2. Use this device in longer cycle than this value.
3. t_{WC} must be longer than this value unless polling techniques or RDY/$\overline{Busy}$ are used. This device automatically completes the internal write operation within this value.
4. Next read or write operation can be initiated after t_{DW} if polling techniques or RDY/$\overline{Busy}$ are used.
5. A6 through A12 are page addresses and these addresses are latched at the first falling edge of $\overline{WE}$.
6. A6 through A12 are page addresses and these addresses are latched at the first falling edge of $\overline{CE}$.
7. See AC read characteristics.

Timing Waveforms

Read Timing Waveform



Byte Write Timing Waveform(1) ($\overline{WE}$ Controlled)



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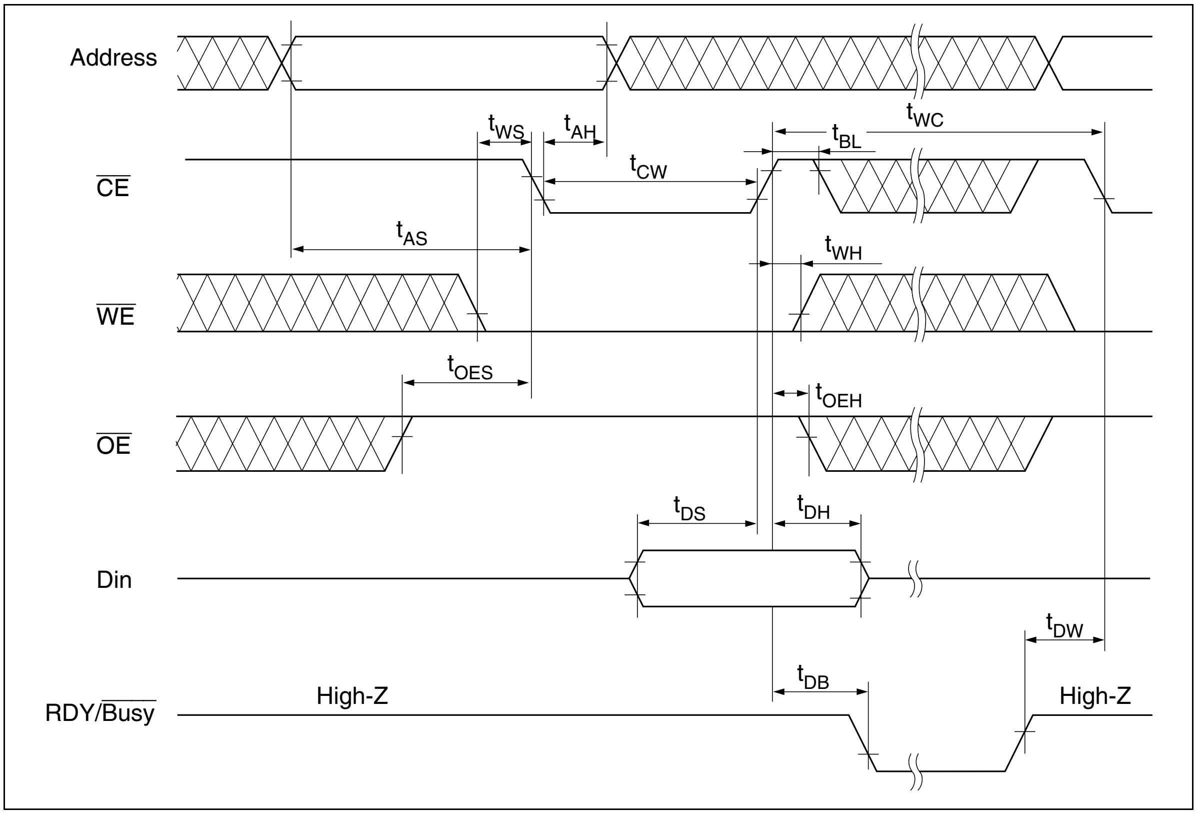
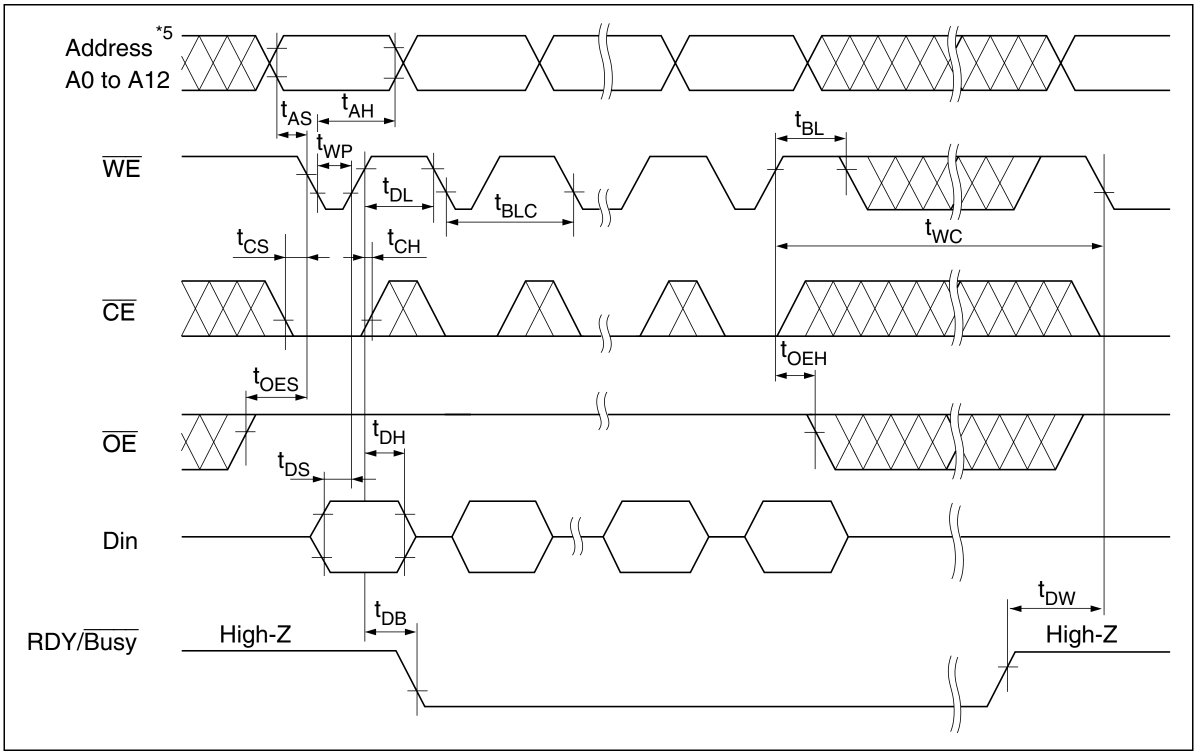
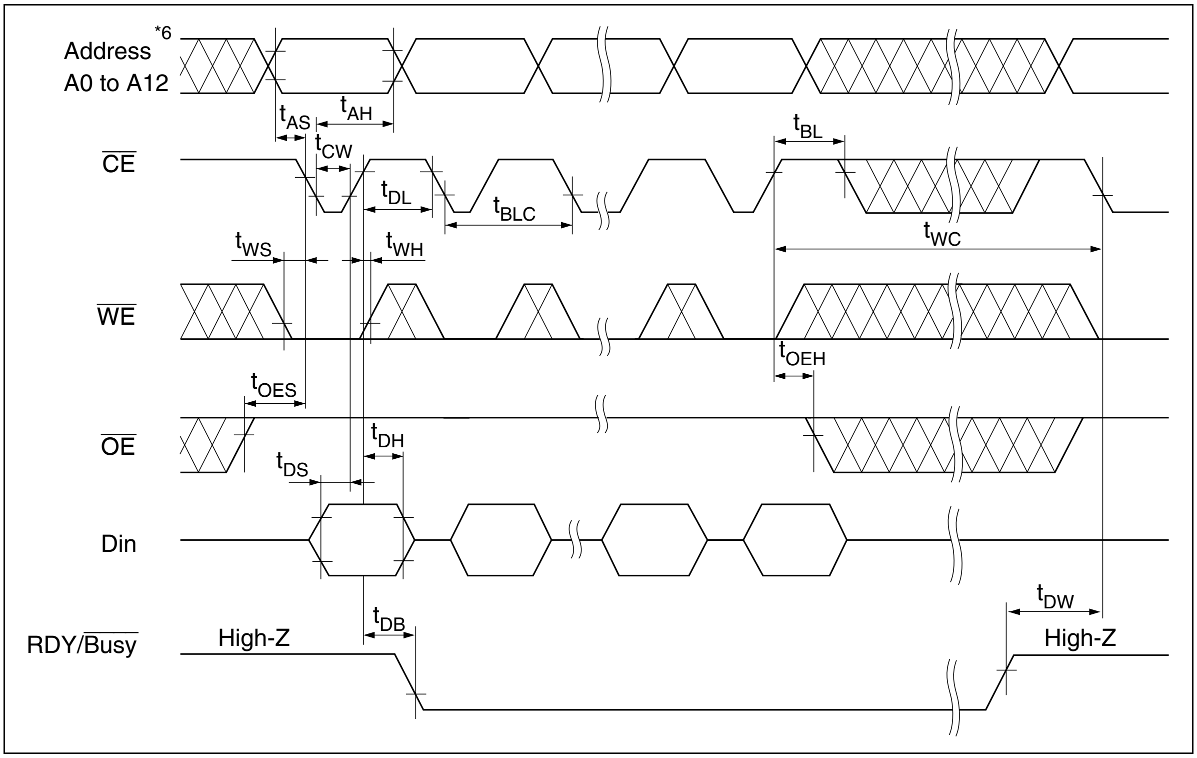
Byte Write Timing Waveform(2) ($\overline{CE}$ Controlled)



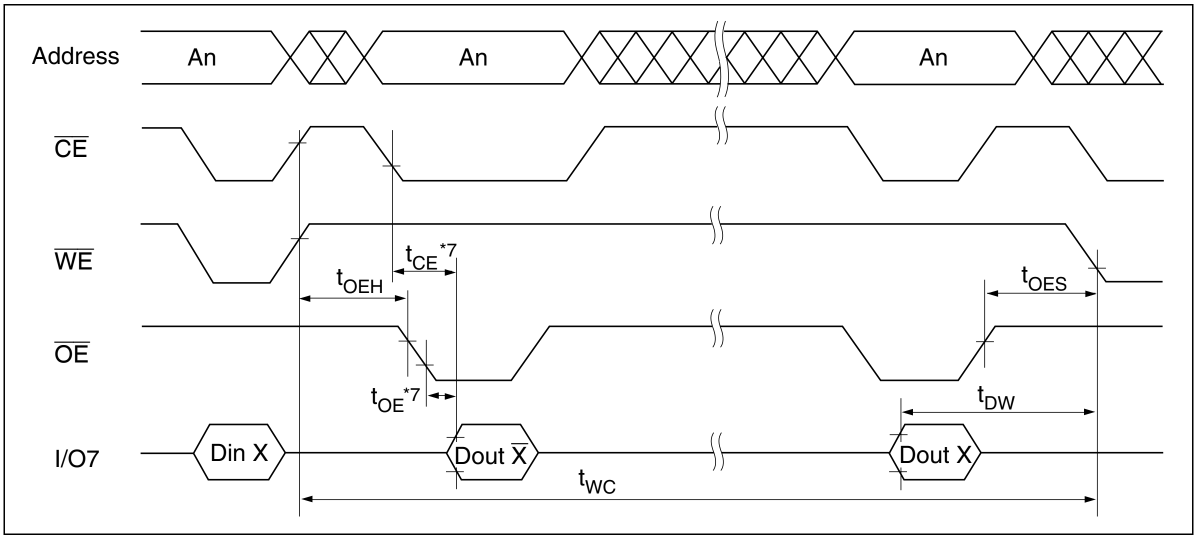
Page Write Timing Waveform(1) ($\overline{WE}$ Controlled)



Page Write Timing Waveform(2) ($\overline{CE}$ Controlled)



$\overline{\text{Data}}$ Polling Timing Waveform

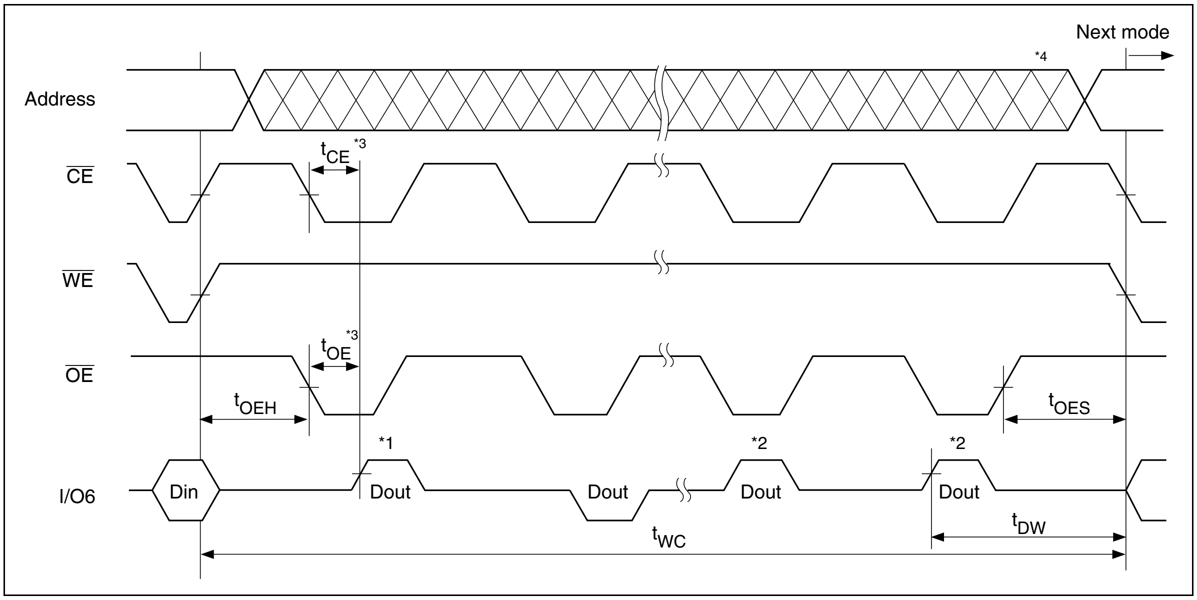


Toggle Bit

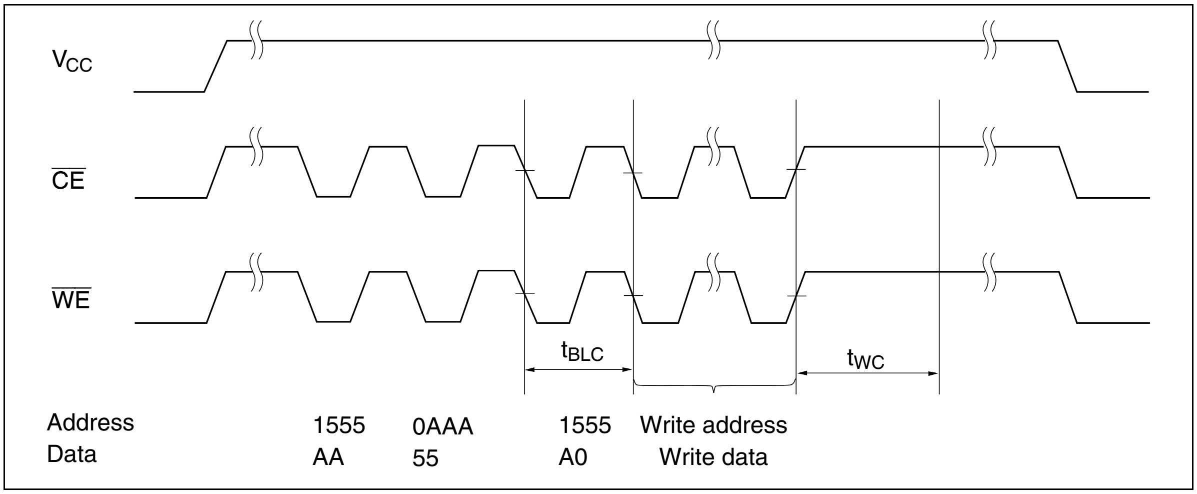
This device provide another function to determine the internal programming cycle. If the EEPROM is set to read mode during the internal programming cycle, I/O6 will charge from “1” to “0” (toggling) for each read. When the internal programming cycle is finished, toggling of I/O6 will stop and the device can be accessible for next read or program.

Toggle Bit Waveform

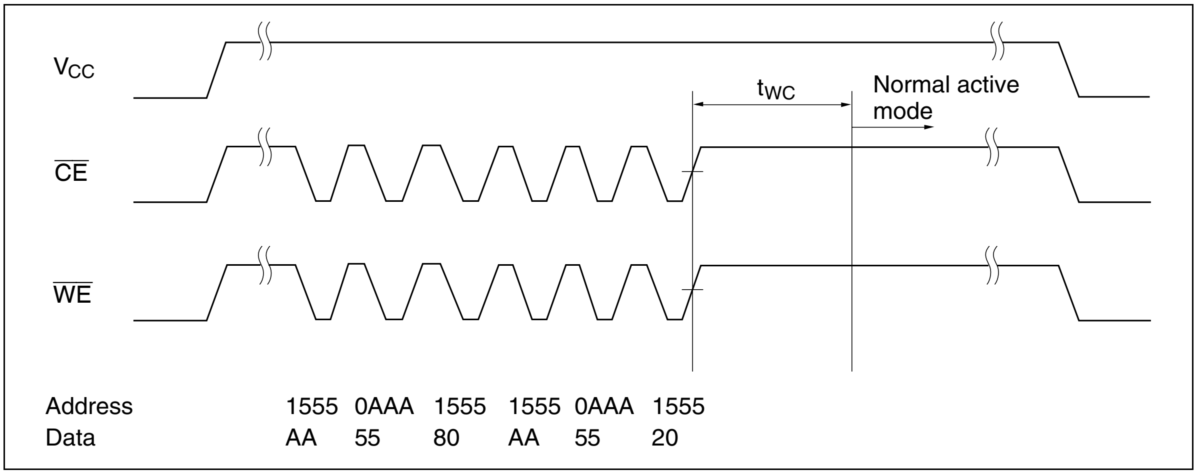
Notes: 1. I/O6 beginning state is “1”.
2. I/O6 ending state will vary.
3. See AC read characteristics.
4. Any address location can be used, but the address must be fixed.



Software Data Protection Timing Waveform(1) (in protection mode)



Software Data Protection Timing Waveform(2) (in non-protection mode)



Functional Description

Automatic Page Write

Page-mode write feature allows 1 to 64 bytes of data to be written into the EEPROM in a single write cycle. Following the initial byte cycle, an additional 1 to 63 bytes can be written in the same manner. Each additional byte load cycle must be started within 30 µs from the preceding falling edge of $\overline{\text{WE}}$ or $\overline{\text{CE}}$. When $\overline{\text{CE}}$ or $\overline{\text{WE}}$ is kept high for 100 µs after data input, the EEPROM enters write mode automatically and the input data are written into the EEPROM.

$\overline{\text{Data}}$ Polling

$\overline{\text{Data}}$ polling indicates the status that the EEPROM is in a write cycle or not. If EEPROM is set to read mode during a write cycle, an inversion of the last byte of data outputs from I/O7 to indicate that the EEPROM is performing a write operation.

RDY/$\overline{\text{Busy}}$ Signal

RDY/$\overline{\text{Busy}}$ signal also allows status of the EEPROM to be determined. The RDY/$\overline{\text{Busy}}$ signal has high impedance except in write cycle and is lowered to V_{OL} after the first write signal. At the end of a write cycle, the RDY/$\overline{\text{Busy}}$ signal changes state to high impedance.

$\overline{\text{WE}}$, $\overline{\text{CE}}$ Pin Operation

During a write cycle, addresses are latched by the falling edge of $\overline{\text{WE}}$ or $\overline{\text{CE}}$, and data is latched by the rising edge of $\overline{\text{WE}}$ or $\overline{\text{CE}}$.

Write/Erase Endurance and Data Retention Time

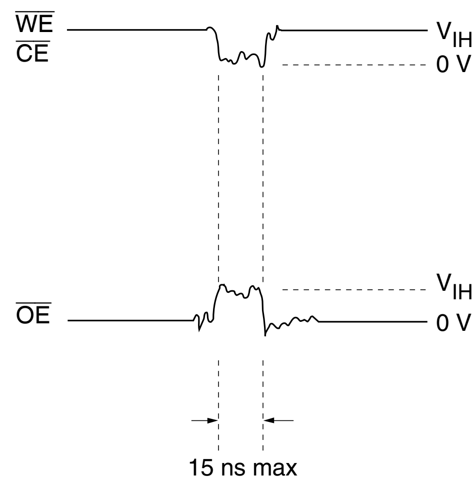
The endurance is 10^5 cycles in case of the page programming and 10^4 cycles in case of the byte programming (1% cumulative failure rate). The data retention time is more than 10 years when a device is page-programmed less than 10^4 cycles.

Data Protection

To prevent this phenomenon, this device has a noise cancellation function that cuts noise if its width is 15 ns or less.

1. Data Protection against Noise on Control Pins ($\overline{CE}$, $\overline{OE}$, $\overline{WE}$) during Operation

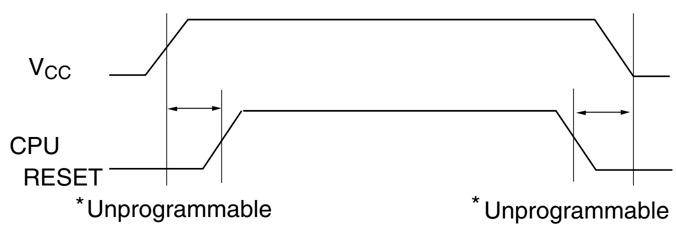
   During readout or standby, noise on the control pins may act as a trigger and turn the EEPROM to programming mode by mistake. Be careful not to allow noise of a width of more than 15 ns on the control pins.



2. Data protection at V_{CC} on/off

   When V_{CC} is turned on or off, noise on the control pins generated by external circuits (CPU, etc) may act as a trigger and turn the EEPROM to program mode by mistake. To prevent this unintentional programming, the EEPROM must be kept in an unprogrammable state while the CPU is in an unstable state.

Note: The EEPROM should be kept in unprogrammable state during V_{CC} on/off by using CPU RESET signal.



2.1 Protection by $\overline{CE}$, $\overline{OE}$, $\overline{WE}$

To realize the unprogrammable state, the input level of control pins must be held as shown in the table below.

$\overline{CE}$	V_{CC}	×	×
$\overline{OE}$	×	V_{SS}	×
$\overline{WE}$	×	×	V_{CC}

×: Don’t care.

V_{CC}: Pull-up to V_{CC} level.

V_{SS}: Pull-down to V_{SS} level.

3. Software data protection

To prevent unintentional programming caused by noise generated by external circuits, this device has the software data protection function. In software data protection mode, 3 bytes of data must be input before write data as follows. And these bytes can switch the non-protection mode to the protection mode. SDP is enabled if onry the 3 byte code is input.

Address	Data
1555	AA
↓	↓
0AAA	55
↓	↓
1555	A0
↓	↓
Write address	Write data } Normal data input

Software data protection mode can be canceled by inputting the following 6 bytes. After that, this device turns to the non-protection mode and can write data normally. But when the data is input in the canceling cycle, the data cannot be written.

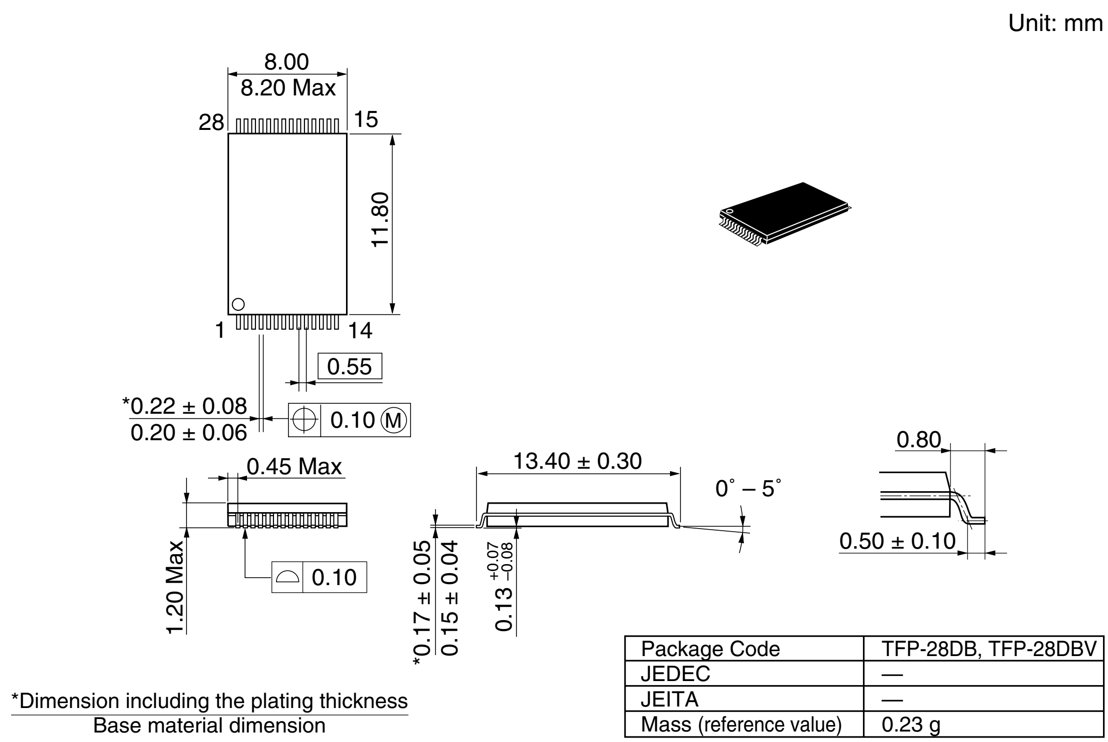
Address	Data
1555	AA
↓	↓
0AAA	55
↓	↓
1555	80
↓	↓
1555	AA
↓	↓
0AAA	55
↓	↓
1555	20

The software data protection is not enabled at the shipment.

Note: There are some differences between Renesas Technology’s and other company’s for enable/disable sequence of software data protection. If there are any questions , please contact with Renesas Technology’s sales offices.

Package Dimensions

HN58S65AT Series (TFP-28DB, TFP-28DBV)



Package Code	TFP-28DB, TFP-28DBV
JEDEC	—
JEITA	—
Mass (reference value)	0.23 g

Revision History HN58S65A Series Data Sheet

Rev.	Date	Contents of Modification	
		Page	Description
0.0	Dec. 5, 1996	—	Initial issue
0.1	Mar. 13, 1997	—	Change of page size: 32 byte to 64 byte
0.2	Aug. 29, 1997	6	Timing Waveform Read Timing Waveform: Correct error Functional Description Data Protection: Addition of description
0.3	Nov.1997		Change of Subtitle
1.00	Feb. 03, 2004	— 2 18	Change format issued by Renesas Technology Corp. Ordering Information Addition of HN58S65AT-15E Package Dimensions TFP-28DB to TFP-28DB, TFP-28DBV

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Colophon 1.0