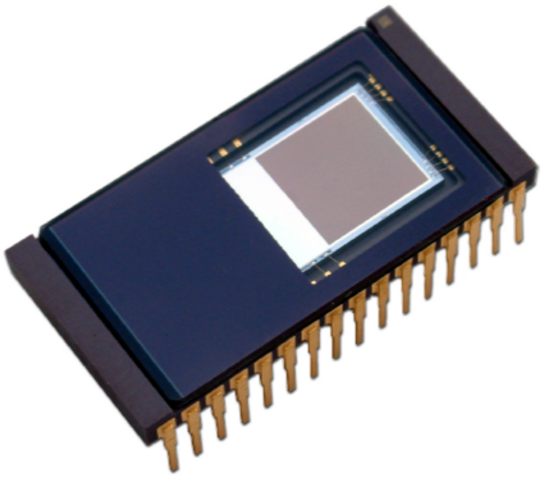
DATA SHEET



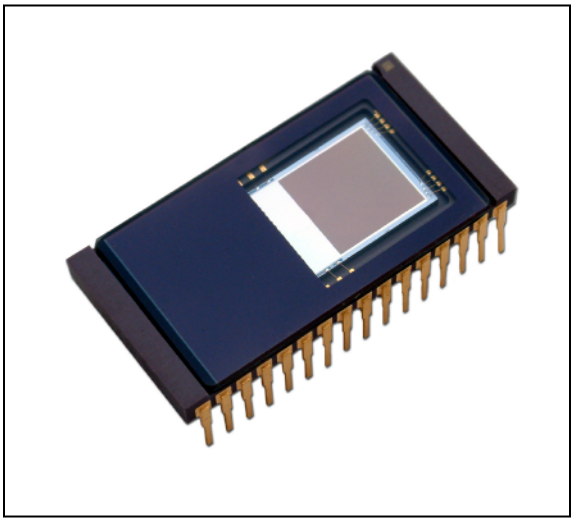
FT18
1M Frame Transfer CCD Image Sensor

Product specification 2006 December 19

DALSA
Professional Imaging

1M Frame Transfer CCD Image Sensor FT18

- **2/3-inch optical format**
- **1M active pixels (1024H x 1024V)**
- **Progressive scan**
- **Excellent antiblooming**
- **Variable electronic shuttering**
- **Square pixel structure**
- **H and V binning**
- **100% optical fill factor**
- **High dynamic range (>60dB)**
- **High sensitivity**
- **Low dark current and fixed pattern noise**
- **Low readout noise**
- **Data rate up to 40 MHz**
- **Frame rate up to 30 Hz**
- **Mirrored readout option**
- **RoHS compliant**



Description

The FT18 is a monochrome progressive-scan frame transfer image sensor offering 1K x 1K pixels at 30 frames per second through a single output buffer. The combination of high speed and a high linear dynamic range (>10 true bits at room temperature without cooling) makes this device the perfect solution for high-end real time medical x-ray, scientific, and industrial applications. A second output can be used for mirrored images. The device structure is shown in Figure 1.

Device structure

Optical size:	7.68 mm (H) x 7.68 mm (V)	
Chip size:	8.9 mm (H) x 17.0 mm (V)	
Pixel size:	7.5 µm x 7.5 µm	
Active pixels:	1024 (H) x 1024 (V)	
Total no. of pixels:	1072 (H) x 1048 (V)	
Optical black pixels:	Left: 20	Right:20
Timing pixels:	Left: 4	Right:4
Dummy register pixels:	Left: 7	Right: 7
Contour lines:	Bottom: 1	Top: 4
Optical black lines:	Bottom: 11	Top: 8

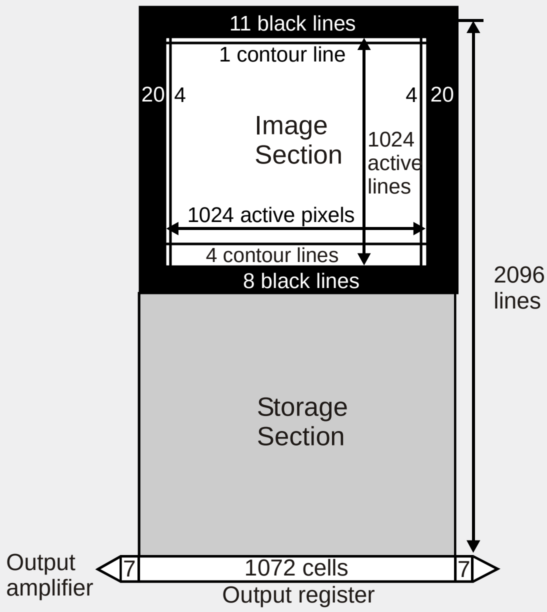


Figure 1 - Device structure

Architecture of the FT18

The FT18 consists of a shielded storage section and an open image section. Both sections have the same structure with identical cells and properties. The only difference between the two sections is the optical light shield.

The optical centres of all pixels in the image section form a square grid. The charge is generated and integrated in this section. The image section is controlled by four image clocks (A1 to A4). After integration, the image charge is completely shifted to the storage section. The integration time is electronically controlled by charge reset (CR).

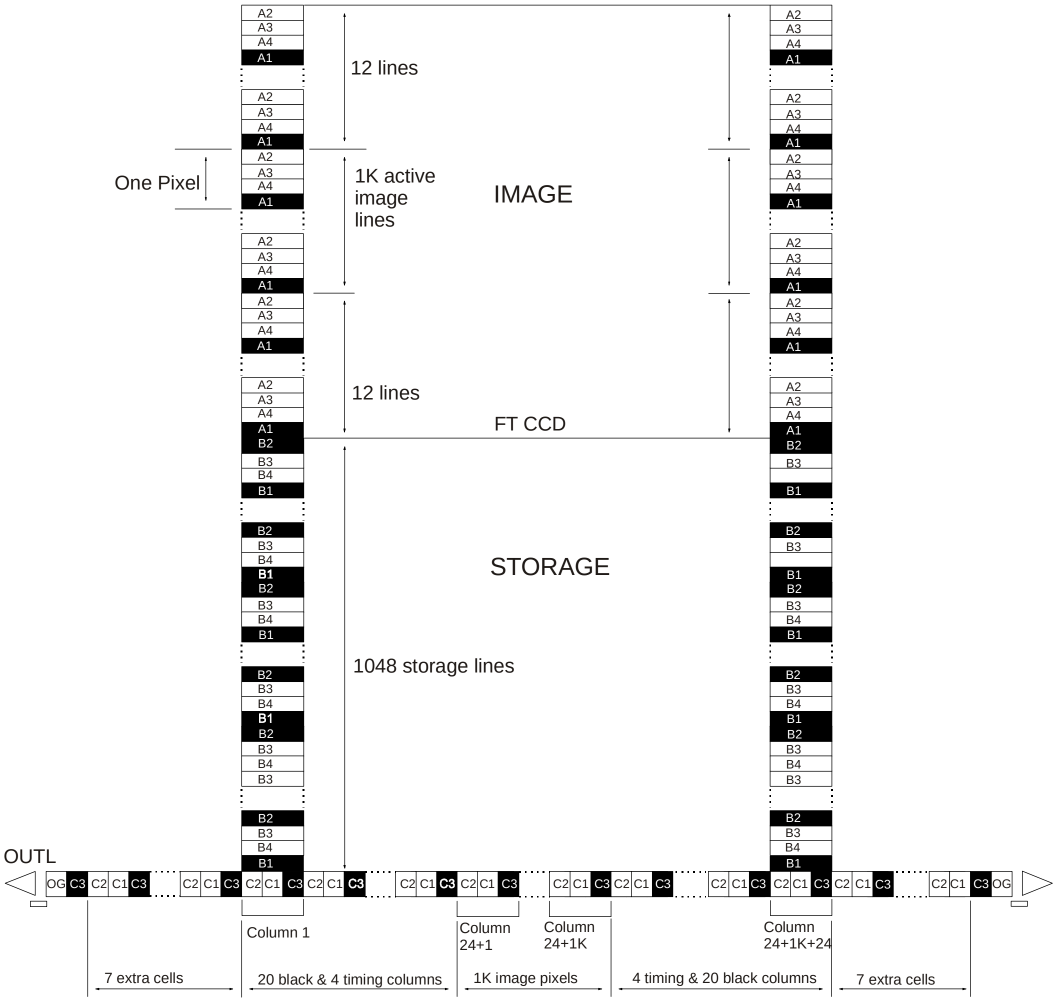
The storage section is controlled by four storage clocks (B1 to B4). An output register is located below the storage section for readout. The output register has buffers at both ends. This allows either normal or mirrored readout.

Transport of the pixels in the output register is controlled by three register clock phases (C1 to C3). The register can be used for vertical binning. Horizontal binning can be achieved by summing pixel charges under the floating diffusion. More information can be found in the application note. Figure 2 shows the detailed internal structure.

IMAGE SECTION	
Image diagonal	10.9 mm
Aspect ratio	1:1
Active image width x height	7.680 x 7.680 mm^2
Total width x height	8.040 x 7.860 mm^2
Pixel width x height	7.5 x 7.5 μm^2
Geometric fill factor	100%
Image clock pins	A1, A2, A3, A4
Capacity of each clock phase	<3.75nF per pin
Number of active lines	1024
Number of contour lines	4 (top) + 1 (bottom)
Number of black lines	8 (top) + 11 (bottom)
Total number of lines	1048
Number of active pixels per line	1024
Number of overscan (timing)pixels per line	8 (2x4)
Number of black reference pixels per line	40 (2x20)
Total number of pixels per line	1072

STORAGE SECTION	
Storage width x height	8.040 x 7.860 mm^2
Cell width x height	7.5 x 7.5 μm^2
Storage clock phases	B1, B2, B3, B4
Capacity of each B phase	<4.1nF per pin
Number of cells per line x number of lines	1072 x 1048

OUTPUT REGISTER	
Output buffers (three-stage source follower)	2
Number of registers	1 (bidirectional below storage)
Number of register cells below storage	1072
Number of extra cells to output	2 x 7
Output register horizontal transport clock pins	3 (C1..C3)
Capacitance of each C-clock phase	<85pF per pin
Overlap capacity between neighboring C-clocks	<35pF
Reset Gate clock phases	2 pins (RGL, RGR)
Capacity of each RG	<15pF



A1, A2, A3, A4: clocks of image section
B1, B2, B3, B4: clocks of storage section
C1, C2, C3: clocks of horizontal register
OG: output gate

Figure 2 - Detailed internal structure

Specifications

ABSOLUTE MAXIMUM RATINGS	MIN	MAX	UNIT
GENERAL:			
storage temperature	-55	+80	ºC
ambient temperature during operation	-40	+60	ºC
voltage between any two gates	-20	+20	V
DC current through any clock (absolute value)	-0.2	+0.2	µA
OUT current (no short circuit protection)	0	+6	mA
VOLTAGES IN RELATION TO VNS:			
VPS, SFS	-30	+0.5	V
SFD	-8	+8	V
RD	-15	+0.5	V
All other pins	-32	+0.5	V
VOLTAGES IN RELATION TO VPS:			
VNS	-0.5	+30	V
SFD, RD	+0	+30	V
SFS	-8	+8	V
All other pins	-20	+20	V

DC CONDITIONS[1]		MIN [V]	TYPICAL [V]	MAX [V]	UNIT
VNS[2]	N substrate	16	adjusted	24	V
VPS	P well	2	4	6	V
SFD	Source Follower Drain	18	20	22	V
SFS	Source Follower Source	-	0	-	V
VCS	Current Source Gate	-2	0	3	V
OG	Output Gate	3	5.4	8	V
RD	Reset Drain	12	13	15	V

AC CLOCK LEVEL CONDITIONS[1]	MIN	TYPICAL	MAX	UNIT
IMAGE CLOCKS (duty cycle = 5/8)				
A-clock swing	9.5	10	-	V
A-clock low level	-	0	-	V
Charge Reset (CR) level on A-clocks[3]	-	-5	-	V
Charge Pump (CP) level on A-clocks	-	0	-	V
STORAGE CLOCKS (duty cycle = 5/8)				
B-clock swing	9.5	10	-	V
B-clock low level	-	0	-	V
OUTPUT REGISTER CLOCKS (duty cycle = 1/2)				
C-clock swing	-	5	-	V
C-clock low level	-	3	-	V
OTHER CLOCKS:				
Reset Gate (RG) swing	-	10	12	V
Reset Gate (RG) low level	-	1	-	V

[1] All voltages in relation to SFS.
[2] To set the VNS voltage for optimal Vertical Antiblooming (VAB), it should be adjustable between minimum and maximum values.
[3] Guaranteed charge requires the CR voltage to last at least 1.2µs.

Timing diagrams (for default operation)

AC Characteristics	Min.	Typical	Max.	Unit
Horizontal frequency (1/Tp))	-	36	40	MHz
Vertical frequency	-	750	833	kHz

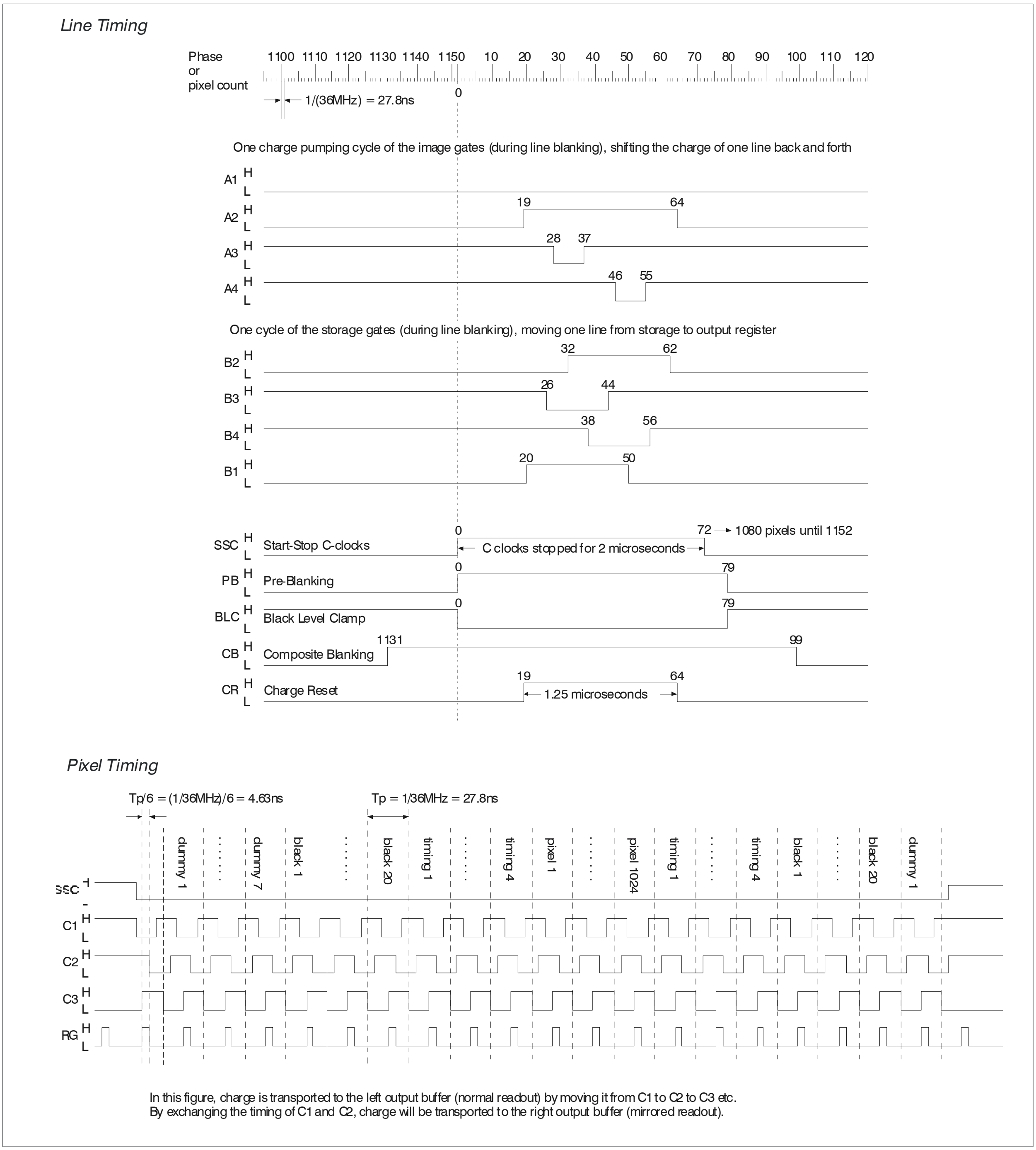


Figure 3 – Line and pixel timing diagrams

1M Frame Transfer CCD Image Sensor FT18

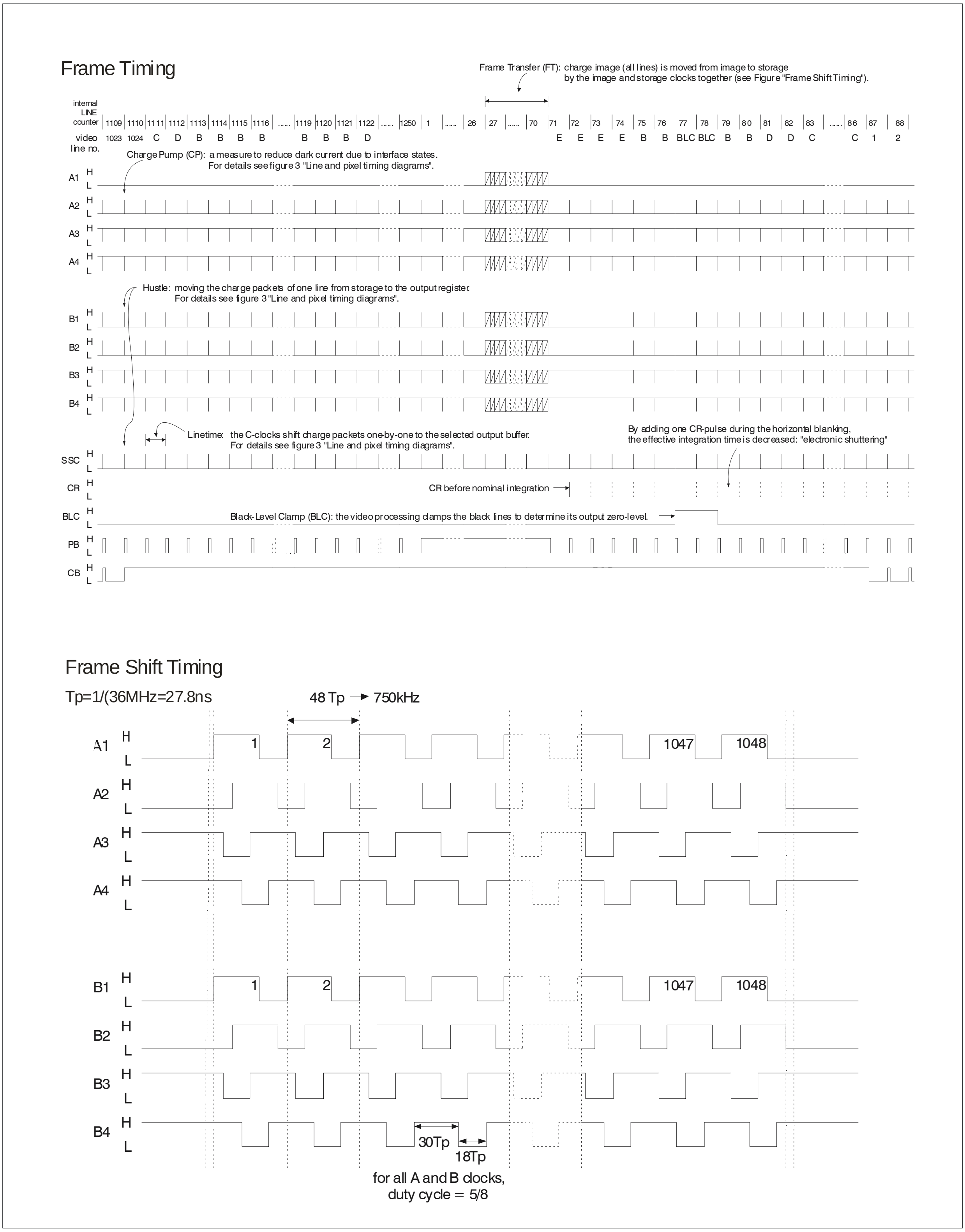


Figure 4: Frame Timing Diagrams

Performance

The performance of the FT18 is described using modes of operation with 25fps or 30fps respectively. Measurements for the FT18 are done under the following circumstances (values in brackets apply to the 30fps mode):

- VNS is adjusted as low as possible while maintaining proper Vertical Antiblooming
- Integration takes place under 2 gates with 10V clock swing during 40ms (33.33ms)
- The vertical transport or frame shift frequency equals 750kHz (714kHz)
- The horizontal transport or readout frequency equals 36MHz (40MHz)
- The RMS readout noise of the output buffers and the FPN are measured in the bandwidth 0.1-18MHz (0.1-20MHz)
- The performance in dark is given at a temperature of 318K/45°C. Note that the dark current decreases by a factor of two for every decrease of temperature of approximately 10°C.

LINEAR / SATURATION	MIN	TYPICAL	MAX	UNIT
Overexposure over entire area while maintaining good VAB	300	-	-	lux
Vertical resolution (MTF) @ 67 lp/mm	25	-	-	%
Quantum efficiency @ 450 nm	10	11	-	%
Quantum efficiency @ 520 nm	21	22	-	%
Quantum efficiency @ 600 nm	18	19	-	%
Quantum efficiency @ 800 (near IR)	5	-	-	%
Image lag	-	0	-	%
White Shading[1]	-	-	2.5	%
Random Non-Uniformity (RNU)[2]	-	1.0	1.4	%
Full-well capacity Floating Diffusion (FD)	120	-	-	kel.
Full-well capacity saturation level (Q_{max})[3] image	40	45	-	kel.
Full-well capacity saturation level (Q_{max}) storage	45	-	-	kel.
Full-well capacity saturation level (Q_{max}) output register[4]	90	-	-	kel.
25 FRAMES / SEC MODE ONLY				
Sensitivity @ 3200K without IR cut-off filter	5.6	5.8	-	kel/lux
Smear without shutter[5]	-	-	0.39	%
Dynamic range	60	63.8	-	dB
RMS readout noise	-	29	38	el
30 FRAMES / SEC MODE ONLY				
Sensitivity @ 3200K without IR cut-off filter	4.6	4.8	-	kel/lux
Smear without shutter[5]	-	-	0.40	%
Dynamic range	60	63.5	-	dB
RMS readout noise	-	30	40	el

[1]White Shading is defined as the ratio of one-σ value of an 8x8 pixel blurred image (low-pass) to the mean signal value.
[2]Random Non Uniformity is defined as the ratio of one-σ value of the high-pass image to the mean signal value at nominal light.
[3]Q_{max} is determined from the low-pass filtered image.
[4] Q_{max} of the output register may be increased up to 200kel. In this case, the charge packets of the pixels get mixed in the output register during horizontal transport. This may reduce the number of times that the output register needs to be read out if lines are read out solely to be dumped.
[5]The smear condition is: overexposure with a spot with a height of 10% of the image height (approx. 100 lines).

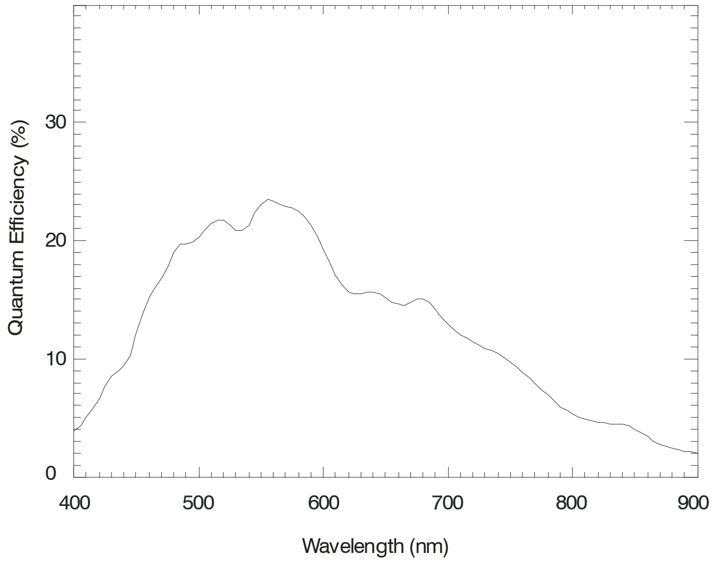


Figure 5 – Quantum efficiency versus wavelength

OUTPUT BUFFERS	MIN	TYPICAL	MAX	UNIT
Conversion factor	8.5	10	11.5	µV/el.
Supply current	-	4	-	mA
Bandwidth	-	110	-	MHz
Output impedance buffer (R_{load}=3.3kΩ, C_{load}=2pF)	-	400	-	Ω

DARK CONDITION	MIN	TYPICAL	MAX	UNIT
Dark current	-	-	240	pA/cm^2
Black level offset[1]	-	-	25	el
Dark condition at 25 frames/sec:				
Average dark signal	-	56	67	el
Shot noise on the dark current	-	-	10	el
Horizontal shading	-	-	25	el
Vertical shading	-	-	66	el
Fixed Pattern Noise[2] in dark (FPN)	-	-	19	el
Dark condition at 30 frames/sec:				
Average dark signal	-	47	56	el
Shot noise on the dark current	-	-	10	el
Horizontal shading	-	-	25	el
Vertical shading	-	-	56	el
Fixed Pattern Noise[2] in dark (FPN)	-	-	19	el

[1]Black level offset is defined as the difference in dark signal of a black reference and an active image line.
[2]FPN is the one-σ value of the high-pass image.

Application information

Current handling

One of the purposes of VPS is to drain the holes that are generated during exposure of the sensor to light. Free electrons are either transported to the VRD connection and, if excessive (from overexposure), free electrons are drained to VNS. No current should flow into any VPS connection of the sensor. During high overexposure a total current of 10 to 15mA through all VPS connections together may be expected. The PNP emitter follower in the circuit diagram (figure 6) serves these current requirements.

VNS drains superfluous electrons as a result of overexposure. In other words, it only sinks current. During high overexposure a total current of 10 to 15mA through all VNS connections together may be expected. The NPN emitter follower in the circuit diagram meets these current requirements.

Decoupling of DC voltages

All DC voltages should be decoupled with a100nF decoupling capacitor. This capacitor must be mounted as close as possible to the sensor pin. Further noise reduction (by bandwidth limiting) is achieved by the resistors in the connections between the sensor and its voltage supplies. The electrons that build up the charge packets that will reach the floating diffusions only add up to a small current, which will flow through VRD. Therefore, a large series resistor in the VRD connection may be used.

Outputs

To limit the on-chip power dissipation, the output buffers are designed with open source outputs. Outputs to be used should therefore be loaded with a current source or more simply with a resistance to GND. In order to prevent the output (which typically has an output impedance of about 400Ω) from bandwidth limitation as a result of capacitive loading, load the output with an emitter follower built from a high-frequency transistor. Mount the base of this transistor as close as possible to the sensor and keep the connection between the emitter and the next stage short. The CCD output buffer can easily be destroyed by ESD. By using this emitter follower, this danger is suppressed; do NOT reintroduce this danger by measuring directly on the output pin of the sensor with an oscilloscope probe. Instead, measure on the output of the emitter follower. Slew rate limitation is avoided by avoiding a too-small quiescent current in the emitter follower; about 10mA should do the job. The collector of the emitter follower should be uncoupled properly to suppress the Miller effect from the base-collector capacitance.

A CCD output load resistor of 3.3kΩ typically results in a bandwidth of 110MHz. The bandwidth can be enlarged to about 130MHz by using a resistor of 2.2kΩ instead, which, however, also enlarges the on-chip power dissipation.

Device protection

The output buffers of the FT18 are likely to be damaged if VPS rises above SFD or RD at any time. This danger is most realistic during power-on or power-off of the camera. The RD voltage should always be lower than the SFD voltage.

Never exceed the maximum output current. This may damage the device permanently. The maximum output current should be limited to 6mA.

Be especially aware that the output buffers of these image sensors are very sensitive to ESD damage.

Because of the fact that our CCDs are built on an n-type substrate, we are dealing with some parasitic npn transistors. To avoid activation of these transistors during switch-on and switch-off of the camera, we recommend the application diagram of figure 6.

Device Handling

An image sensor is a MOS device which can be destroyed by electro-static discharge (ESD). Therefore, the device should be handled with care.

Always store the device with short-circuiting clamps or on conductive foam. Always switch off all electric signals when inserting or removing the sensor into or from a camera (the ESD protection in the CCD image sensor process is less effective than the ESD protection of standard CMOS circuits).

Being a high quality optical device, it is important that the cover glass remain undamaged. When handling the sensor, use fingercots.

When cleaning the coverglass we strongly recommend using ethanol. Use of other liquids is strongly discouraged:

- if the cleaning liquid evaporates too quickly, rubbing is likely to cause ESD damage.
- the cover glass and its coating can be damaged by other liquids.

Rub the window carefully and slowly.

Dry rubbing of the window may cause electro-static charges or scratches which can destroy the device.

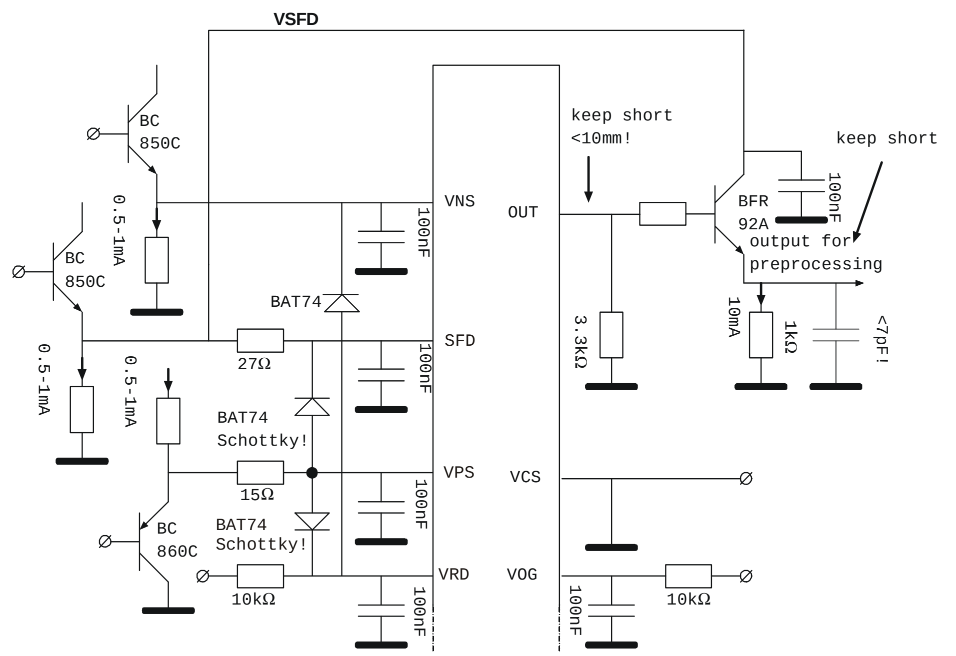


Figure 6 – Application diagram to protect the FT18

Pin configuration

The FT18 is mounted in a ceramic DIL 32-pin package.
The position of pin 1 is marked with a white dot on top of the package.

Pinning		
Symbol	**Name**	**Pin #**
VNS	N substrate	12
VNS	N substrate	21
VPS	P well	5
VPS	P well	28
SFDL	Source Follower Drain Left	9
SFDR	Source Follower Drain Right	24
SFSL	Source Follower Source Left	8
SFSR	Source Follower Source Right	25
VCSL	Current Source Gate Left	7
VCSR	Current Source Gate Right	26
OGL	Output Gate Left	6
OGR	Output Gate Right	27
RDL	Reset Drain Left	11
RDR	Reset Drain Right	22
A1	Image Clock (Phase 1)	3
A2	Image Clock (Phase 2)	4
A3	Image Clock (Phase 3)	30
A4	Image Clock (Phase 4)	29
B1	Storage Clock (Phase 1)	1
B2	Storage Clock (Phase 2)	2
B3	Storage Clock (Phase 3)	32
B4	Storage Clock (Phase 4)	31
C1	Register Clock (Phase 1)	14
C1	Register Clock (Phase 1)	19
C2	Register Clock (Phase 2)	15
C2	Register Clock (Phase 2)	18
C3	Register Clock (Phase 3)	16
C3	Register Clock (Phase 3)	17
RGL	Reset Gate Left	13
RGR	Reset Gate Right	20
OUTL	Output Left	10
OUTR	Output Right	23

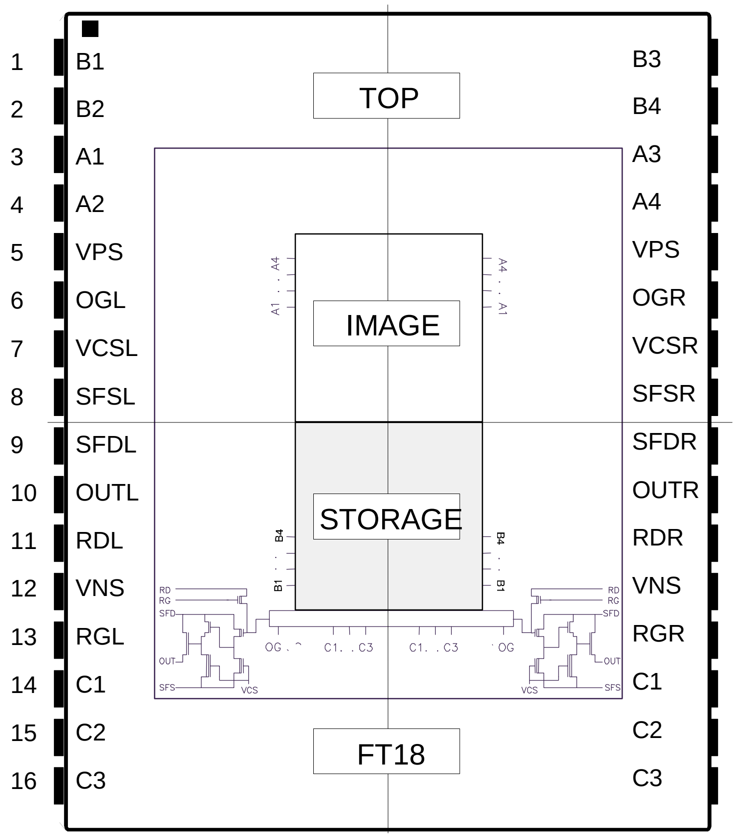
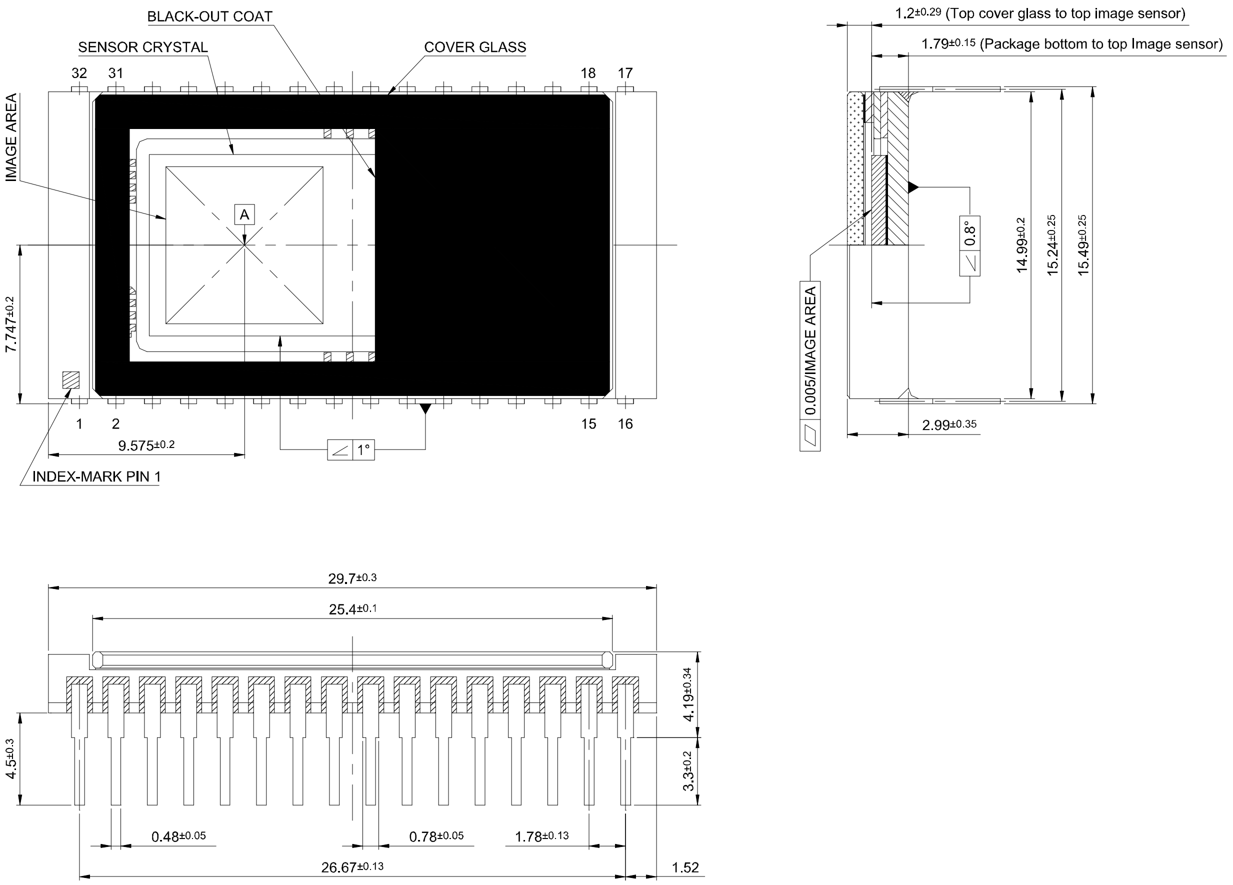


Figure 7 – FT18 pin configuration (top view)

Package information



A is the center of the image area
Position of A:
9.575 ± 0.2 to left edge of package
7.747 ± 0.2 to lower edge of package
1.79 ± 0.15 to bottom of package

Angle of rotation: less than ± 1°
Sensor flatness: < 5 µm (P-V)

Cover glass: Hoya CG1
Thickness of cover glass: 0.8 ± 0.05
Refractive index: nd = 1.53
Single sided AR coating inside, < 1 % reflection (430-660 nm)
Hermetically sealed package

All drawing units are in mm.

Figure 8 – Mechanical drawing of the FT18 package

Order codes

The sensor can be ordered using the following codes:

FT18 sensors		
Description	**Quality Grade**	**Order Code**
FT18/TG	Test Grade	9922 157 32031
FT18/IG	Industrial Grade	9922 157 32021
FT18/HG	High Grade	9922 157 32011
FT18/SG	Selected Grade	9922 157 32001

Defect Specifications

The CCD image sensor can be ordered in a specific quality grade. The grading is defined with the maximum amount of pixel defects, column defects, row defects and cluster defects, in both illuminated and non-illuminated conditions. For detailed grading information, please contact your local DALSA representative.

For More Information

For more detailed information on this and other products, contact your local rep or visit our Web site at http://www.dalsa.com/pi/products.

DALSA Professional Imaging
Sales Department
High Tech Campus 12a
5656 AE Eindhoven
The Netherlands
Tel: +31 40 2745110
Fax: +31 40 2743650
www.dalsa.com/pi
sales.sensors@dalsa.com

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