Ultra-Low-Noise, High PSRR, Low-Dropout, 300mA Linear Regulator

Features

- **Wide Operating Voltage: 2.5~6V**
- **Low Dropout Voltage: 290mV@3V/300mA**
- **Fixed Output Voltages: 1.2~3.6V with Step 100mV, and 2.85V**
- **Guaranteed 300mA Output Current**
- **High PSRR: 70dB**
- **Current-Limit Protection**
- **Controlled Short Circuit Current: 50mA**
- **Over-Temperature Protection**
- **Stable with 1㎌F Capacitor for Any Load**
- **Excellent Load/Line Transient**
- **SOT-23-5, SC-70-5, VTDFN1.2x1.6-4, and TDFN1.6x1.6-6 Packages**
- **Lead Free and Green Devices Available (RoHS Compliant)**

Applications

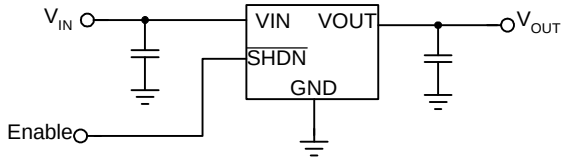
- **Cellular Phones**
- **Portable and Battery-Powered Equipments**
- **Laptops, Palmtops, Notebook Computers**
- **Wireless LANs**
- **Portable Information Appliances**
- **GPSes**

General Description

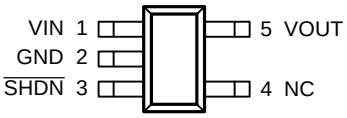
The APL5320 is a P-channel low dropout linear regulator which needs only one input voltage from 2.5 to 6V, and delivers current up to 300mA to set output voltage. It also can work with low ESR ceramic capacitors and is ideal for using in the battery-powered applications such as notebook computers and cellular phones. Typical dropout voltage is only 290mV at 300mA loading.

The APL5320 provides several versions of fixed output voltages ranging from 1.2 to 3.6V with step 100mV and 2.85V. Current limit with current foldback and thermal shutdown functions protects the device against current overloads and over temperature. The APL5320 is available in SOT-23-5, SC-70-5, VTDFN1.2x1.6-4, and TDFN 1.6x1.6-6 packages.

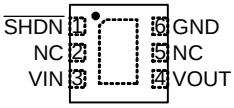
Simplified Application Circuit



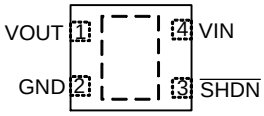
Pin Configuration



SOT23-5/SC-70-5
(Top View)



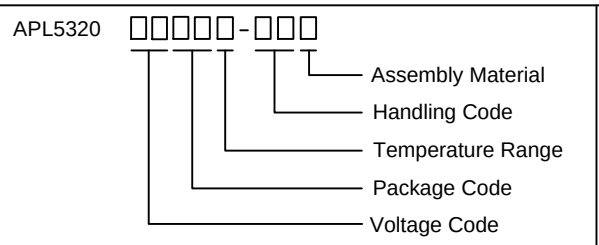
TDFN1.6x1.6-6
(Top View)



VTDFN1.2x1.6-4
(Top View)

= Exposed Pad (connected to ground plane for better heat dissipation)

Ordering and Marking Information



Package Code
B : SOT-23-5 S5 : SC-70-5 QB : TDFN1.6x1.6-6
QF: VTDFN1.2x1.6-4
Operating Ambient Temperature Range
I : -40 to 85 °C
Handling Code
TR : Tape & Reel
Voltage Code
12 : 1.2V 3.6 : 3.6V
Assembly Material
G : Halogen and Lead Free Device

Note : ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant)and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

SOT-23-5

Product Name	Marking	Product Name	Marking	Product Name	Marking	Product Name	Marking
APL5320-12B	205X	APL5320-13B	207X	APL5320-14B	208X	APL5320-15B	209X
APL5320-16B	20AX	APL5320-17B	20BX	APL5320-18B	20CX	APL5320-19B	20DX
APL5320-20B	20EX	APL5320-21B	20FX	APL5320-22B	20GX	APL5320-23B	20HX
APL5320-24B	20IX	APL5320-25B	20JX	APL5320-26B	20KX	APL5320-27B	20LX
APL5320-28B	20MX	APL5320-29B	20NX	APL5320-30B	20OX	APL5320-31B	20PX
APL5320-32B	20QX	APL5320-33B	20RX	APL5320-34B	20SX	APL5320-35B	20TX
APL5320-36B	20gX	APL5320-285B	20dX				

Note: X - Code.

SC-70-5

Product Name	Marking	Product Name	Marking	Product Name	Marking	Product Name	Marking
APL5320-12S5	205	AP5320-13S5	207	APL5320-14S5	208	APL5320-15S5	209
APL5320-16S5	20A	APL5320-17S5	20B	APL5320-18S5	20C	APL5320-19S5	20D
APL5320-20S5	20E	APL5320-21S5	20F	APL5320-22S5	20G	APL5320-23S5	20H
APL5320-24S5	20I	APL5320-25S5	20J	APL5320-26S5	20K	APL5320-27S5	20L
APL5320-28S5	20M	APL5320-29S5	20N	APL5320-30S5	20O	APL5320-31S5	20P
APL5320-32S5	20Q	APL5320-33S5	20R	APL5320-34S5	20S	APL5320-35S5	20T
APL5320-36S5	20g	APL5320-285S5	20d				

TDFN1.6x1.6-6

Product Name	Marking	Product Name	Marking	Product Name	Marking	Product Name	Marking
APL5320-12QB	205 X	APL5320-13QB	207 X	APL5320-14QB	208 X	APL5320-15QB	209 X
APL5320-16QB	20A X	APL5320-17QB	20B X	APL5320-18QB	20C X	APL5320-19QB	20D X
APL5320-20QB	20E X	APL5320-21QB	20F X	APL5320-22QB	20G X	APL5320-23QB	20H X
APL5320-24QB	20I X	APL5320-25QB	20J X	APL5320-26QB	20K X	APL5320-27QB	20L X

Ordering and Marking Information (Cont.)

TDFN1.6x1.6-6 (Cont.)

Product Name	Marking	Product Name	Marking	Product Name	Marking	Product Name	Marking
APL5320-28QB	20M X	APL5320-29QB	20N X	APL5320-30QB	20O X	APL5320-31QB	20P X
APL5320-32QB	20Q X	APL5320-33QB	20R X	APL5320-34QB	20S X	APL5320-35QB	20T X
APL5320-36QB	20g X	APL5320-285QB	20d X				

Note: X - Code.

VTDFN1.2x1.6-4

Product Name	Marking	Product Name	Marking	Product Name	Marking	Product Name	Marking
APL5320-12QF	05 X	APL5320-13QF	07 X	APL5320-14QF	08 X	APL5320-15QF	09 X
APL5320-16QF	0A X	APL5320-17QF	0B X	APL5320-18QF	0C X	APL5320-19QF	0D X
APL5320-20QF	0E X	APL5320-21QF	0F X	APL5320-22QF	0G X	APL5320-23QF	0H X
APL5320-24QF	0I X	APL5320-25QF	0J X	APL5320-26QF	0K X	APL5320-27QF	0L X
APL5320-28QF	0M X	APL5320-29QF	0N X	APL5320-30QF	0O X	APL5320-31QF	0P X
APL5320-32QF	0Q X	APL5320-33QF	0R X	APL5320-34QF	0S X	APL5320-35QF	0T X
APL5320-36QF	0g X	APL5320-285QF	0d X				

Note : X - Code.

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{IN}	VIN to GND Voltage	-0.3 ~ 6.5	V
V_{OUT}	VOUT to GND Voltage	-0.3 ~ 6.5	V
$V_{\overline{SHDN}}$	$\overline{SHDN}$ to GND Voltage	-0.3 ~ 6.5	V
T_J	Maximum Junction Temperature	-40 ~ 150	°C
T_{STG}	Storage Temperature	-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature, 10 Seconds	260	°C

Note 1 : Absolute Maximum Ratings are those values beyond which the life of a device may be impaired. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in Free Air (Note 2)		°C/W
	SOT-23-5	240	
	SC-70-5	325	
	TDFN1.6x1.6-6	165	
	VTDFN1.2x1.6-4	100	

Note 2 : θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Recommended Operating Conditions (Note 3)

Symbol	Parameter	Range	Unit
V_{IN}	VIN Input Voltage	2.5 ~ 6	V
$V_{\overline{SHDN}}$	$\overline{SHDN}$ Input Voltage	2.5 ~ 6	V
I_{OUT}	VOUT Output Current	0 ~300	mA
V_{OUT}	Output Voltage	Fixed Voltage	
C_{OUT}	Output Capacitor	1~22	µF
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

Note 3 : Refer to the typical application circuit

Electrical Characteristics

Unless otherwise specified, these specifications apply over V_{IN}=V_{OUT}+1V, C_{IN}=C_{OUT}=1µF and T_A=-40~85 °C. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions		APL5320			Unit
				Min.	Typ.	Max.	
UNDER-VOLTAGE LOCKAGE (UVLO) AND SUPPLY CURRENT							
	VIN UVLO Threshold Voltage	V_{IN} rising, T_A=-40~85°C		1.9	2.2	2.4	V
	VIN UVLO Hysteresis			-	0.1	-	V
I_Q	Quiescent Current	I_{OUT}=0mA, $V_{\overline{SHDN}}$=5V		-	40	60	µA
		I_{OUT}=300mA $V_{\overline{SHDN}}$=5V		-	40	60	µA
I_{QSHDN}	Shut Down Supply Current	$V_{\overline{SHDN}}$=0V, V_{IN}= V_{OUT}+1V		-	-	1	µA
OUTPUT VOLTAGE							
	Output Voltage Accuracy	I_{OUT}=1mA, T_A=25 °C		-2	-	2	%
		I_{OUT}=1mA to 300mA, T_A=-40~85°C		-3	-	3	%
REG_{LINE}	Line Regulation	ΔV_{OUT}%/ ΔV_{IN}, V_{OUT}+0.3V<V_{IN}<6V, I_{OUT}=1mA		-	-	0.2	%/V
REG_{LOAD}	Load Regulation	ΔV_{OUT}%, V_{IN}= V_{OUT}+1V, 0mA<I_{OUT}<300mA		-	-	0.6	%
V_{DROP}	Dropout Voltage	V_{OUT}=1.5V, I_{OUT}=300mA		-	0.52	0.68	V
		V_{OUT}=2V, I_{OUT}=300mA		-	0.43	0.56	V
		V_{OUT}=3V, I_{OUT}=300mA		-	0.29	0.38	V
PSRR	Ripple Rejection	C_{OUT}=1µF, I_{OUT}=50mA	f=1kHz	-	70	-	dB
			f=10kHz	-	63	-	dB
			f=100kHz	-	35	-	dB
	Output Noise	f=10Hz to 100kHz, C_{OUT}=10µF, I_{OUT} = 1mA		-	100	-	μV_{RMS}
	VOUT Discharge Resistance	$V_{\overline{SHDN}}$=0V		-	0.7	-	kΩ
SHUT DOWN							
$V_{\overline{SHDN}}$	High Threshold Voltage	V_{IN}=2.5 to 6V		1.5	-	-	V
	Low Threshold Voltage	V_{IN}=2.5 to 6V		-	-	0.4	V
$I_{\overline{SHDN}}$	$\overline{SHDN}$ Input Current	$V_{\overline{SHDN}}$=5V		-	0.2	-	µA

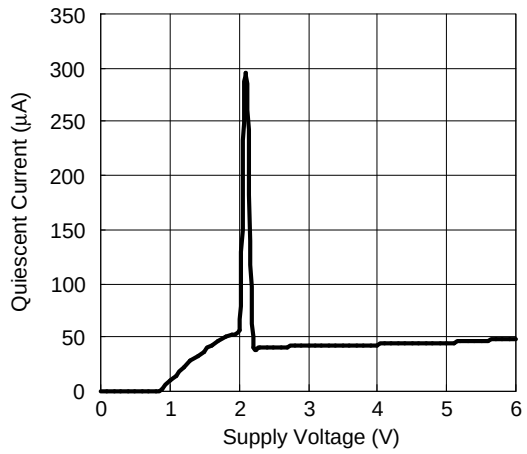
Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over V_{IN}=V_{OUT}+1V, C_{IN}=C_{OUT}=1µF and T_A=-40~85 °C. Typical values are at T_A=25°C.

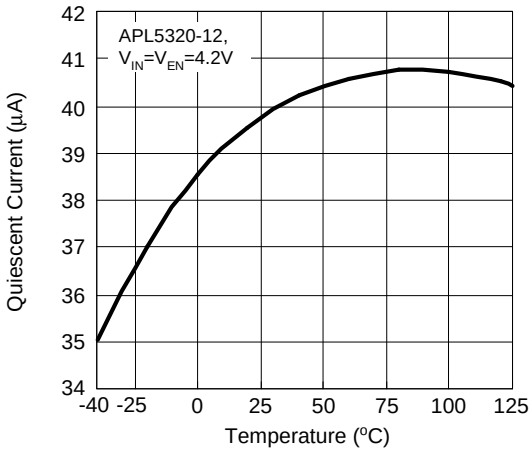
Symbol	Parameter	Test Conditions	APL5320			Unit
			Min.	Typ.	Max.	
PROTECTIONS						
I_{LIMIT}	Current Limit Threshold		330	450	750	mA
I_{SHORT}	Short Circuit Current	V_{OUT} =0V	-	50	-	mA
t_{SS}	Soft-Start	V_{OUT} rising from 0 to 90%, R_{LOAD}=50Ω	-	60	-	µs
T_{OTP}	Over-Temperature Threshold	T_J rising	-	160	-	°C
	Over-Temperature Hysteresis		-	40	-	°C

Typical Operating Characteristics

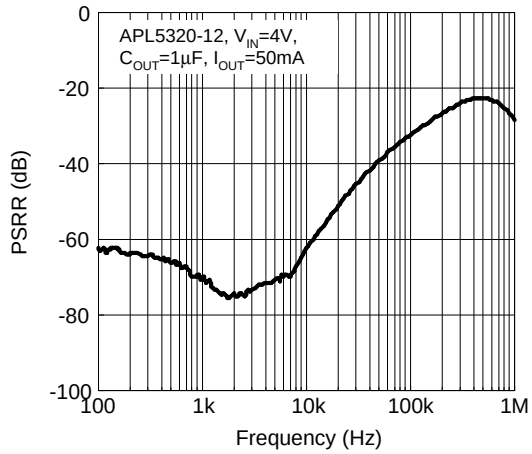
Quiescent Current vs. Supply Voltage



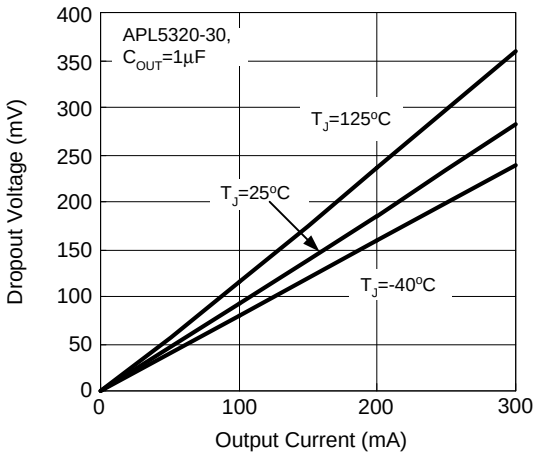
Quiescent Current vs. Temperature



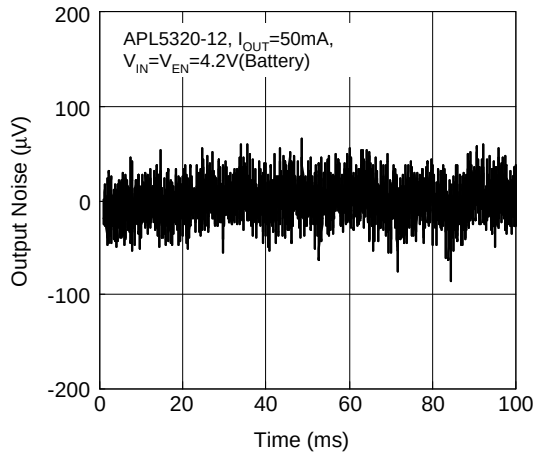
PSRR vs. Frequency



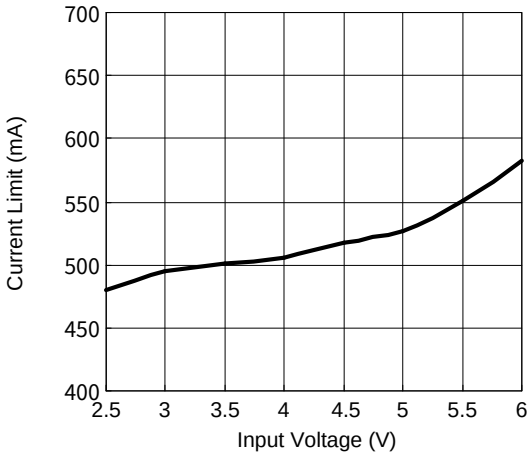
Dropout Voltage vs. Output Current



Output Noise

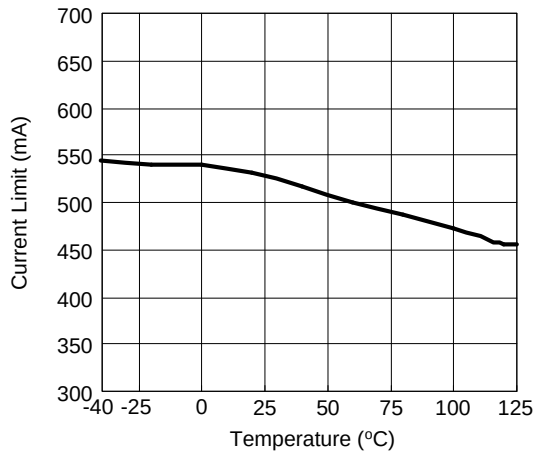


Current Limit Threshold vs. Input Voltage

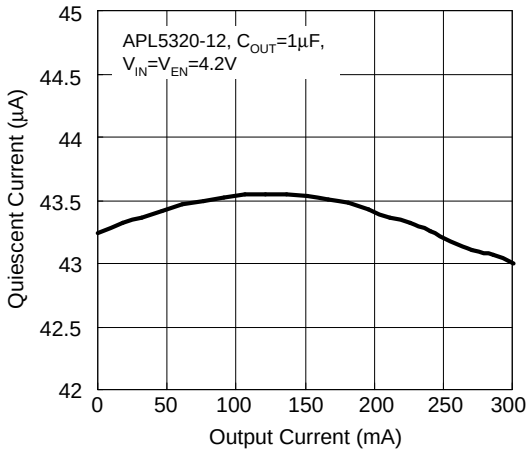


Typical Operating Characteristics (Cont.)

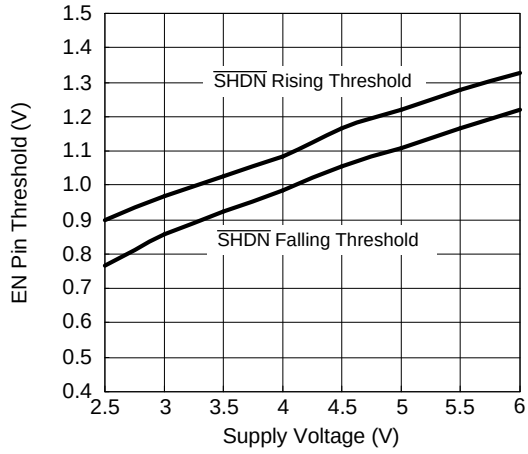
Current Limit Threshold vs. Temperature



Quiescent Current vs. Output Current



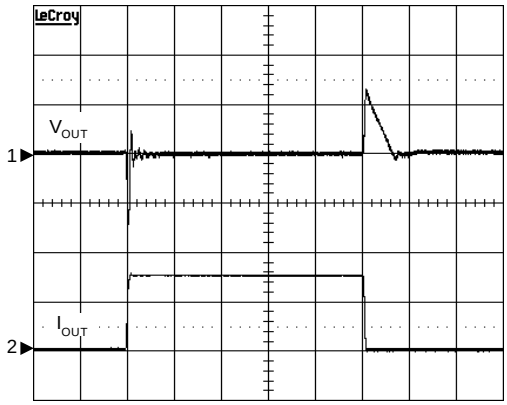
$\overline{SHDN}$ Pin Threshold Voltage vs. Supply Voltage



Operating Waveforms

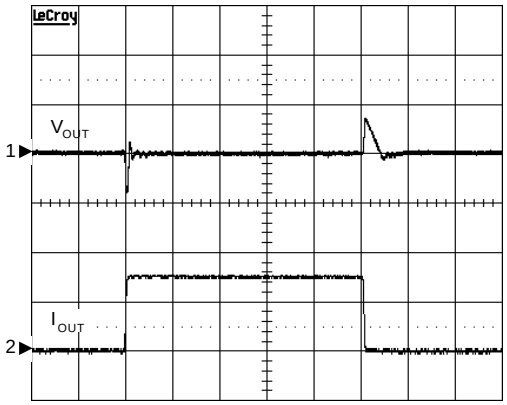
The test condition is V_{IN}=4.2V, T_A= 25°C unless otherwise specified.

Load Transient Response



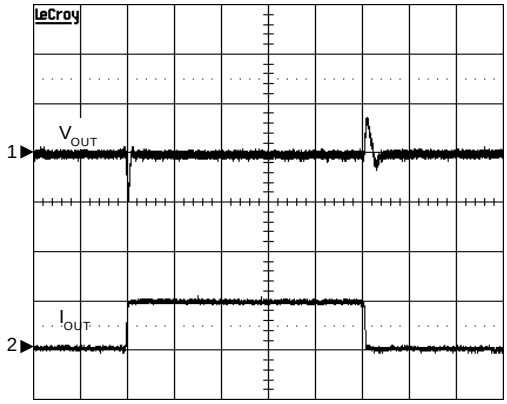
V_{IN} =4.2V, V_{OUT}=1.2V, C_{IN} =C_{OUT} =1µF,
I_{OUT} =10mA to 300mA to 10mA (Rise/Fall time=1µs)
CH1: V_{OUT}, 50mV/Div, DC, Offset=1.2V
CH2: I_{OUT}, 200mA/Div, DC
TIME: 20µs/Div

Load Transient Response



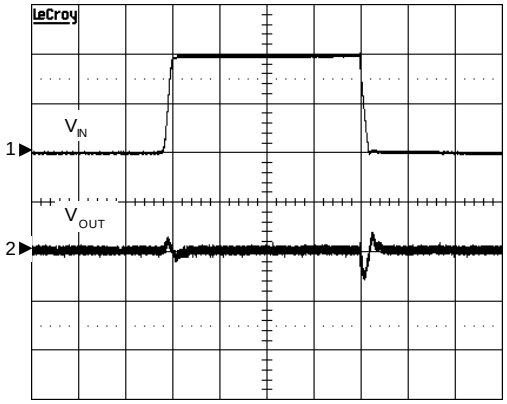
V_{IN} =4.2V, V_{OUT}=1.2V, C_{IN} =C_{OUT} =1µF,
I_{OUT} =10mA to 150mA to 10mA (Rise/Fall time=1µs)
CH1: V_{OUT}, 50mV/Div, DC, Offset=1.2V
CH2: I_{OUT}, 100mA/Div, DC
TIME: 20µs/Div

Load Transient Response



V_{IN} =4.2V, V_{OUT}=1.2V, C_{IN} =C_{OUT} =1µF,
I_{OUT} =10mA to 50mA to 10mA (Rise/Fall time=1µs)
CH1: V_{OUT}, 20mV/Div, DC, Offset=1.2V
CH2: I_{OUT}, 50mA/Div, DC
TIME: 20µs/Div

Line Transient Response

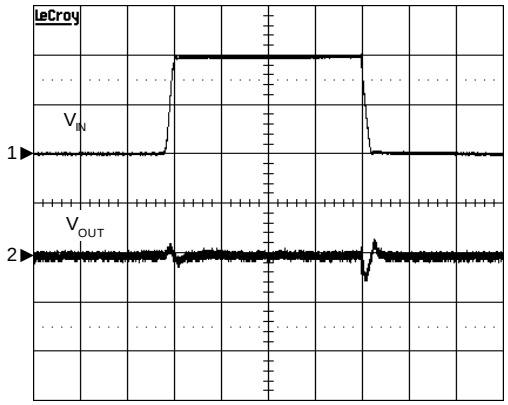


V_{IN} =3.8V to 4.8V to 3.8V (Rise/Fall time=4µs),
V_{OUT}=1.2V, C_{IN} =C_{OUT} =1µF, I_{OUT} =100mA
CH1: V_{IN}, 500mV/Div, DC, Offset=3.8V
CH2: V_{OUT}, 20mV/Div, DC, Offset=1.2V
TIME: 20µs/Div

Operating Waveforms (Cont.)

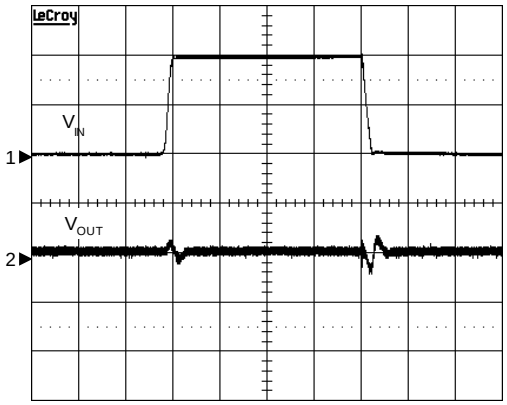
The test condition is V_{IN}=4.2V, T_A= 25°C unless otherwise specified.

Line Transient Response



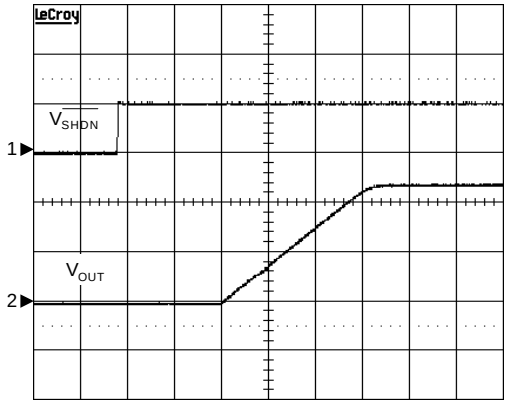
V_{IN} =3.8V to 4.8V to 3.8V (Rise/Fall time=4µs),
V_{OUT}=1.2V, C_{IN} =C_{OUT} =1µF, I_{OUT} =50mA
CH1: V_{IN}, 500mV/Div, DC, Offset=3.8V
CH2: V_{OUT}, 20mV/Div, DC, Offset=1.2V
TIME: 20µs/Div

Line Transient Response



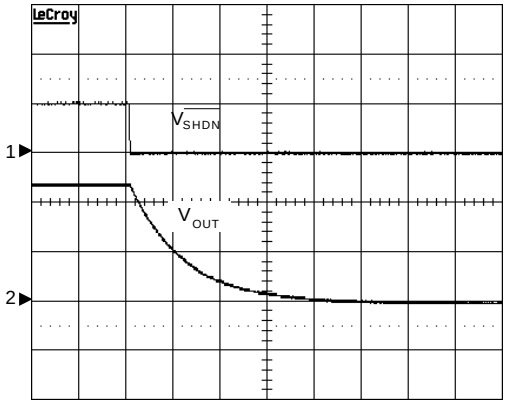
V_{IN} =3.8V to 4.8V to 3.8V (Rise/Fall time=4µs),
V_{OUT}=1.2V, C_{IN} =C_{OUT} =1µF, I_{OUT} =10mA
CH1: V_{IN}, 500mV/Div, DC, Offset=3.8V
CH2: V_{OUT}, 20mV/Div, DC, Offset=1.2V
TIME: 20µs/Div

Exiting Shutdown



V_{IN} =4.2V, V_{OUT}=1.2V, C_{IN} =C_{OUT} =1µF,
I_{OUT} =10mA
CH1: $V_{\overline{SHDN}}$, 2V/Div, DC
CH2: V_{OUT}, 500mV/Div, DC
TIME: 20µs/Div

Entering Shutdown

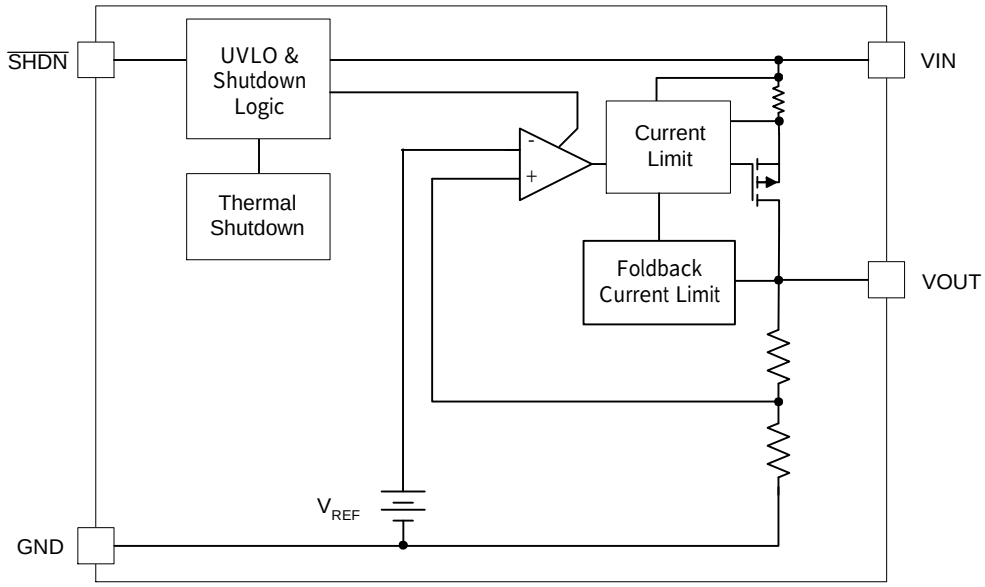


V_{IN} =4.2V, V_{OUT}=1.2V, C_{IN} =C_{OUT} =1µF,
I_{OUT} =10mA
CH1: $V_{\overline{SHDN}}$, 2V/Div, DC
CH2: V_{OUT}, 500mV/Div, DC
TIME: 10µs/Div

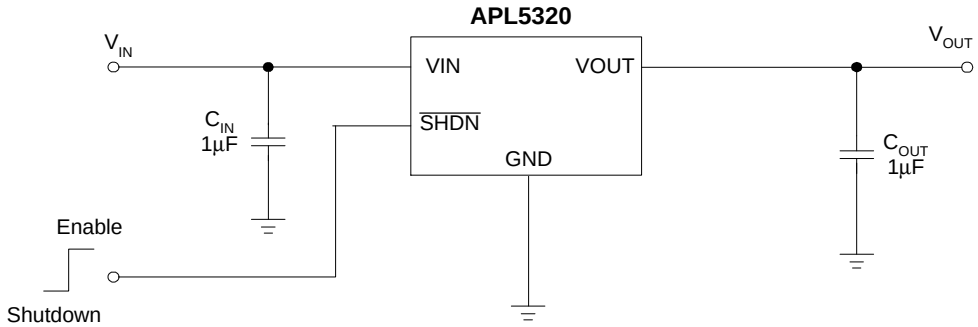
Pin Description

PIN			NAME	FUNCTION
NO.				
SOT-23-5/ SC-70-5	TDFN 1.6x1.6-6	VTDFN 1.2x1.6-4		
1	3	4	VIN	Voltage Supply Input Pin.
2	6	2	GND	Ground.
3	1	3	$\overline{SHDN}$	Shut Down Control Pin. Logic high: enable; logic low: shutdown. This pin can not be left floating.
4	2, 5	-	NC	NC Pin.
5	4	1	VOUT	Regulator Output Pin.

Block Diagram



Typical Application Circuit



Function Description

Internal Soft-Start

An internal soft-start function controls rising rate of the output voltage to limit the surge current at start-up. The typical soft-start interval is about 60μs.

Thermal Shutdown

A thermal shutdown circuit limits the junction temperature of APL5320. When the junction temperature exceeds +160°C, a thermal sensor turns off the output PMOS, allowing the device to cool down. The regulator regulates the output again through initiation of a new soft-start cycle after the junction temperature cools by 40°C.The thermal shutdown is designed with a 40°C hysteresis to lower the average junction temperature during continuous thermal overload conditions, extending lifetime of the device. For normal operation, device power dissipation should be externally limited so that junction temperature will not exceed 125°C.

Current-Limit with Current Foldback

The APL5320 monitors the current via the output PMOS and limits the maximum current. When the output current reaches the current limit threshold, current limit with current foldback circuit starts to work to prevent load and APL5320 from damages during overload or short-circuit conditions. Typical foldback current is about 50mA.

Shutdown Control

The APL5320 has an active-low shutdown function. Forcing $\overline{SHDN}$ high (>1.5V) enables the V_{OUT}; forcing $\overline{SHDN}$ low (<0.4V) disables the V_{OUT}. The $\overline{SHDN}$ can not be left floating. If it is not used, connect it to VIN for normal operation.

Under-Voltage Lock Out (UVLO)

The APL5320 monitors the input voltage to prevent wrong logic control. The UVLO function initiates a soft-start process after input voltage exceeds its rising UVLO threshold during power on. The UVLO function also shuts off the output when the input voltage falls below it's falling threshold.

Application Information

Input capacitor

The APL5320 requires proper input capacitors to supply surge current during stepping load transients to prevent the input rail from dropping. Because the parasitic inductor from the voltage sources or other bulk capacitors to the VIN limit the slew rate of the surge current, place the Input capacitors near VIN as close as possible. Input capacitors should be larger than 1μF and a minimum ceramic capacitor of 1μF is necessary.

Output Capacitor

The APL5320 needs a proper output capacitor to maintain circuit stability and improve transient response over temperature and current. In order to insure the circuit stability, the proper output capacitor value should be larger than 1μF. With X5R and X7R dielectrics, 1μF is sufficient at all operating temperatures. Large output capacitor value can reduce noise and improve load-transient response and PSRR, Figure 1 shows the curves of allowable ESR range as the function of load current for various output capacitor values.

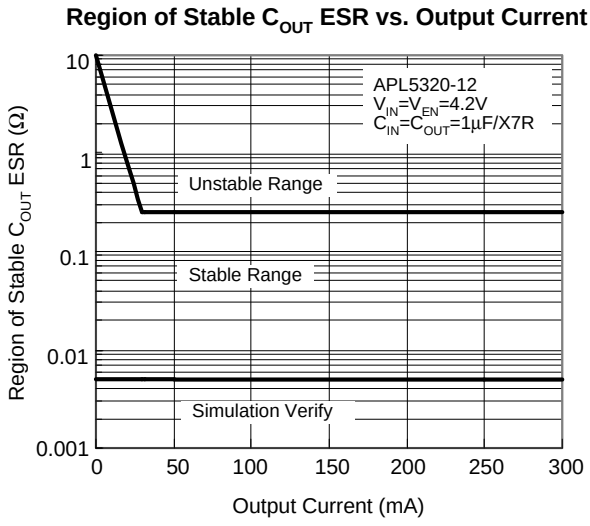


Figure1. Stable C_{OUT} ESR Range

Operation Region and Power Dissipation

The APL5320 maximum power dissipation depends on the thermal resistance and temperature difference between the die junction and ambient air. The TDFN1.6x1.6-6 package power dissipation P_D across the device is:

$$P_D = (T_J - T_A) / \theta_{JA}$$

where $(T_J - T_A)$ is the temperature difference between the junction and ambient air. θ_{JA} is the thermal resistance between Junction and ambient air. Assuming the T_A=25°C and maximum T_J=160°C (typical thermal limit threshold), the maximum power dissipation is calculated as:

$$P_D(max)=(160-25)/165=0.81(W)$$

For normal operation, do not exceed the maximum junction temperature rating of T_J=125°C. The calculated power dissipation should be less than:

$$P_D=(125-25)/165=0.6(W)$$

The GND provides an electrical connection to the ground and channels heat away. Connect the GND to the ground by using a large pad or a ground plane.

Layout Consideration

Figure 2 illustrates the layout. Below is a checklist for your layout:

1. Please place the input capacitors close to the VIN.
2. Ceramic capacitors for load must be placed near the load as close as possible.
3. To place APL5320 and output capacitors near the load is good for performance.
4. Large current paths, the bold lines in figure 2, must have wide tracks.

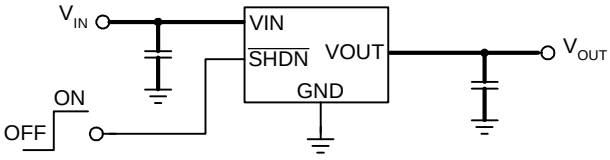
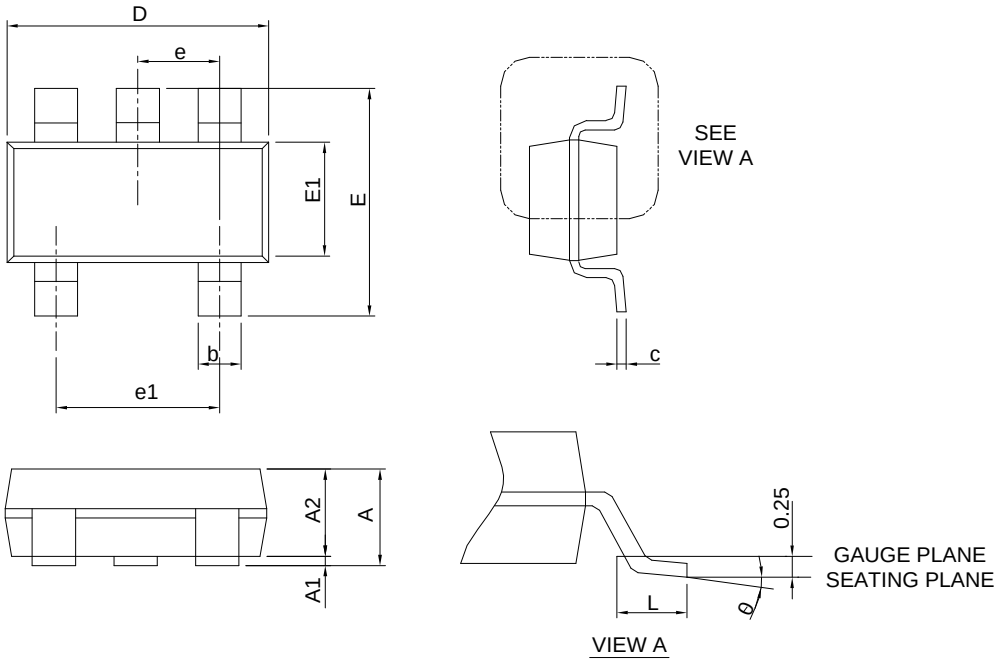


Figure2. Large Current Paths Shown as Bold Lines

Package Information

SOT-23-5

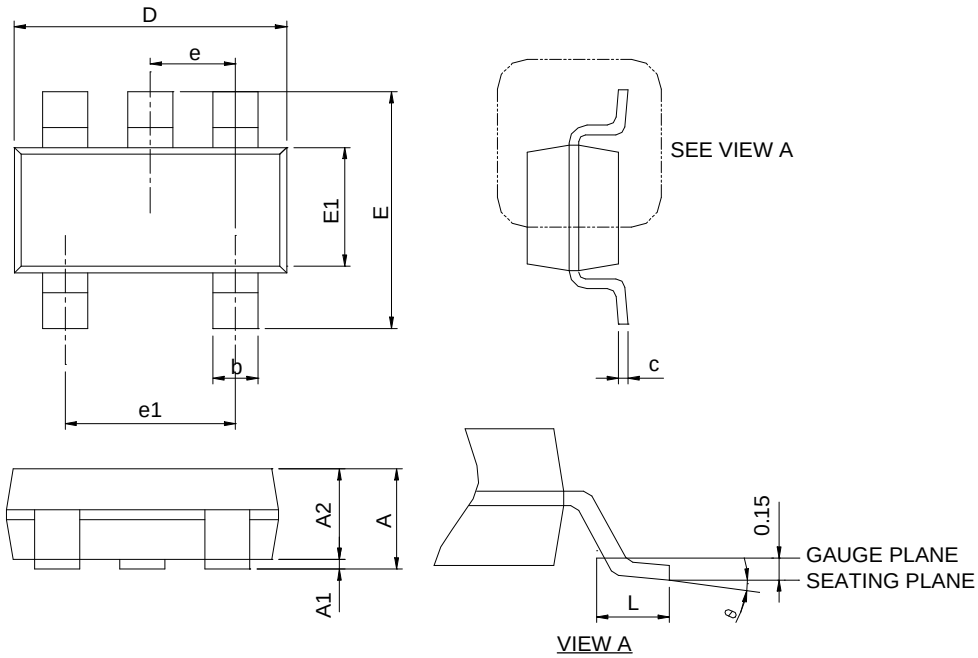


SYMBOL	SOT-23-5			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.45		0.057
A1	0.00	0.15	0.000	0.006
A2	0.90	1.30	0.035	0.051
b	0.30	0.50	0.012	0.020
c	0.08	0.22	0.003	0.009
D	2.70	3.10	0.106	0.122
E	2.60	3.00	0.102	0.118
E1	1.40	1.80	0.055	0.071
e	0.95 BSC		0.037 BSC	
e1	1.90 BSC		0.075 BSC	
L	0.30	0.60	0.012	0.024
θ	0°	8°	0°	8°

Note : 1. Follow JEDEC TO-178 AA.
2. Dimension D and E1 do not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 10 mil per side.

Package Information

SC-70-5

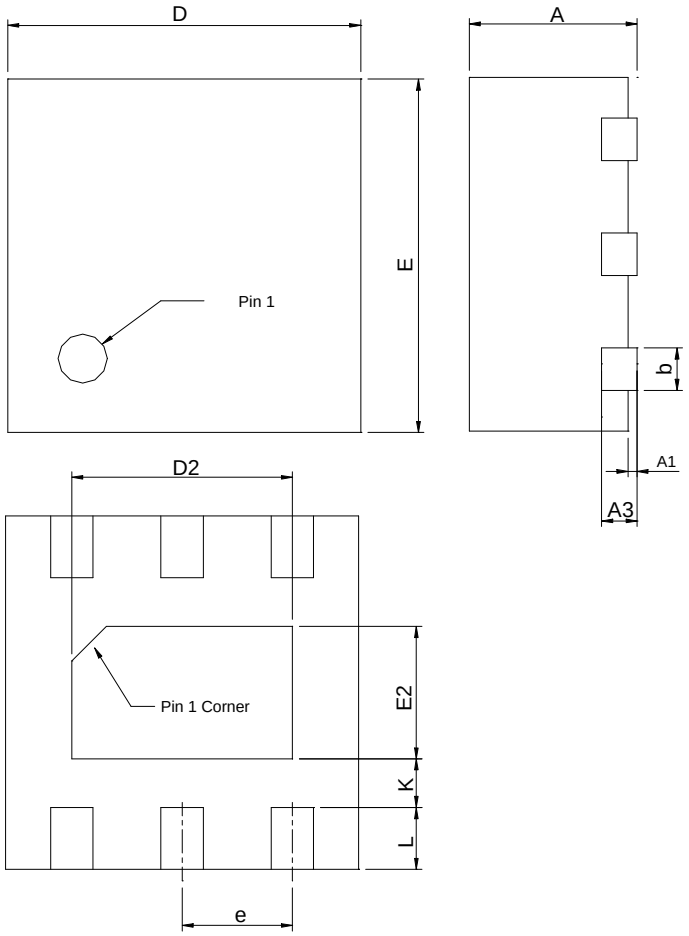


SYMBOL	SC-70-5			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.80	1.10	0.031	0.043
A1	0.00	0.10	0.000	0.004
A2	0.80	1.00	0.031	0.040
b	0.15	0.30	0.006	0.012
c	0.08	0.25	0.003	0.010
D	1.90	2.20	0.075	0.087
E	2.00	2.40	0.079	0.095
E1	1.15	1.35	0.045	0.053
e	0.65 BSC		0.026 BSC	
e1	1.30 BSC		0.051 BSC	
L	0.15	0.45	0.006	0.018
θ	0°	8°	0°	8°

Note : 1. Followed from JEDEC MO-223 AB.
2. Dimension D and E1 do not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.

Package Information

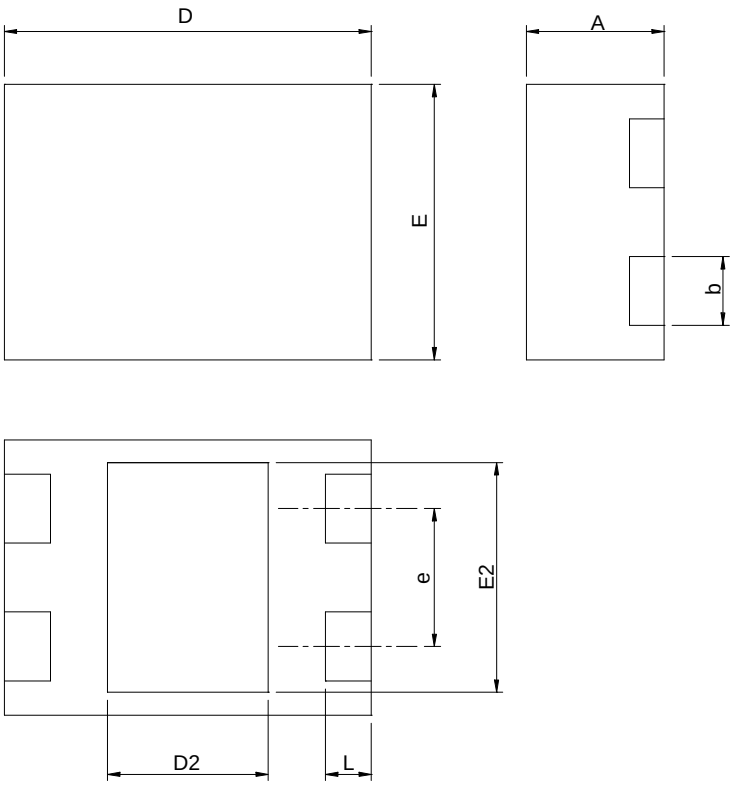
TDFN1.6x1.6-6



SYMBOL	TDFN1.6x1.6-6			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.20	0.30	0.008	0.012
D	1.55	1.65	0.061	0.065
D2	0.95	1.05	0.037	0.041
E	1.55	1.65	0.061	0.065
E2	0.55	0.65	0.022	0.026
e	0.50 BSC		0.020 BSC	
K	0.20	-	0.008	-
L	0.19	0.29	0.007	0.011

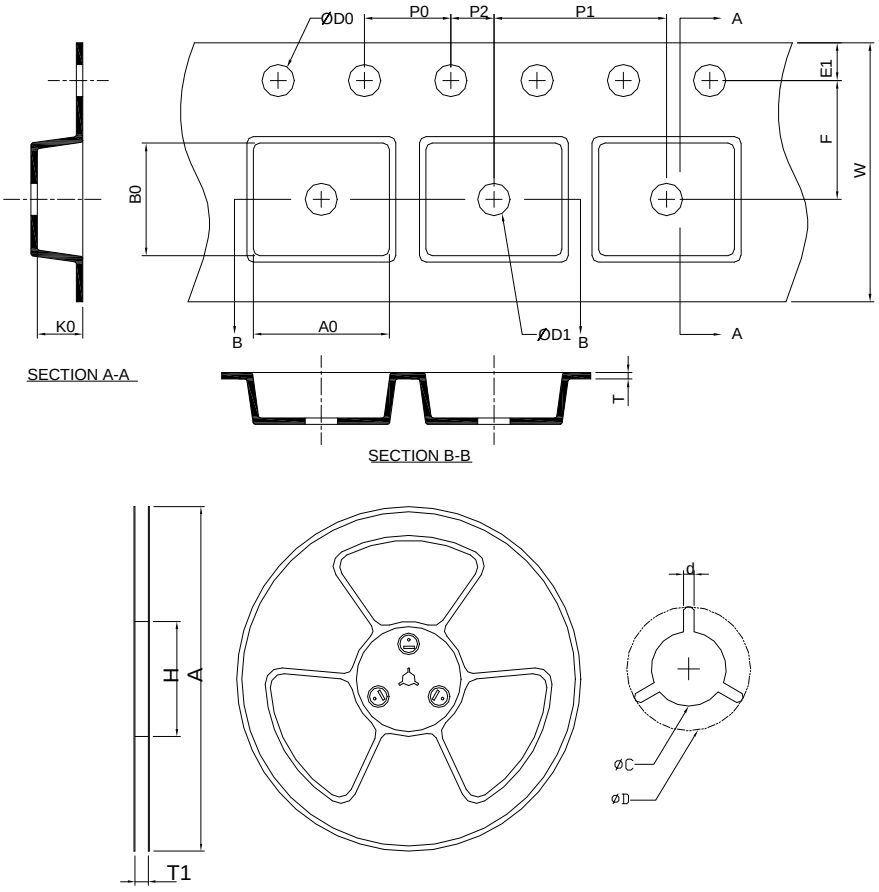
Package Information

VTDFN1.2x1.6-4



SYMBOL	VTDFN1.2x1.6-4			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.50	0.60	0.020	0.024
b	0.25	0.35	0.010	0.014
D	1.55	1.65	0.061	0.065
D2	0.65	0.75	0.026	0.030
E	1.15	1.25	0.045	0.049
E2	0.95	1.05	0.037	0.041
e	0.60 BSC		0.024 BSC	
L	0.10	0.30	0.004	0.012

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
SOT-23-5	178.0±2.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	8.0±0.30	1.75±0.10	3.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	4.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.0 MIN.	0.6+0.00 -0.40	3.20±0.20	3.10±0.20	1.50±0.20
Application	**A**	**H**	**T1**	**C**	**d**	**D**	**W**	**E1**	**F**
SC-70-5	178.0±2.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	8.0±0.30	1.75±0.10	3.50±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	4.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.00 MIN.	0.6+0.00 -0.40	2.40±0.20	2.40±0.20	1.20±0.20
Application	**A**	**H**	**T1**	**C**	**d**	**D**	**W**	**E1**	**F**
TDFN1.6x1.6-6	178.0±2.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	8.0±0.30	1.75±0.10	3.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	4.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	1.70±0.20	1.70±0.20	0.90±0.20

(mm)

Carrier Tape & Reel Dimensions (Cont.)

Application	A	H	T1	C	d	D	W	E1	F
VTDFN1.2x1.6-4	178.0±2.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	8.0±0.20	1.75±0.10	3.50±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	4.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.4	1.4 MIN	1.8 MIN	1.30±0.20

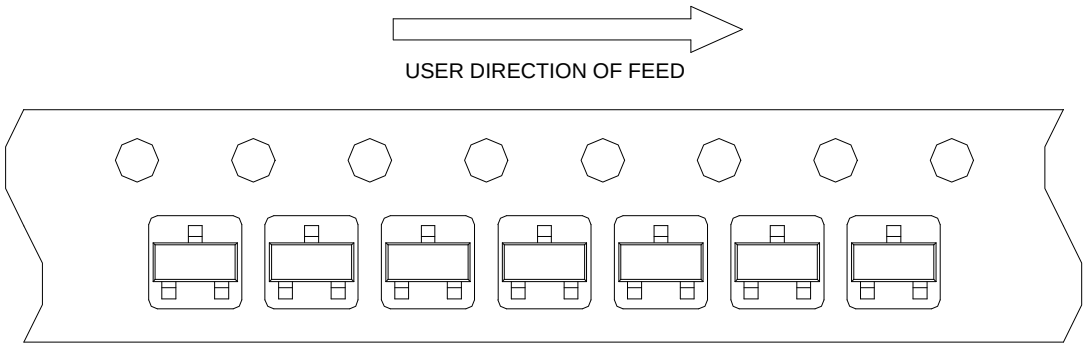
(mm)

Devices Per Unit

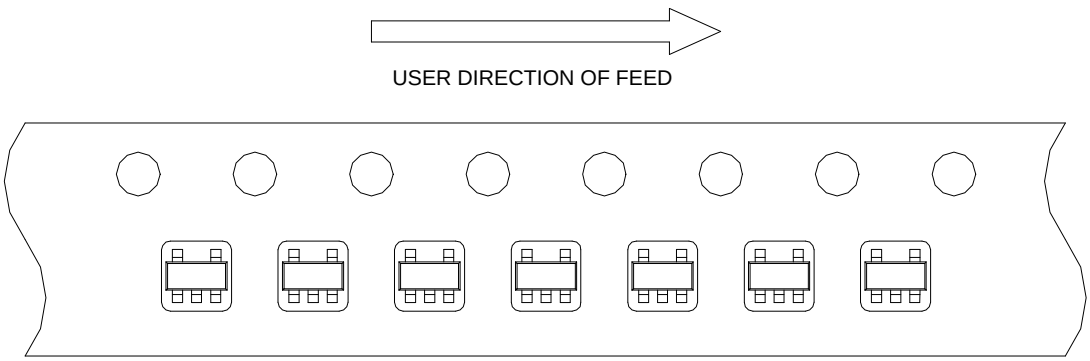
Package Type	Unit	Quantity
SOT-23-5	Tape & Reel	3000
SC-70-5	Tape & Reel	3000
TDFN1.6x1.6-6	Tape & Reel	3000
VTDFN1.2x1.6-4	Tape & Reel	3000

Taping Direction Information

SOT-23-5

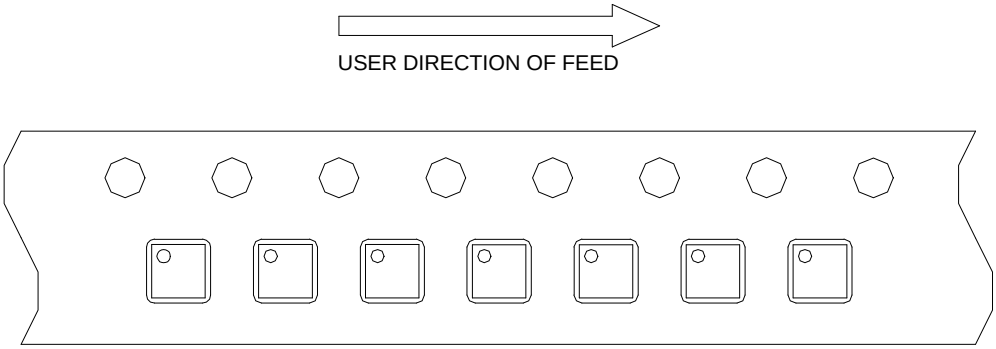


SC-70-5

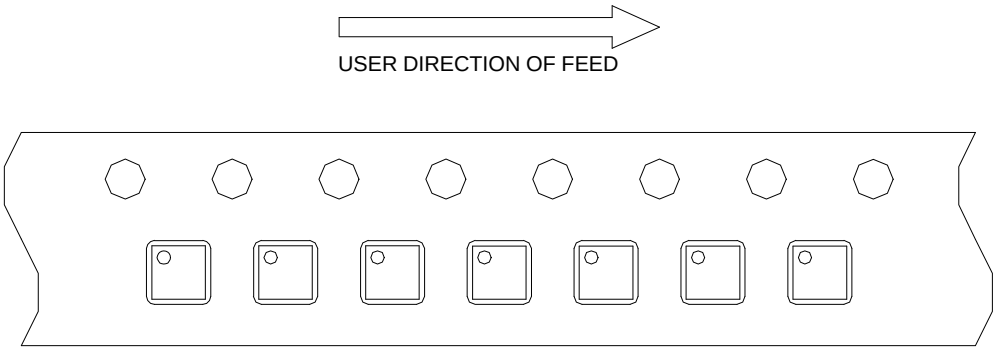


Taping Direction Information (Cont.)

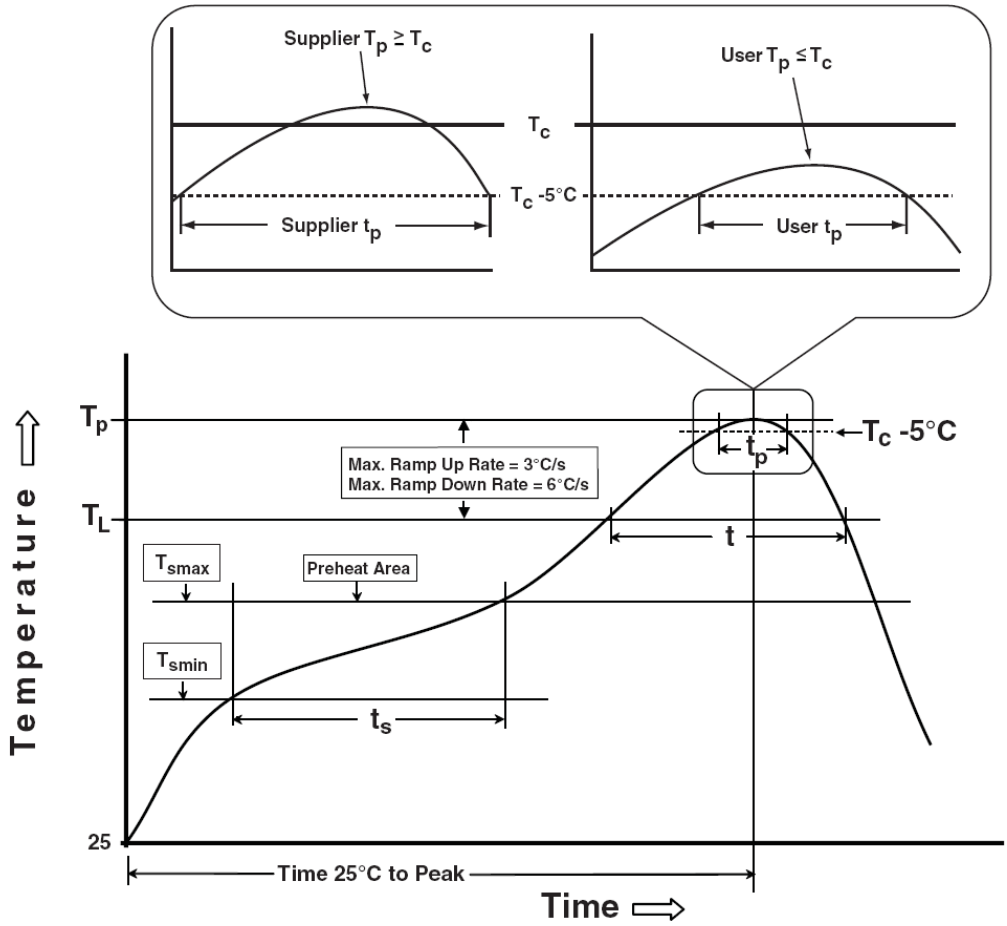
TDFN1.6x1.6-6



VTDFN1.2x1.6-4



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Classification Reflow Profiles (Cont.)

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

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