
DATA SHEET

HM 65728B

**2 K x 8
HIGH SPEED CMOS SRAM**

FEATURES

- **FAST ACCESS TIME**
COMMERCIAL : 25/35/45/55 ns (max)
MILITARY : 25/35/45/55 ns (max)
- **LOW POWER CONSUMPTION**
ACTIVE : 550 mW (max)
STANDBY : 110 mW (max)
- **WIDE TEMPERATURE RANGE :**
- 55°C TO + 125°C
- **300 AND 600 MILS WIDTH PACKAGE**
- **TTL COMPATIBLE INPUTS AND OUTPUTS**
- **ASYNCHRONOUS**
- **CAPABLE OF WITHSTANDING GREATER THAN 2000 V ELECTROSTATIC DISCHARGE**
- **SINGLE 5 VOLT SUPPLY**

INTRODUCTION

The HM 65728B is a high speed CMOS static RAM organized as 2048 x 8 bits. It is manufactured using MHS's high performance CMOS technology. Access times as fast as 25 ns are available with maximum power consumption of only 600 mW. The HM 65728B features fully static operation requiring no external clocks or timing strobes. The automatic power-down feature reduces the power consumption by 80 % when the circuit is deselected.

Easy memory expansion is provided by an active low chip select (CS) and active low output enable (OE) and three state drivers.

All inputs and outputs of the HM 65728 are TTL compatible and operate from single 5V supply thus simplifying system design.

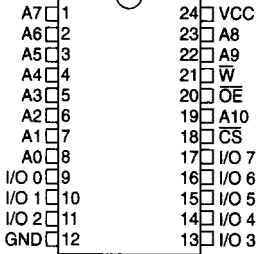
The HM 65728B is 100 % processed following the test methods of MIL STD 883C and/or ESA/SCC 9000 making it ideally suitable for military/space applications that demand superior levels of performance and reliability.

INTERFACE

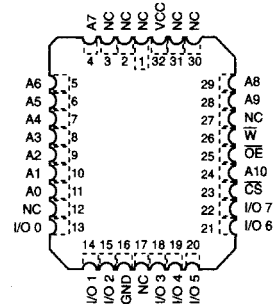
PIN CONFIGURATION

Ceramic 300 mils, 24 pins, DIL
Plastic 300 & 600 mils, 24 pins, DIL
SOIC 300 mils, 24 pins

LCC, 32 pins

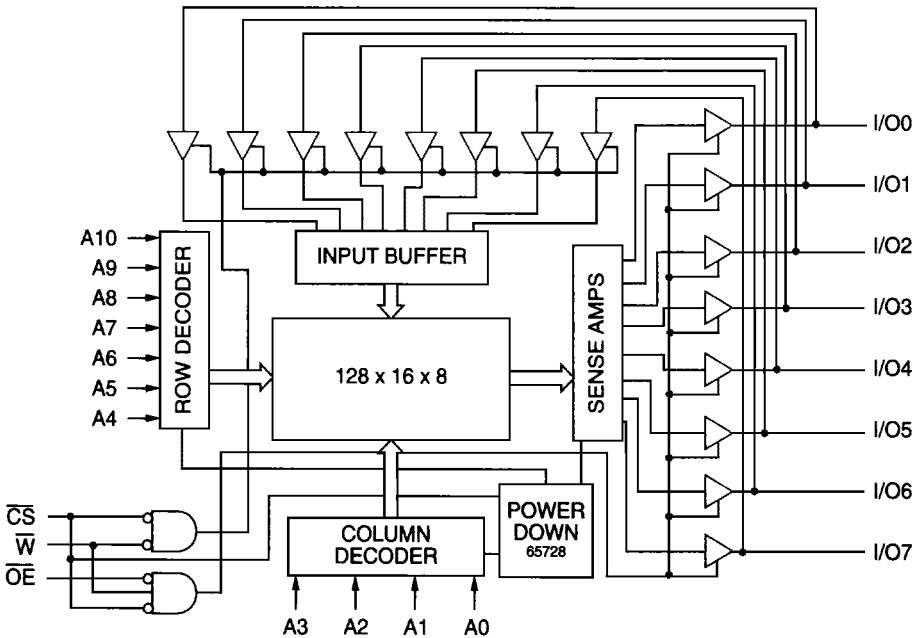


Pinout DIL/SOIC 24 pins (top view)

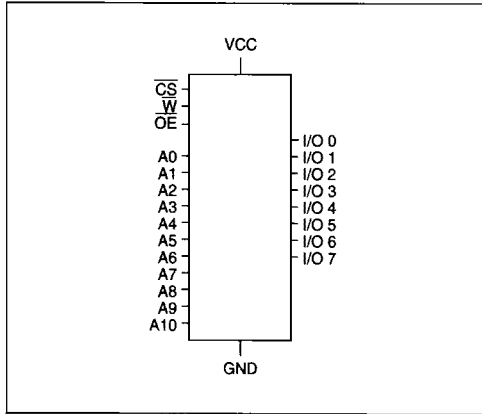


Pinout LCC 32 pins (top view)

BLOCK DIAGRAM



LOGIC SYMBOL



PIN NAMES

A0-A10 : Address inputs	CS : Chip Select
I/O0-I/O7 : Input/Output	OE : Output Enable
Vcc : Power	W : Write enable
Gnd : Ground	

TRUTH TABLE

CS	OE	W	DATA-IN	DATA-OUT	MODE
H	X	X	Z	Z	Deselect
L	L	H	Z	Valid	Read
L	H	L	Valid	Z	Write
L	L	L	Valid	Z	Write

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Supply voltage to GND potential : $-0.5\text{ V to }+7.0\text{ V}$
 DC input voltage : $-3.0\text{ V to }+7.0\text{ V}$
 DC output voltage in high Z state : $-0.5\text{ V to }+7.0\text{ V}$

Storage temperature : $-65^{\circ}\text{C to }+150^{\circ}\text{C}$
 Output current into outputs (low) : 20 mA
 Electro Static Discharge Voltage > 200 V
 (MIL STD 883C METHOD 3015.2)

OPERATING RANGE

		OPERATING VOLTAGE	OPERATING TEMPERATURE
Military	(-2)	$5\text{ V} \pm 10\%$	$-55^{\circ}\text{C to }+125^{\circ}\text{C}$
Commercial	(-5)	$5\text{ V} \pm 10\%$	$0^{\circ}\text{C to }+70^{\circ}\text{C}$

RECOMMENDED DC OPERATING CONDITIONS

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Vcc	Supply Voltage	4.5	5.0	5.5	V
Gnd	Ground	0.0	0.0	0.0	V
VIL	Input low voltage	-0.3	0.0	0.8	V
VIH	Input high voltage	2.2	-	5.5	V

CAPACITANCE

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Cin (1)	Input capacitance	-	-	5	pF
Cout (1)	Output capacitance	-	-	7	pF

Note : 1. TA = 25°C, f = 1 MHz, Vcc = 5.0 V, these parameters are not tested.

DC PARAMETERS

PARAMETER		DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
IIX	(2)	Input leakage current	- 10.0	-	10.0	μA
IOZ	(3)	Output leakage current	- 10.0	-	10.0	μA
IOS	(3)	Output short circuit current	-	-	- 300.0	mA
VOL	(4)	Output low voltage	-	-	0.4	V
VOH	(5)	Output high voltage	2.4	-	-	V

- Notes :**
2. $\text{Gnd} < \text{Vin} < \text{Vcc}$, $\text{Gnd} < \text{Vout} < \text{Vcc}$ Output disabled.
 3. $\text{Vcc} = \text{max}$, $\text{Vout} = \text{Gnd}$, duration of the short circuit should not exceed 30 seconds.
Not more than 1 output should be shorted at one time.
 4. Vcc min , $\text{IOL} = 8.0 \text{ mA}$.
 5. Vcc min , $\text{IOH} = -4.0 \text{ mA}$.

CONSUMPTION FOR COMMERCIAL (- 5) SPECIFICATION

SYMBOL		PARAMETER	65728B H-5	65728B K-5	65728B M-5	65728B N-5	UNIT	VALUE
ICCSB	(6)	Standby supply current	20	20	20	30	mA	max
ICCOP	(7)	Dynamic operating current	100	100	100	100	mA	max

CONSUMPTION FOR MILITARY (- 2) SPECIFICATION

SYMBOL		PARAMETER	65728B H-2	65728B K-2	65728B M-2	65728B N-2	UNIT	VALUE
ICCSB	(6)	Standby supply current	40	30	30	30	mA	max
ICCOP	(7)	Dynamic operating current	120	120	120	120	mA	max

- Notes :**
6. $\text{CS} \geq \text{VIH}$, a pull-up resistor to Vcc on the CS input is required to keep the device deselected during Vcc power-up otherwise ICCSB will exceed values above.
 7. Vcc max , Output current = 0 mA, $f = \text{max}$, $\text{Vin} = \text{Vcc}$ or Gnd .

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AC PARAMETERS

AC CONDITIONS :

Input pulse levels : Gnd to 3.0 V
Input rise : 5 ns

Input timing reference levels : 1.5 V
Output loading IOL/IOH (see figure 1a and 1b) : + 30 pF

AC TEST LOADS AND WAVEFORMS

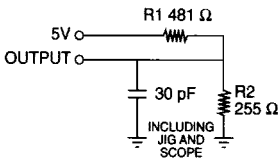


Figure 1 a

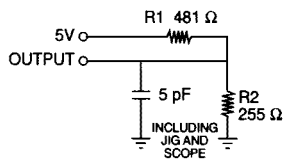


Figure 1 b

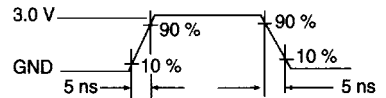
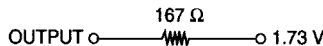


Figure 2

Equivalent to : THEVENIN EQUIVALENT



WRITE CYCLE : COMMERCIAL (– 5) SPECIFICATION

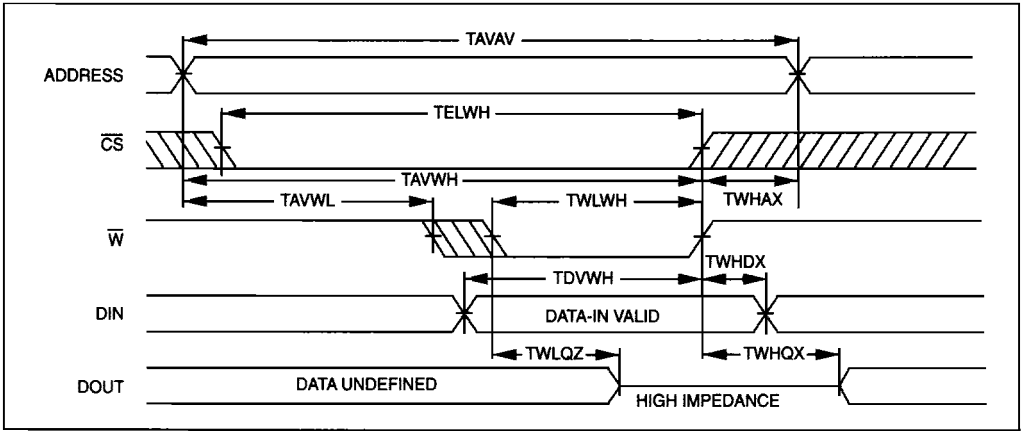
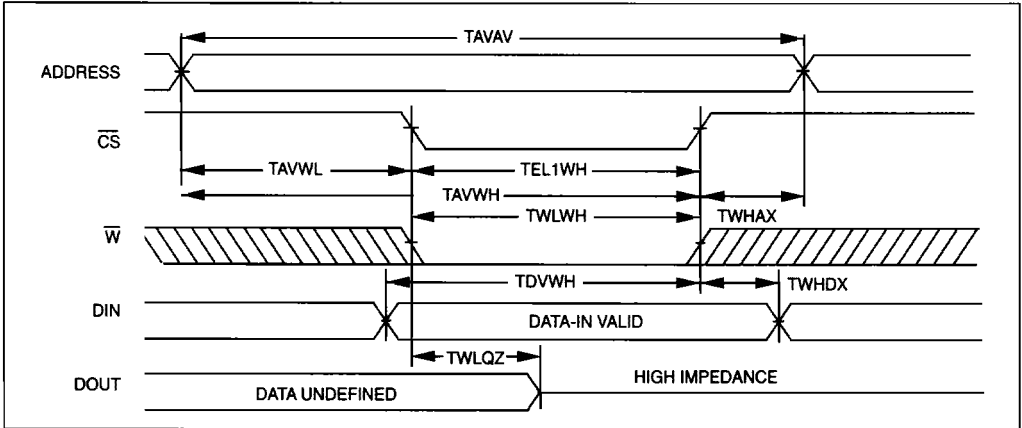
SYMBOL	PARAMETER	65728B H-5	65728B K-5	65728B M-5	65728B N-5	UNIT	VALUE
TAVAV	Write cycle time	25	35	45	55	ns	min
TAVWL	Address set-up time	0	0	0	0	ns	min
TAVWH	Address valid to end of write	20	30	40	50	ns	min
TDVWH	Data set-up time	15	15	20	25	ns	min
TELWH	CS low to write end	20	30	40	50	ns	min
TWLQZ (8)	Write low to high Z	10	15	15	20	ns	max
TWLWH	Write pulse width	20	20	20	30	ns	min
TWHAX	Address hold to end of write	2	2	2	2	ns	min
TWHDX	Data hold time	0	0	0	5	ns	min
TWHQX (8, 9)	Write high to low Z	3	0	0	0	ns	min
TEHAX	Address hold end CS	3	3	3	3	ns	min

Notes : 8. The data input set up and hold timing should be referenced to the rising edge of the signal that terminates the write.

9. At any given temperature and voltage condition, TWHQX is less than TWLQZ for all devices. These parameters are sampled and not 100 % tested.

WRITE CYCLE : MILITARY (– 2) SPECIFICATION

SYMBOL	PARAMETER	65728B H-2	65728B K-2	65728B M-2	65728B N-2	UNIT	VALUE
TAVAV	Write Cycle time	25	35	45	55	ns	min
TAVWL	Address set-up time	0	0	0	0	ns	min
TAVWH	Address valid to end of write	20	30	40	50	ns	min
TDVWH	Data set-up time	15	15	20	25	ns	min
TELWH	CS low to write end	20	30	40	50	ns	min
TWLQZ (8)	Write low to high Z	10	15	15	20	ns	max
TWLWH	Write pulse width	20	20	25	30	ns	min
TWHAX	Address hold to end of write	2	2	2	2	ns	min
TWHDX	Data hold time	5	5	5	5	ns	min
TEHAX	Address hold end CS	3	3	3	3	ns	min

WRITE CYCLE 1 ($\overline{W}$ CONTROLLED)WRITE CYCLE 2 ($\overline{CS}$ CONTROLLED)

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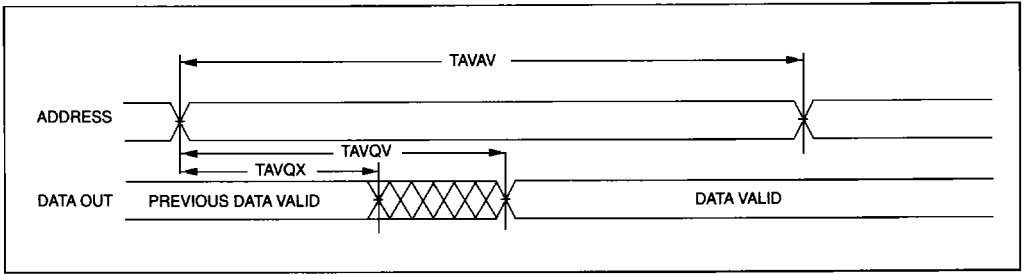
READ CYCLE : COMMERCIAL (– 5) SPECIFICATION

SYMBOL	PARAMETER	65728B H-5	65728B K-5	65728B M-5	65728B N-5	UNIT	VALUE
TAVAV	Read cycle time	25	35	45	55	ns	min
TAVQV	Address access time	25	35	45	55	ns	max
TAVQX	Address valid to low Z	5	5	5	5	ns	min
TELQV	Chip-select access time	25	35	45	55	ns	max
TELQX	$\overline{\text{CS}}$ low to low Z	5	5	5	5	ns	min
TEHQZ	$\overline{\text{CS}}$ high to high Z	12	15	20	20	ns	max
TELIC	$\overline{\text{CS}}$ low to power up	0	0	0	0	ns	min
TEHICL	$\overline{\text{CS}}$ high to power down	15	20	25	25	ns	max
TGLQV	Output enable access time	15	15	20	25	ns	max
TGLQX	$\overline{\text{OE}}$ low to low Z	2	0	0	0	ns	min
TGHQZ	$\overline{\text{OE}}$ high to high Z	10	15	15	20	ns	max

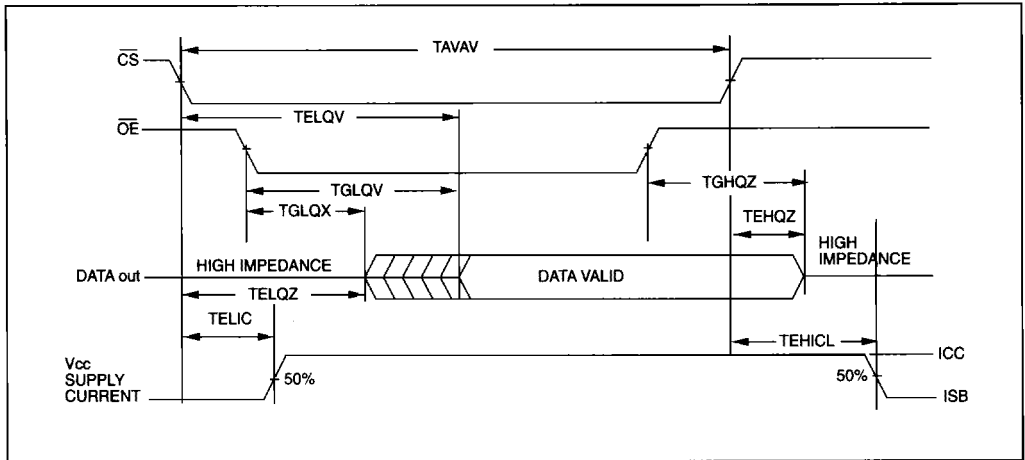
READ CYCLE : MILITARY (– 2) SPECIFICATION

SYMBOL	PARAMETER	65728B H-2	65728B K-2	65728B M-2	65728B N-2	UNIT	VALUE
TAVAV	Read cycle time	25	35	45	55	ns	min
TAVQV	Address access time	25	35	45	55	ns	max
TAVQX	Address valid to low Z	5	5	5	5	ns	min
TELQV	Chip-select access time	25	35	45	55	ns	max
TELQX	$\overline{\text{CS}}$ low to low Z	5	5	5	5	ns	min
TEHQZ	$\overline{\text{CS}}$ high to high Z	12	15	20	20	ns	max
TELIC	$\overline{\text{CS}}$ low to power up	0	0	0	0	ns	min
TEHICL	$\overline{\text{CS}}$ high to power down	20	20	25	25	ns	max
TGLQV	Output enable access time	15	15	20	25	ns	max
TGLQX	$\overline{\text{OE}}$ low to low Z	0	0	0	0	ns	min
TGHQZ	$\overline{\text{OE}}$ high to high Z	12	15	15	20	ns	max

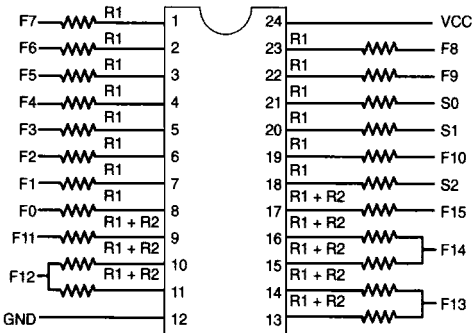
READ CYCLE nb 1



READ CYCLE nb 2



BURN-IN SCHEMATICS


 $R1 = 220 \Omega$ per row

 $R2 = 2.2 K \Omega$ per driver

 $FO = 50 KHz \pm 20 \%$
 $F_n = 1/2 F_{n-1}$
 $S0, S1, S2$: programmable signals
for write/read cycles

 $VCC = 5.5 V$

ORDERING INFORMATION

HM	PACKAGE	—	DEVICE TYPE	GRADE	LEVEL
HM	3	—	65728B	H	— 5 : R
			2 k x 8 high speed static RAM		
	0 - Chip form			H = 25 ns	- 2 : Military
	1 - Ceramic 24 pins			K = 35 ns	- 5 : Commercial
	3 - Plastic 24 pins			M = 45 ns	- 6 : 100% 25°C Probe
	300 mils			N = 55 ns	/883 : MIL STD 883 Class B or S
	3E - Plastic 24 pins				DB : Dice Military program
	600 mils				R : Tape & Reel option
	4 - LCC 32 pins				RD : Tape & Reel / Dry pack option
	T - SOIC 24 pins 300 mils				D : Dry pack option

