AUG 16 1993

Preliminary Data Sheet
July 1993

AT&T Microelectronics

Fibre Channel Receiver and Transmitter Integrated Circuits ATTDA204A/ATTDA205A

Features

- Operationally compliant with the Fibre Channel Standard X3T9.3, providing FC-0 and FC-1 services at 1.0625 Gbits/s
- Total power dissipation of 2.85 W for the receiver and 1.75 W for the transmitter with a single 5.0 V supply
- Novel PLL design requires no external components for the clock recovery and frequency synthesis
- User-enabled 8B/10B encode/decode circuitry on-chip
- On-chip 75 Ω termination resistors at receiver inputs, and built-in 270 Ω pull-down resistors on transmitter outputs
- PECL high-speed interface I/O for use with optical transceiver or 75 Ω coaxial copper media
- User-enabled 17- or 20-bit parallel TTL interface

Description

The ATTDA204A and ATTDA205A Fibre Channel receiver and transmitter integrated circuits provide for data transmission over fiber or coaxial media at 1.0625 Gbits/s. Both devices are available in plastic 80-pin PQFP packages.

The ATTDA204A receives high-speed serial data at its differential ECL input port. This data is fed to the clock recovery section which generates a recovered clock and retimes the data. The retimed data is deserialized and word aligned before being sent to the decoder. Here, data is either 8B/10B decoded (user's option) or passed straight through to the TTL parallel output port. A divided-down version of the recovered clock, synchronous with the parallel data bytes, is also available as a TTL output.

The ATTDA205A accepts TTL data at the parallel input port. It also accepts the low-speed TTL system clock and uses this clock to synthesize the internal high-speed serial bit clock. Parallel data is optionally 8B/10B encoded (user's choice) and then serialized using the synthesized high-speed clock. The serialized data is then made available at the differential ECL output to drive either an optical transmitter or 75 Ω coaxial copper media.

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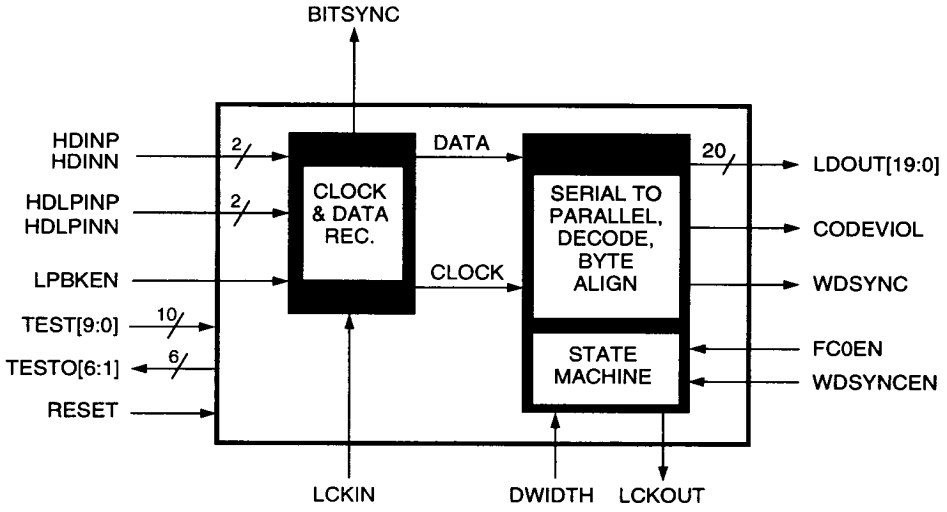
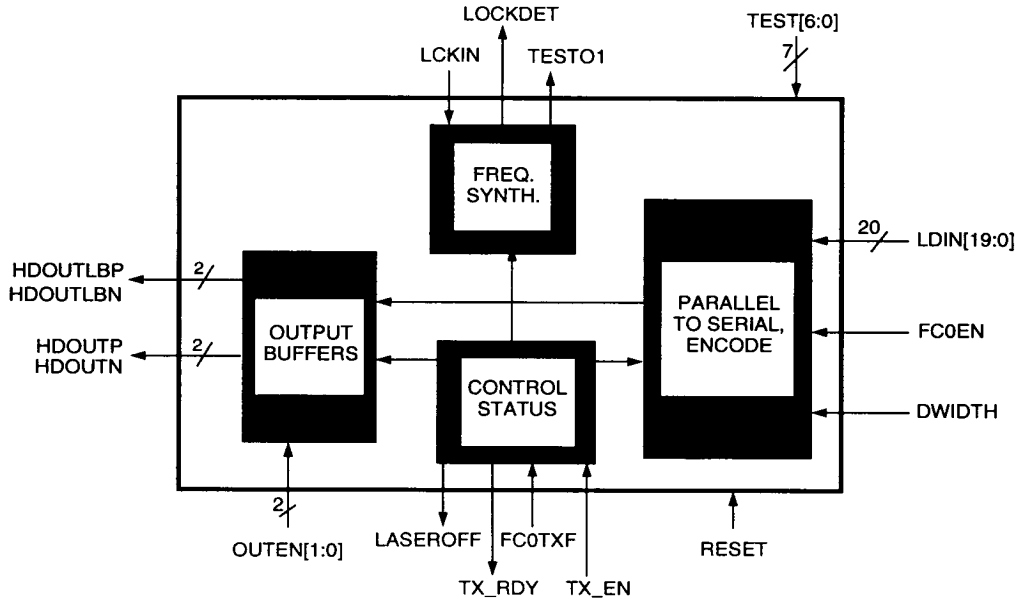
Description (continued)



A. ATTDA204A-Receiver IC



B. ATTDA205A-Transmitter IC

Figure 1. Fibre Channel Receiver and Transmitter IC Functional Diagrams

Pin Information

Table 1. ATTDA204A Receiver Pin Descriptions (See Table 3 for data-byte bit definitions.)

Pin	Name	I/O	Level	Description
1, 5, 9, 13, 17	QGND	—	—	Quiet ground.
2	TEST1	I	TTL	Test input. Tie to ground for normal operation.
3, 7, 11, 15, 80	QVcc	—	—	+5 V quiet supply.

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Pin Information (continued)

Table 1. ATTDA204A Receiver Pin Descriptions (continued) (See Table 3 for data-byte bit definitions.)

Pin	Name	I/O	Level	Description
4	TEST2	I	TTL	Test input. Tie to ground for normal operation.
6	TEST3	I	TTL	Test input. Tie to ground for normal operation.
8	TEST4	I	TTL	Test input. Tie to ground for normal operation.
10	TESTO1	O	TTL	Test output. Open circuit for normal operation.
12	TESTO2	O	TTL	Test output. Open circuit for normal operation.
14	TEST5	I	TTL	Test input. Tie to ground for normal operation.
16	LCKIN	I	TTL	Low-speed reference clock. For 1.0625 Gbits/s operation. LCKIN frequency should be 53.125 MHz.
18, 24, 30, 40	NVcc	—	—	+5 V supply for TTL I/O.
19	LDOUT19	O	TTL	j1 (MSB for undecoded high data byte).
20	LDOUT18	O	TTL	h1 (for undecoded high data byte).
21, 25, 35, 41	NGND	—	—	Ground for TTL I/O.
22	LDOUT17	O	TTL	H1 (MSB for decoded high data byte) or g1.
23	LDOUT16	O	TTL	G1 or f1 (high data byte).
26	LDOUT15	O	TTL	F1 or i1 (high data byte).
27	LDOUT14	O	TTL	E1 or e1 (high data byte).
28	LDOUT13	O	TTL	D1 or d1 (high data byte).
29	LDOUT12	O	TTL	C1 or c1 (high data byte).
31	LDOUT11	O	TTL	B1 or b1 (high data byte).
32	LDOUT10	O	TTL	A1 or a1 (LSB for high data byte).
33	LDOUT9	O	TTL	j0 (MSB for undecoded low data byte).
34	LDOUT8	O	TTL	K or h0 (low data byte).
36	LDOUT7	O	TTL	H0 (MSB for decoded low data byte) or g0.
37	LDOUT6	O	TTL	G0 or f0 (low data byte).
38	LDOUT5	O	TTL	F0 or i0 (low data byte).
39	LDOUT4	O	TTL	E0 or e0 (low data byte).
42	LDOUT3	O	TTL	D0 or d0 (low data byte).
43	LDOUT2	O	TTL	C0 or c0 (low data byte).
44, 49, 55, 61, 65, 73	Vcc	—	—	+5 V supply.
45	LDOUT1	O	TTL	B0 or b0 (low data byte).
46	LDOUT0	O	TTL	A0 or a0 (LSB for low data byte).
47, 50, 58, 64	GND	—	—	Ground.
48	LCKOUT	O	TTL	Low-speed clock out.
51	DWIDTH	I	TTL	Tie to ground for normal operation.
52	WDSYNC	O	TTL	When WDSYNC = 1, the receiver has achieved word sync.
53	WDSYNCEN	I	TTL	Enable byte alignment when WDSYNCEN = 1.
54	FC0EN	I	TTL	8B/10B decoder disabled when FC0EN = 1. 8B/10B decoder enabled when FC0EN = 0.
56	TESTO3	O	ECL	Test output. Tie to Vcc for normal operation.
57	TESTO4	O	ECL	Test output. Tie to Vcc for normal operation.
59	TEST6	I	ECL	Test input. Tie to Vcc for normal operation.
60	TEST7	I	ECL	Test input. Tie to Vcc for normal operation.

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Pin Information (continued)

Table 1. ATTDA204A Receiver Pin Descriptions (continued) (See Table 3 for data-byte bit definitions.)

Pin	Name	I/O	Level	Description
62	CODEVIOL	O	TTL	CODEVIOL = 1 when 8B/10B code violation observed.
63	BITSYNC	O	TTL	BITSYNC = 0 when bit sync achieved.
66	TESTO5	O	ECL	Test output. Tie to Vcc for normal operation.
67	TESTO6	O	ECL	Test output. Tie to Vcc for normal operation.
68	TEST8	I	TTL	Test input. Tie to ground for normal operation.
69	TEST9	I	TTL	Test input. Tie to ground for normal operation.
70	HDINP	I	ECL	High-speed input data (+).
71	HDINC	—	—	75 Ω termination common node.
72	HDINN	I	ECL	High-speed input data (–).
74	HDLPINP	I	ECL	Loopback input data (+).
75	HDLPINC	—	—	75 Ω termination common node.
76	HDLPINN	I	ECL	Loopback input data (–).
77	LPBKEN	I	TTL	Loopback enabled when LPBKEN = 1.
78	TEST0	I	TTL	Test input. Tie to ground for normal operation.
79	RESET	I	TTL	Master reset, active-high.

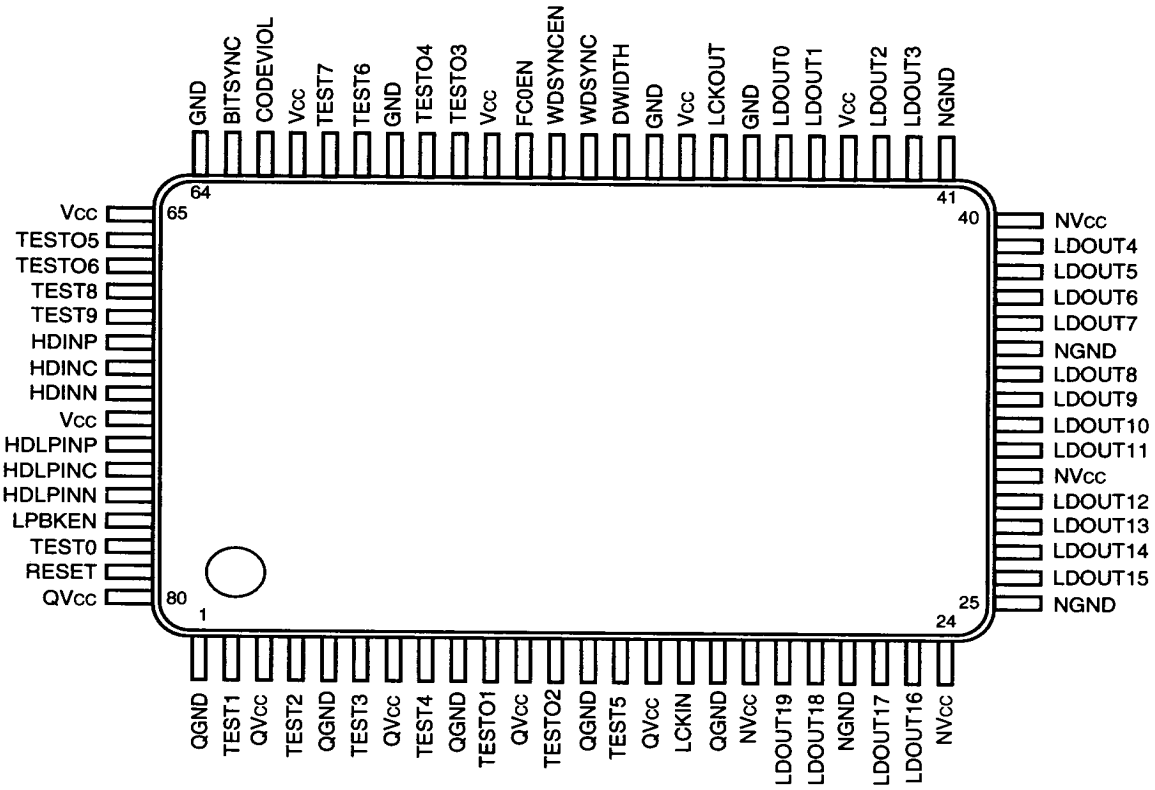

Figure 2. ATTDA204A Receiver Pin Diagram

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Pin Information (continued)

Table 2. ATTDA205A Transmitter Pin Descriptions (See Table 3 for data-byte bit definitions.)

Pin	Name	I/O	Level	Description
1, 8, 12, 15, 68, 70, 73, 76, 80	GND	—	—	Ground.
2	TEST4	I	TTL	Test input. Tie to ground for normal operation.
3	TEST5	I	TTL	Test input. Tie to ground for normal operation.
4, 10, 13, 69, 77	Vcc	—	—	+5 V supply.
5	FC0EN	I	TTL	8B/10B encoder disabled when FC0EN = 1. 8B/10B encoder enabled when FC0EN = 0.
6	OUTEN1	I	TTL	HDOUTLBP, HDOUTLBN outputs enabled when OUTEN1 = 1. HDOUTLBP, HDOUTLBN outputs disabled when OUTEN1 = 0.
7	OUTEN0	I	TTL	HDOUTP, HDOUTN outputs enabled when OUTEN0 = 1. HDOUTP, HDOUTN outputs disabled when OUTEN0 = 0.
9	DWIDTH	I	TTL	Tie to ground for normal operation.
11	TEST6	I	TTL	Test input. Tie to ground for normal operation.
14	TEST3	I	TTL	Test input. Use as data pattern generator as follows: FC0EN TEST3 Output Data 0 0 Encoded Data 1 0 Unencoded Data 0 1 101010. . . 1 1 11111000001111100000. . .
16, 20, 24, 29, 36, 41, 48, 52	NVcc	—	—	+5 V supply for TTL I/O.
17	LDIN0	I	TTL	A0 or a0 (LSB for low data byte).
18, 22, 25, 33, 40, 45, 50	NGND	—	—	Ground for TTL I/O.
19	LDIN1	I	TTL	B0 or b0 (low data byte).
21	LDIN2	I	TTL	C0 or c0 (low data byte).
23	LDIN3	I	TTL	D0 or d0 (low data byte).
26	LDIN4	I	TTL	E0 or e0 (low data byte).
27	LDIN5	I	TTL	F0 or i0 (low data byte).
28	LDIN6	I	TTL	G0 or f0 (low data byte).
30	LDIN7	I	TTL	H0 (MSB for encoded low data byte) or g0.
31	LDIN8	I	TTL	K or h0 (low data byte).
32	LDIN9	I	TTL	j0 (MSB for unencoded low data byte).
34	LDIN10	I	TTL	A1 or a1 (LSB for high data byte).
35	LDIN11	I	TTL	B1 or b1 (high data byte).
37	LDIN12	I	TTL	C1 or c1 (high data byte).
38	LDIN13	I	TTL	D1 or d1 (high data byte).
39	LDIN14	I	TTL	E1 or e1 (high data byte).
42	LDIN15	I	TTL	F1 or i1 (high data byte).
43	LDIN16	I	TTL	G1 or f1 (high data byte).
44	LDIN17	I	TTL	H1 (MSB for encoded high data byte) or g1.
46	LDIN18	I	TTL	h1 (high data byte).
47	LDIN19	I	TTL	j1 (MSB for unencoded high data byte).
49	TESTO1	O	TTL	Test output. Open circuit for normal operation.

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Pin Information (continued)

Table 2. ATTDA205A Transmitter Pin Descriptions (continued) (See Table 3 for data-byte bit definitions.)

Pin	Name	I/O	Level	Description
51	LCKIN	I	TTL	Low-speed reference clock. For 1.0625 Gbits/s operation LCKIN frequency should be 53.125 MHz.
53	TX_RDY	O	TTL	1 = transmitter ready to transmit data.
54, 58, 64	QVcc	—	—	+5 V quiet supply.
55	LOCKDET	O	TTL	1 = synthesizer locked. 0 = synthesizer not locked.
56, 61, 65	QGND	—	—	Quiet ground.
57	TEST2	I	TTL	Test input. Tie to ground for normal operation.
59	TX_EN	I	TTL	Transmitter enabled when TX_EN = 1. Transmitter disabled when TX_EN = 0.
60	RESET	I	TTL	Master reset, active-high.
62	TEST1	I	TTL	Test input. Tie to ground for normal operation.
63	TEST0	I	TTL	Test input. Tie to ground for normal operation.
66	—	—	—	NC. Do not connect to this pin.
67	—	—	—	NC. Do not connect to this pin.
71	HDOUTLBN	O	ECL	Loopback data out(–).
72	HDOUTLBP	O	ECL	Loopback data out(+).
74	HDOUTN	O	ECL	Data out(–).
75	HDOUTP	O	ECL	Data out(+).
78	LASEROFF	O	TTL	1 = disable optical TX. 0 = enable optical TX.
79	FC0TXF	I	TTL	See Table 5.

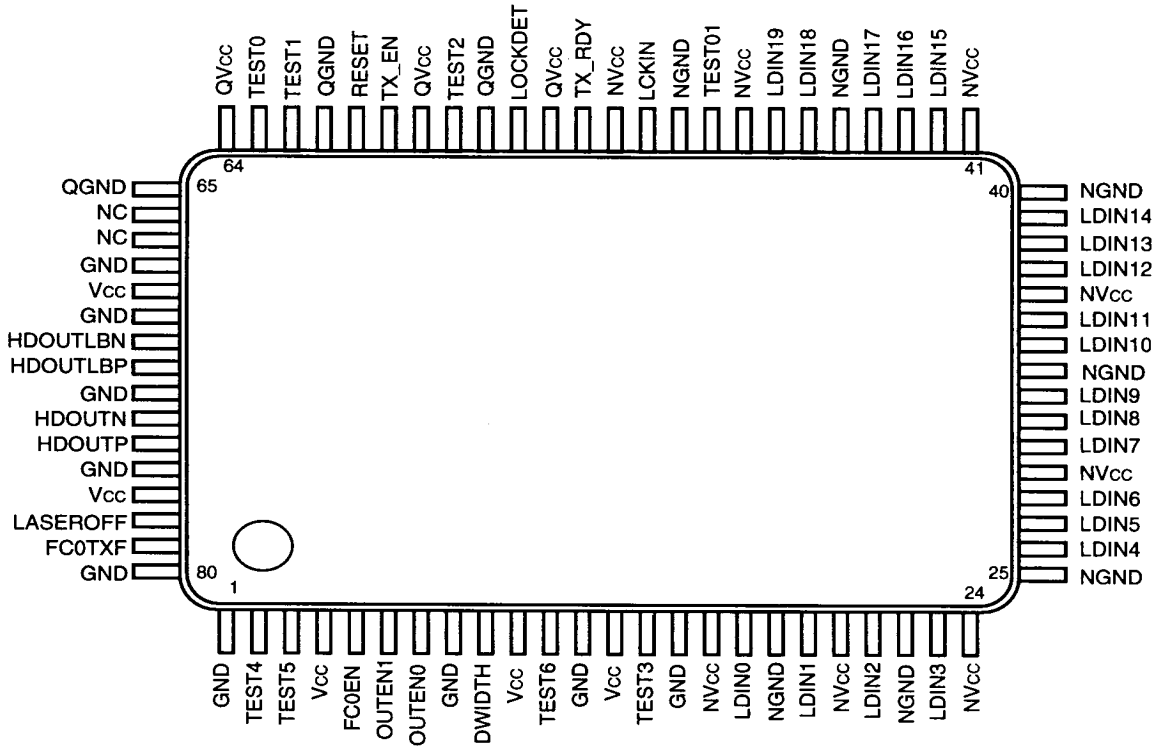

Figure 3. ATTDA205A Transmitter Pin Diagram

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Pin Information (continued)

Table 3. Data-Byte Bit Definitions

Encoding/Decoding Enabled																				
	High Byte										Low Byte									
			MSB							LSB			MSB							LSB
Bit Name			H1	G1	F1	E1	D1	C1	B1	A1		K	H0	G0	F0	E0	D0	C0	B0	A0
ANSI Name			H	G	F	E	D	C	B	A		Z	H	G	F	E	D	C	B	A
Encoding/Decoding Disabled																				
	High Byte										Low Byte									
	MSB									LSB	MSB									LSB
Bit Name	j1	h1	g1	f1	i1	e1	d1	c1	b1	a1	j0	h0	g0	f0	i0	e0	d0	c0	b0	a0
ANSI Name	j	h	g	f	i	e	d	c	b	a	j	h	g	f	i	e	d	c	b	a
Pin Numbers																				
DA204	19	20	22	23	26	27	28	29	31	32	33	34	36	37	38	39	42	43	45	46
DA205	47	46	44	43	42	39	38	37	35	34	32	31	30	28	27	26	23	21	19	17

Functional Description

Receiver ATTDA204A

Data input to the receiver is on differential ECL levels, and on-chip 75 Ω termination resistors are connected as shown in Figure 4.

Figure 4. On-Chip Input Termination Resistors

The termination resistor common nodes, HDINC and HDLPINC, can be left floating for a 150 Ω differential termination, or they can be tied to Vcc – 2 V, providing two independent 75 Ω terminations. For ac-coupled inputs, the common nodes should be biased to Vcc – 1.3 V.

A selector pin LBPKEN selects between two possible sets of inputs: normal data (HDINP, HDINN) or loopback data (HDLPINP, HDLPINN). The selected data is directed to the clock recovery section where clock is recovered and data is resynchronized to the recovered clock. Retimed data and clock now go to the serial-to-parallel converter where byte alignment is performed. External control signals and received data patterns serve to place the receiver into a number of operating states. These states and their transition criteria are shown in Figure 5 and described below.

When alignment has been achieved, data is optionally sent to the 8B/10B decoder and then to the output buffer which drives a 17-bit wide TTL output bus (see Table 3). If the user does not select this decoding, data goes directly to the output buffer section where it is demuxed to a 20-bit wide TTL output bus. In both modes, a 53.125 MHz clock, synchronous with the parallel data, is available as a TTL output. Timing for the parallel port is shown in Figure 7.

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Functional Description (continued)

Receiver ATTDA204A (continued)

Receiver Start-Up

To initialize the receiver, a RESET pulse is normally applied after powerup, but RESET can be applied at any time in any state. Once applied, RESET will place the receiver into the Not Operational state. To initiate the word and byte sync alignment, a WDSYNCEN pulse must be asserted. This causes the receiver to go into the Loss-of-Synchronization state as shown in Figure 5, and WDSYNC will go low. Note that WDSYNCEN should be a pulse. Simply leaving WDSYNCEN asserted high forces the receiver to stay in state f, as shown in Figure 5. If the receiver successfully achieves byte and word alignment, the receiver goes into the Synchronization-Acquired state and WDSYNC goes high.

Byte Alignment

When WDSYNCEN is asserted, the receiver starts looking for ordered sets (any word containing four valid characters and beginning with a comma), and begins byte synchronization on detection of the first comma. At that time, the 53.125 MHz clock LCKOUT will be synchronized with the byte beginning with a comma, and approximately 1.5 (low frequency) clock cycles later (see Figure 6), the LDOUT8 pin will be asserted high. Upon receipt of the third valid ordered set, WDSYNC will be set high, and the chip will enter the Synchronization-Acquired state. There are four substates within the Synchronization-Acquired state, and these are described below and illustrated in Figure 5.

The ATTDA204 Receiver can be operated in modes that are not strictly compliant with the Fibre Channel standard; however, the sequence for byte alignment is the same. WDSYNCEN must be pulsed for alignment to begin, and alignment will occur on receipt of any comma until the receiver goes into the Synchronization-Acquired state. Once in the Synchronization-Acquired state, byte alignment is disabled.

STATES:
SYNCHRONIZATION-ACQUIRED (SUB-STATES a, b, c, d)
LOSS-OF-SYNCHRONIZATION (SUB-STATES e, f, g, h)
NOT OPERATIONAL

TRANSITION VARIABLES:
EN = WDSYNCEN ASSERTED
D = ANY DATA
CV = CODE VIOLATION
VW = VALID WORDS
2VW = 2 CONSECUTIVE VALID WORDS
$\overline{OS}$ = ORDERED SET
OS = ANY DATA EXCEPT OS
R = RESET

OUTPUT VARIABLE:
WDSYNC

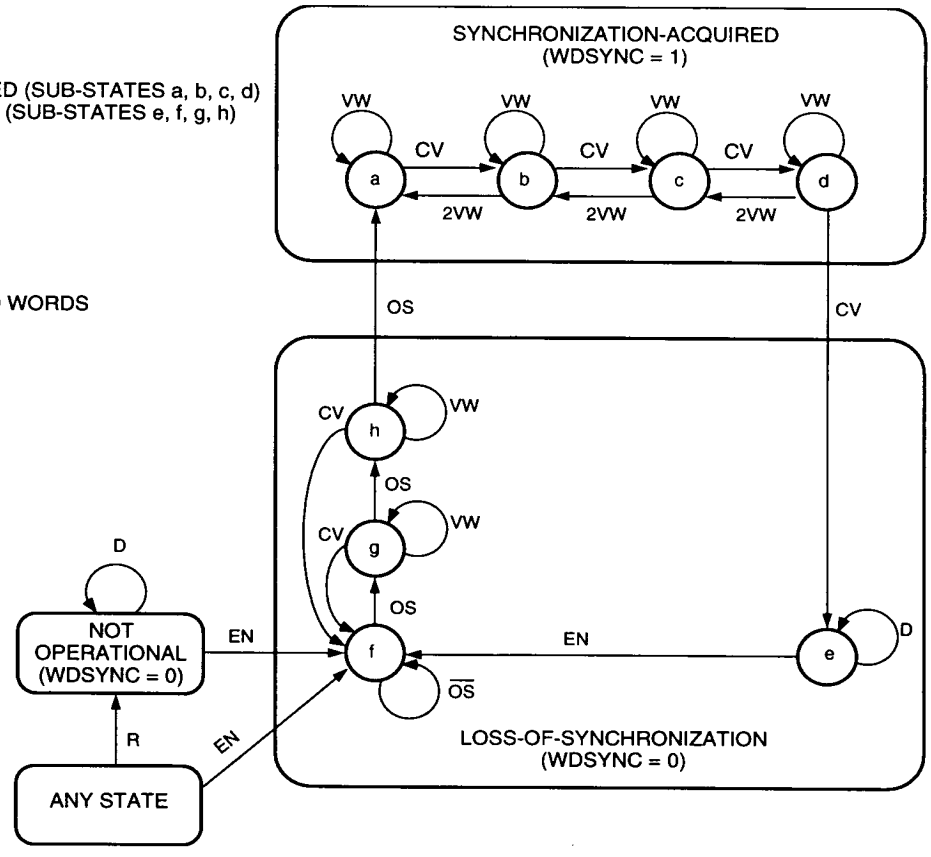

Figure 5. Receiver State Diagram

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Functional Description (continued)

Receiver ATTDA204A (continued)

Synchronization-Acquired State

In this state, words are checked for any code violations. Figure 5 details the criteria for entering and exiting this state. The requirement for entering this state is always the reception of three valid ordered sets. Once in this state, the minimum criterion for exiting is four consecutive code violations. Other combinations of valid words and code violations will also lead to exiting the Synchronization-Acquired state, and these are shown in Figure 5.

Clock Recovery

The clock recovery section, which recovers clock from the data input, requires a 53.125 MHz ± 100 ppm reference clock which regulates the capture range of the oscillator. Phase comparison between data and regenerated clock occurs only on the positive-going data edge. This means that data pulse-width distortion will not affect the clock recovery performance.

When the recovered clock has locked onto the incoming data transitions, BITSYNC = 0 provides an indication that bit synchronization has been achieved. The BITSYNC flag, however, is not a precise measure of clock acquisition and has no direct effect on any state machines. In the absence of data transitions (e.g., no input signal), the BITSYNC flag has no meaning.

Transmitter ATTDA205A

In normal operation, the transmitter takes in parallel data from the parallel port, optionally encodes that data, and converts it to a serial data stream at 1.0625 Gbits/s. A 53.125 MHz ± 100 ppm reference clock is also required for this chip, and this reference is used to generate the 1.0625 GHz internal clock, read in data from the parallel port, and generate specific test patterns.

Reset and Lock Detector

Normally, a reset is not necessary for correct operation of the ATTDA205A, but in some cases, applying a RESET pulse might help ensure rapid and correct locking of the 1.0625 GHz synthesizer. If the synthesizer is not locked properly, the LOCKDET output will go to a logic 0. The reset and lock detector functions are described in Table 4.

Table 4. Transmitter Reset and Lock Detect Functions

Condition		Outputs			
RESET	LOCKDET	TX_RDY	LASEROFF	HDOUT	HDOUTLB
1	0	0	1	0	0
0	0	0	1	0	0
0	1	Table 5	Table 5	Table 5	Table 5
1	1	Operation not defined for this condition			

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Functional Description (continued)

Transmitter ATTDA205A (continued)

Serial Output Port

There are two equivalent differential ECL outputs which are enabled by two control signals. The HDOUTP, HDOUTN pair is enabled by OUTEN0 (enabled = 1), and the HDOUTLBP, HDOUTLBN pair is enabled by OUTEN1 (enabled = 1). The deselected output always sources a differential logic 0. OUTEN0 and OUTEN1 should never be enabled at the same time. These enable signals also interact with the laser output control signals as described below and in Table 5. Drive capability on these outputs allows the chip to drive either 50 Ω or 75 Ω loads terminated to Vcc – 2 V. On-chip 270 Ω resistors are connected from each output to GND.

Parallel Input Port

Parallel port input data can either be 8B/10B encoded (FC0EN = 0) on a 17-bit bus (see Table 3) or unencoded (FC0EN = 1) on a 20-bit bus. Timing for the parallel input data and the 53.125 MHz reference clock is shown in Figure 9.

Laser Output Control

The data transmit functions described in the following paragraphs are also shown in Table 5. Once LOCKDET goes high, TX_EN can be asserted high to enable the selected differential ECL output. If OUTEN0 is asserted high (OUTEN1 must = 0) and FC0TXF = 0, within one low-speed clock cycle, TX_RDY will go high and the HDOUTP, HDOUTN pair will start sourcing normal data. If either TX_EN or LOCKDET goes low or FC0TXF goes high, then HDOUTP is forced low and HDOUTN is forced high in order to shut down the laser output. If the laser shutdown condition occurs, then the flag, LASEROFF, goes high and the TX_RDY goes low.

If OUTEN1 is asserted high (OUTEN0 must = 0) while LOCKDET and TX_EN = 1 and FC0TXF = 0, then the TX_RDY flag will go high and normal data will be sourced from the HDOUTLBP, HDOUTLBN pair. If either TX_EN or LOCKDET goes low while FC0TXF = 0, then TX_RDY goes low, and the HDOUTLBP, HDOUTLBN pair will source a differential logic low.

Under the special condition where LOCKDET and TX_EN = 1, while FC0TXF = 1 and OUTEN1 = 1, the HDOUTP, HDOUTN pair will start sourcing 10101010. . . data. This can help certain laser transmitters to initialize more rapidly. Under this mode of operation, TX_RDY will be a logic low.

Test Pattern Generator

Asserting TEST3 = 1 allows built-in generators in the ATTDA205A to source test patterns onto the serial output. If FC0EN = 0, the pattern is 10101010. . ., and if FC0EN = 1, the pattern is 11111000001111100000. . . . For normal operation, TEST3 = 0. These test pattern modes are illustrated in Table 6.

Table 5. Transmitter Data Transmit Operation (LOCKDET = 1, RESET = 0, TEST3 = 0)

Inputs				Outputs			
TX_EN	FC0TXF	OUTEN0	OUTEN1	TX_RDY	LASEROFF	HDOUT	HDOUTLB
1	0	1	0	1	0	Data	0
1	0	0	1	1	0	0	Data
0	X	X	X	0	1	0	0
X	X	0	0	0	1	0	0
1	1	1	0	0	0	1010. . .	0
X	X	1	1	Operation not defined for this condition			

Table 6. Transmitter Data Test Pattern Operation (LOCKDET = 1, RESET = 0, TX_EN = 1, FC0TXF = 0, TEST3 = 1)

Inputs			Outputs*	
OUTEN0	OUTEN1	FC0EN	HDOUT	HDOUTLB
1	0	0	101010. . .	0
1	0	1	1111100000. . .	0
0	1	0	0	101010. . .
0	1	1	0	1111100000. . .
1	1	X	Operation not defined for this condition	

* For all valid states in this table, the LASEROFF = 0, TX_RDY = 1 condition will be true. This means that the transmitter is working normally to source data (as per Table 5), but the data is now one of two test patterns.

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Absolute Maximum Ratings

Stresses in excess of the Absolute Maximum Ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to Absolute Maximum Ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min	Max	Unit
Power Supply Voltage	V_{CC}	—	7.0	V
Ambient Operating Temperature	T_A	0	70	°C
Storage Temperature	T_{stg}	–40	125	°C

Handling Precautions

CAUTION: This device is susceptible to damage as a result of electrostatic discharge. Take proper precautions during both handling and testing. Follow guidelines such as JEDEC Publication No. 108-A (Dec. 1988).

Although protection circuitry is designed into the device, take proper precautions to avoid exposure to ESD.

AT&T employs a human-body model (HBM) for ESD-susceptibility testing and protection design evaluation. ESD voltage thresholds are dependent on the critical parameters used to define the model. A standard HBM (resistance = 1.5 kΩ, capacitance = 100 pF) is widely used and, therefore, can be used for comparison purposes. The HBM ESD threshold presented here was obtained by using these circuit parameters.

Table 7. Human-Body Model ESD Threshold

Device	Value	Unit
ATTDA204A	>1000	V
ATTDA205A	>1000	V

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Electrical Characteristics

T_A = 0 °C to 70 °C

Table 8. ATTDA204A Receiver dc Electrical Characteristics

Parameter	Symbol	Conditions	Min	Max	Units
+5 V Supplies	V_{CC}, QV_{CC}, NV_{CC}	—	4.75	5.25	V
Power Supply Current	I_{CC}*	V_{CC} = max	437	600	mA
TTL Output Voltage					
Low	V_{OL}	I = 4 mA	—	0.4	V
High	V_{OH}	I = –400 µA	2.4	—	V
TTL Input Voltage					
Low	V_{IL}	—	—	0.8	V
High	V_{IH}	—	2	—	V
TTL Input Current					
Low	I_{IL}	V_{IN} = 0.4 V	—	–400	µA
High	I_{IH}	V_{IN} = 2.7 V	—	20	µA
Differential PECL Input Voltage	V_{DIFF}	—	200	—	mV
PECL Common Mode Bias†	V_{COM}	—	V_{CC} – 1.6	V_{CC} – 1.0	V
PECL Terminating Resistor	R_{TERM}	—	67.0	84.0	Ω

* Does not include current delivered to external loads.
† PECL Common Mode Bias is the dc average of the input signal voltage.

Table 9. ATTDA205A Transmitter dc Electrical Characteristics

Parameter	Symbol	Conditions	Min	Max	Units
+5 V Supplies	V_{CC}, QV_{CC}, NV_{CC}	—	4.75	5.25	V
Power Supply Current	I_{CC}*	V_{CC} = max	245	354	mA
TTL Output Voltage					
Low	V_{OL}	I = 4 mA	—	0.4	V
High	V_{OH}	I = –400 µA	2.4	—	V
TTL Input Voltage					
Low	V_{IL}	—	—	0.8	V
High	V_{IH}	—	2	—	V
TTL Input Current					
Low	I_{IL}	V_{IN} = 0.4 V	—	–400	µA
High	I_{IH}	V_{IN} = 2.7 V	—	20	µA
ECL Output Voltage					
Low	V_{OL}	†	V_{CC} – 1.81	V_{CC} – 1.62	V
High	V_{OH}	†	V_{CC} – 1.02	V_{CC} – 0.88	V

* Does not include current delivered to external loads.
† Driving 50 Ω terminated to V_{CC} – 2 V.

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Timing Characteristics

Receiver ATTDA204A

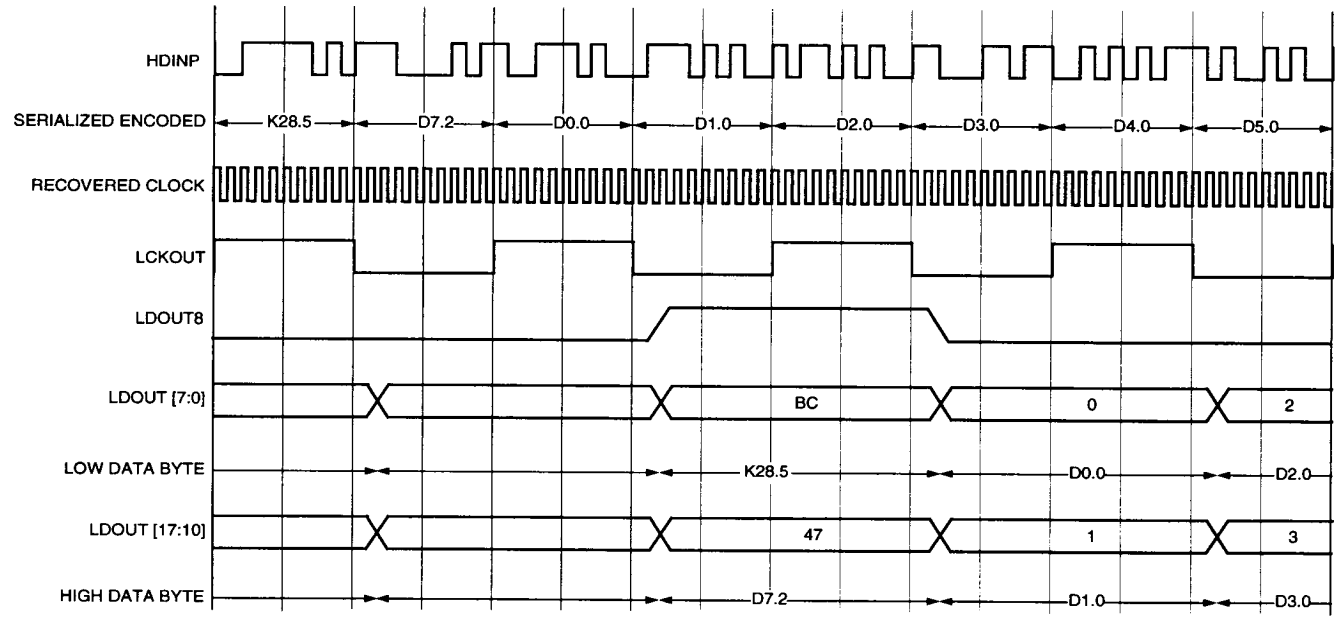

Figure 6. ATTDA204A Receiver IC Timing

Table 10. ATTDA204A Receiver Timing

Symbol	Parameter	Min	Max	Units
tCKLCKL	LCKOUT Period	18.822	18.825	ns
tCKLCKH	LCKOUT Low	7.0	11.8	ns
tCKHCKL	LCKOUT High	7.0	11.8	ns
tCKLDOV	LCKOUT to DO Valid	0	3.0	ns
tRHRL	RESET Pulse Width High	20	—	ns
tSYHSYL	WDSYNCEN High	20	—	ns
tINLINL	LCKIN Period	18.73	18.92	ns

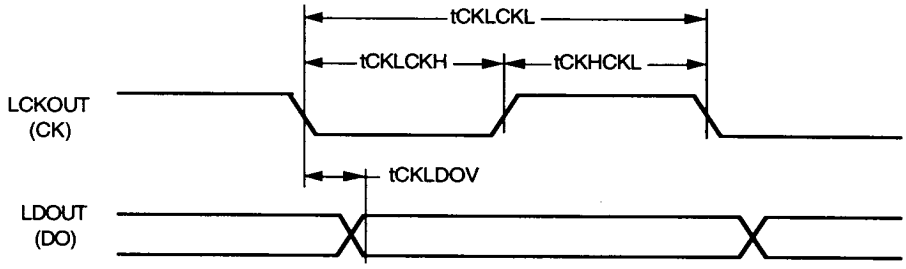

Figure 7. Receiver Port Timing

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Timing Characteristics (continued)

Transmitter ATTDA205A

53.125 MHz Reference Clock

The quality of the jitter and frequency accuracy of this clock will directly affect the quality of the output data signal. Internally, the ATTDA205A synthesizer has a 400 kHz natural frequency to aid in rejecting jitter components above that frequency.

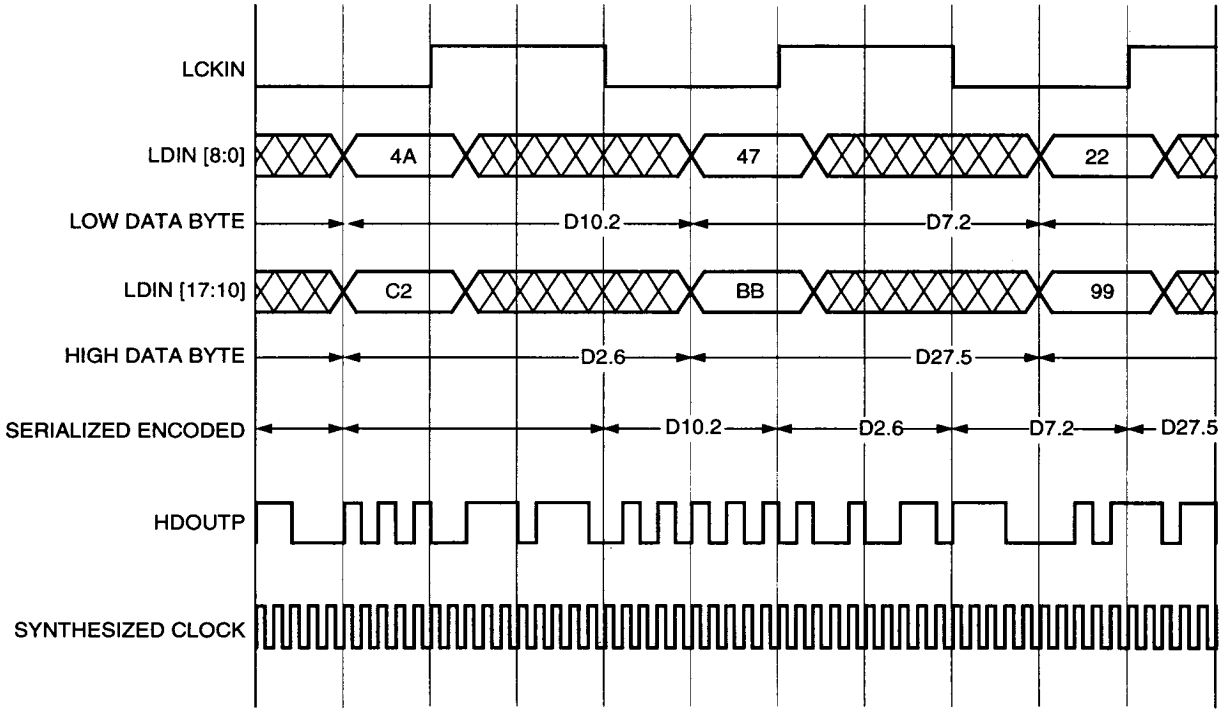

Figure 8. ATTDA205A Transmitter IC Timing

Table 11. ATTDA205A Transmitter Timing

Symbol	Parameter	Min	Max	Units
tLKHDIX	Data In Hold	3.0	—	ns
tDIVLKH	Data In Setup	3.0	—	ns
tRHRL	RESET Pulse Width High	20	—	ns
tINHINH	LCKIN Period	18.882	18.825	ns

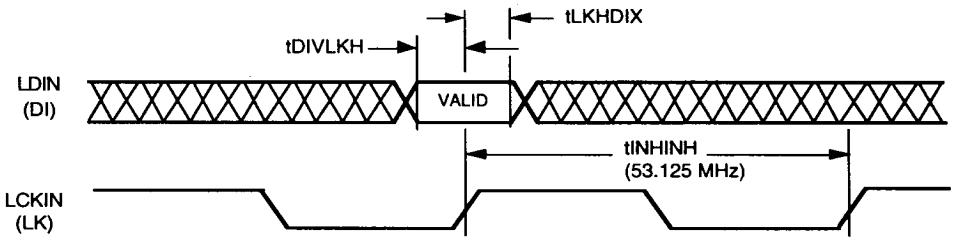

Figure 9. Transmitter Port Timing

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Noise and Jitter Characteristics

Receiver ATTDA204A

Table 12. Clock Recovery Characteristics

Parameter	Min	Max	Units
Noise Factor*	—	1	dB

* Optical power penalty due to retiming jitter and static alignment error.

Transmitter ATTDA205A

Table 13. Transmitter Output Jitter

Parameter	Min	Max	Units
Deterministic Jitter	—	0.08	UI p-p
Random Jitter	—	0.12	UI p-p
Total Jitter	—	0.20	UI p-p

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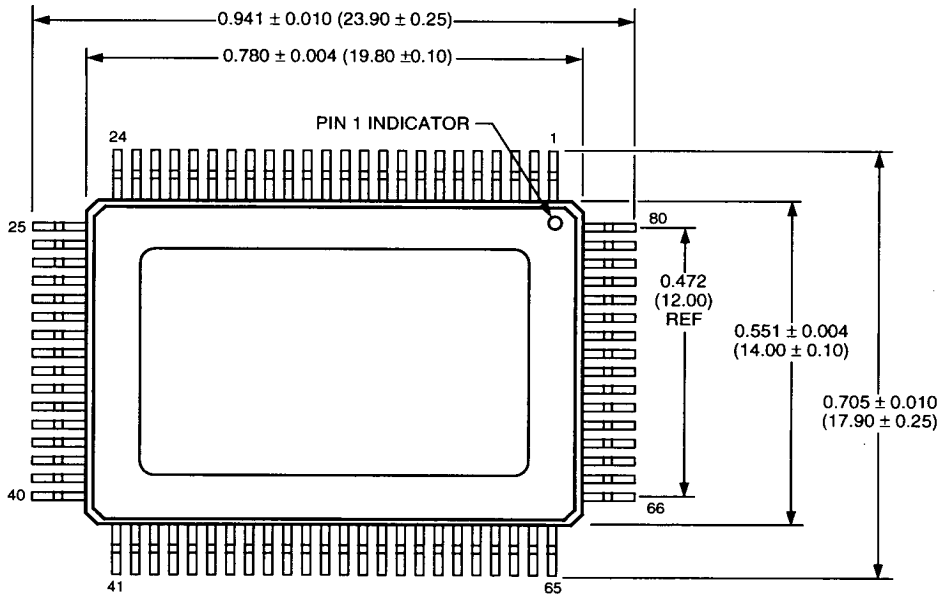
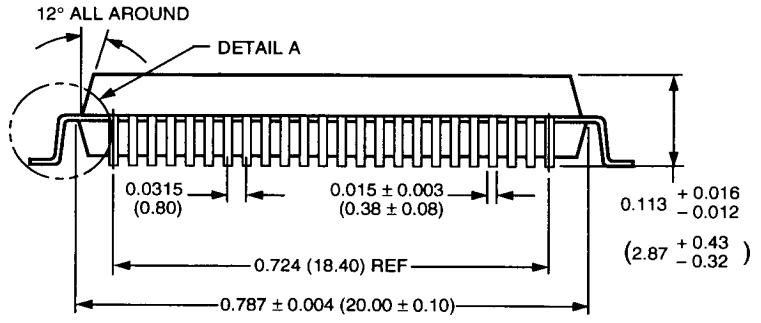
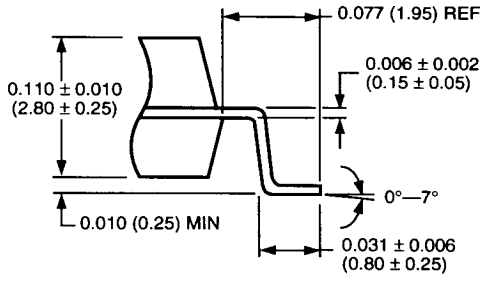
Outline Diagram

Dimensions are in inches and (millimeters). Package outline meets EIAJ registered outline.

80-Pin, Heat Spreader PQFP Package







DETAIL A

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Ordering Information

Table 14. Fibre Channel Receiver

Code	Package	Temperature	Order Code	Shipping Method
ATTDA204AHG	80-Pin PQFP	0 °C to 70 °C	106786718	Bakeable Tray (Dry Pack)
ATTDA204ABE	Die	0 °C to 70 °C	106725161	—

Table 15. Fibre Channel Transmitter

Code	Package	Temperature	Order Code	Shipping Method
ATTDA205AHG	80-Pin PQFP	0 °C to 70 °C	106786726	Bakeable Tray (Dry Pack)
ATTDA205ABE	Die	0 °C to 70 °C	106725179	—

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Tel. (65) 778-8833, FAX (65) 777-7495

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July 1993
DS93-132DBIP (Replaces DS92-178DBIP)

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