



N-Channel 40-V (D-S) MOSFET

PRODUCT SUMMARY

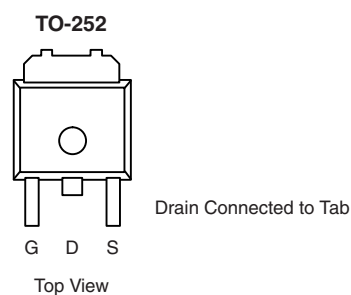
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A) ^a	Q_g (Typ.)
40	0.037 at $V_{GS} = 10$ V	8	5.3 nC
	0.046 at $V_{GS} = 4.5$ V	8	

FEATURES

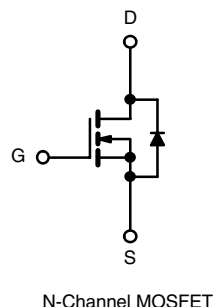
- TrenchFET[®] Power MOSFET
- 100 % UIS Tested

APPLICATIONS

- Backlight Inverter for LCD Display
- Full Bridge DC/DC Converter

RoHS
COMPLIANT

Ordering Information:
SUD50N04-37P-E3 (Lead (Pb)-free)



ABSOLUTE MAXIMUM RATINGS $T_A = 25$ °C, unless otherwise noted				
Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	40	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current ($T_J = 150$ °C)	$T_C = 25$ °C	I_D	8 ^a	A
	$T_C = 70$ °C		8 ^a	
	$T_A = 25$ °C		5.4 ^b	
	$T_A = 70$ °C		4.4 ^b	
Pulsed Drain Current		I_{DM}	30	
Continuous Source-Drain Diode Current	$T_C = 25$ °C	I_S	8 ^a	
	$T_A = 25$ °C		1.6 ^b	
Single Pulse Avalanche Current	L = 0.1 mH	I_{AS}	7	mJ
Avalanche Energy		E_{AS}	2.45	
Maximum Power Dissipation	$T_C = 25$ °C	P_D	10.8	W
	$T_C = 70$ °C		6.9	
	$T_A = 25$ °C		2.0 ^b	
	$T_A = 70$ °C		1.3 ^b	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 150	°C

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^b	Steady State	R_{thJA}	49	60	°C/W
Maximum Junction-to-Case	Steady State	R_{thJC}	9.4	11.5	

Notes:

a. Package limited.

b. Surface mounted on 1" x 1" FR4 board.

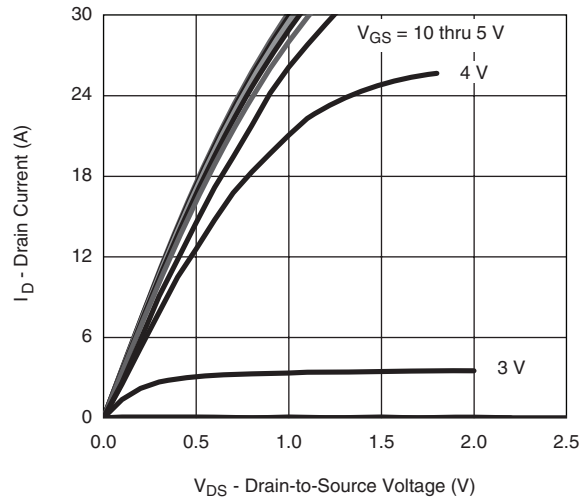
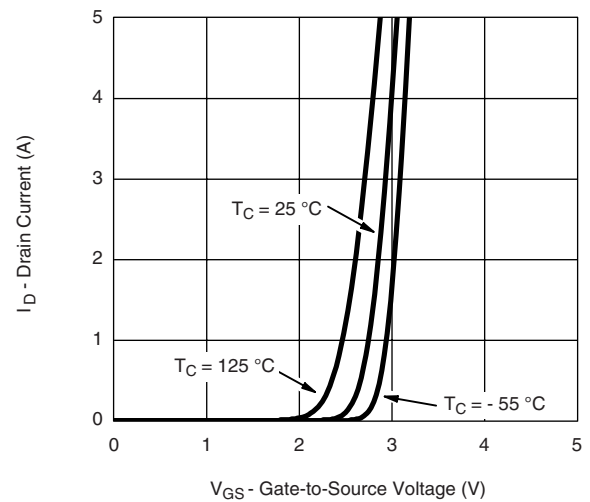
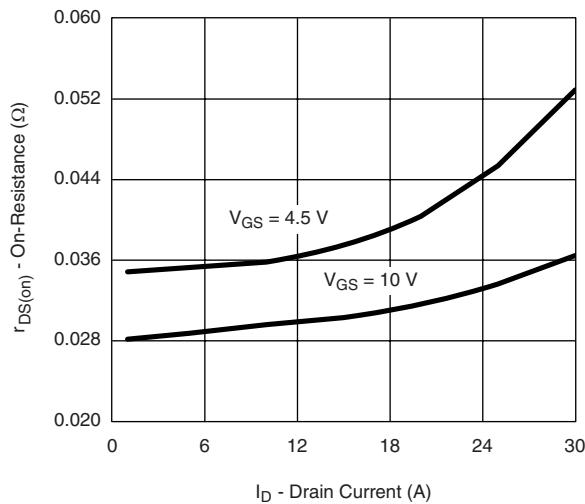
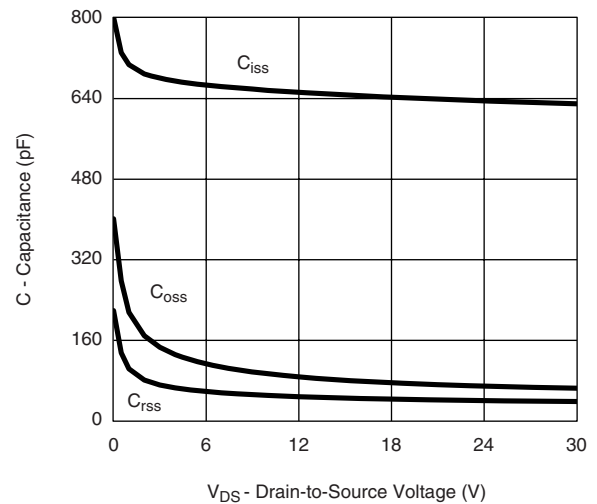
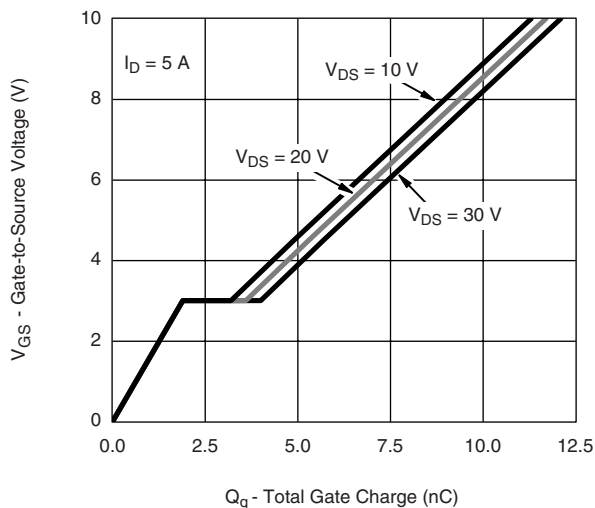
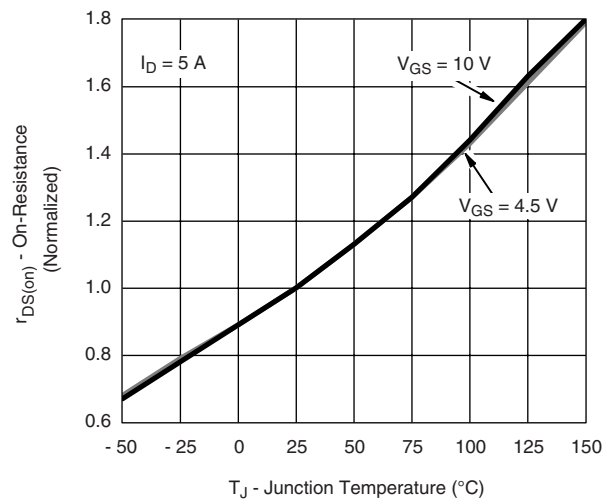
SPECIFICATIONS T _J = 25 °C, unless otherwise noted							
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 1 mA	40			V	
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = 250 μA		44		mV/°C	
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J			- 5.5			
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1.4		2.5	V	
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V			± 100	nA	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 40 V, V _{GS} = 0 V			1	μA	
		V _{DS} = 40 V, V _{GS} = 0 V, T _J = 70 °C			20		
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	10			A	
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = 10 V, I _D = 5 A		0.0305	0.037	Ω	
		V _{GS} = 4.5 V, I _D = 4 A		0.037	0.046		
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 5 A		22		S	
Dynamic ^b							
Input Capacitance	C _{iss}	V _{DS} = 20 V, V _{GS} = 0 V, f = 1 MHz		640		pF	
Output Capacitance	C _{oss}			73			
Reverse Transfer Capacitance	C _{rss}			41			
Total Gate Charge	Q _g	V _{DS} = 20 V, V _{GS} = 10 V, I _D = 5 A		11.7	20	nC	
		V _{DS} = 20 V, V _{GS} = 4.5 V, I _D = 5 A		5.3	9		
					1.9		
					1.7		
Gate-Source Charge	Q _{gs}						
Gate-Drain Charge	Q _{gd}						
Gate Resistance	R _g	f = 1 MHz		2.2		Ω	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 20 V, R _L = 4 Ω I _D ≅ 5 A, V _{GEN} = 4.5 V, R _g = 1 Ω		18	30	ns	
Rise Time	t _r			14	25		
Turn-Off Delay Time	t _{d(off)}			14	25		
Fall Time	t _f			10	20		
Turn-On Delay Time	t _{d(on)}	V _{DD} = 20 V, R _L = 4 Ω I _D ≅ 5 A, V _{GEN} = 10 V, R _g = 1 Ω		9	18		
Rise Time	t _r			11	20		
Turn-Off Delay Time	t _{d(off)}			14	25		
Fall Time	t _f			8	18		
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C			8	A	
Pulse Diode Forward Current ^a	I _{SM}				30		
Body Diode Voltage	V _{SD}	I _S = 2 A		0.805	1.2	V	
Body Diode Reverse Recovery Time	t _{rr}	I _F = 2 A, di/dt = 100 A/μs, T _J = 25 °C		19	30	ns	
Body Diode Reverse Recovery Charge	Q _{rr}			14	25	nC	
Reverse Recovery Fall Time	t _a			13		ns	
Reverse Recovery Rise Time	t _b			6			

Notes:

a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

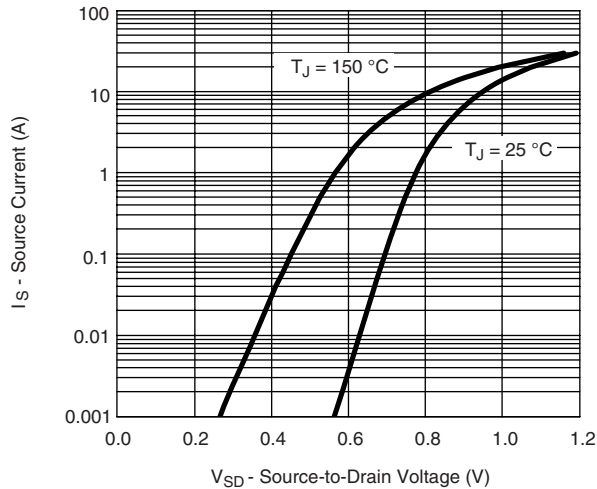
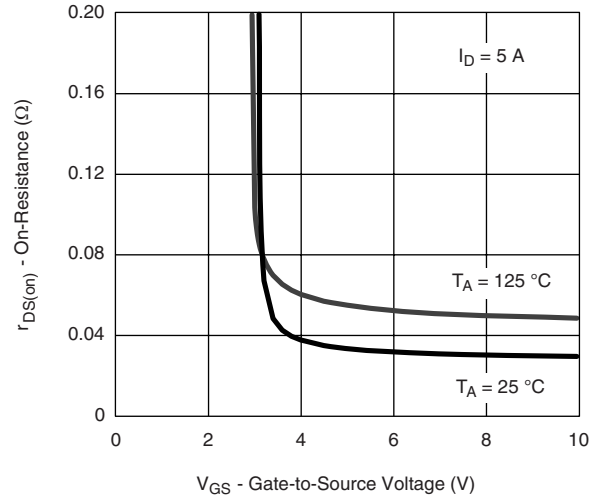
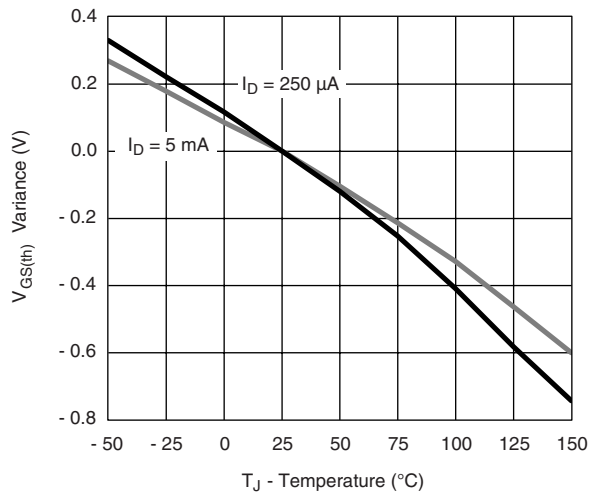
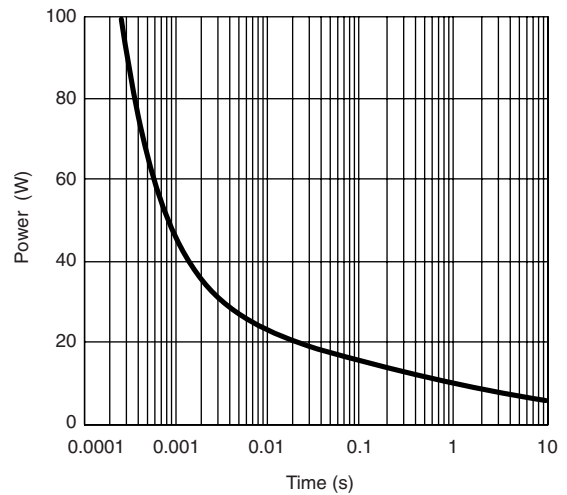
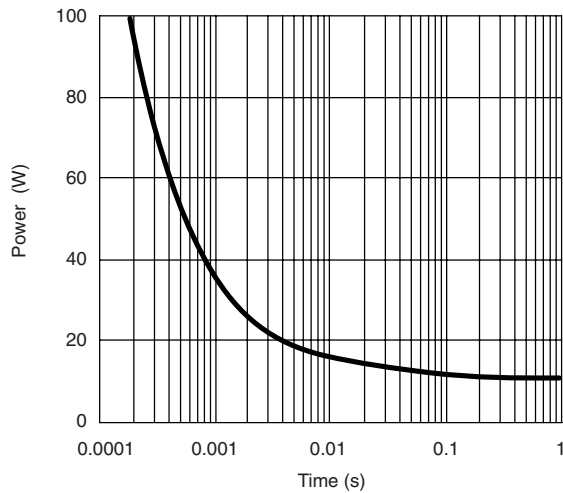
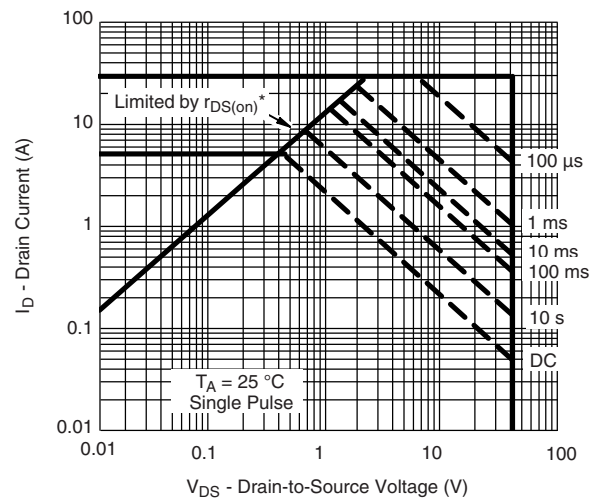
b. Guaranteed by design, not subject to production testing.

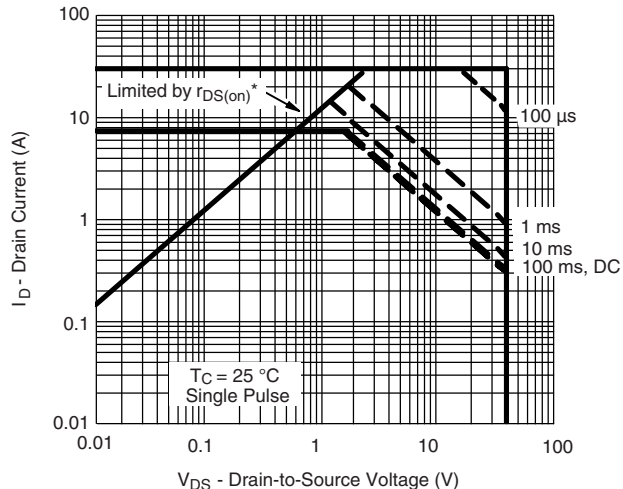
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted**Output Characteristics****Transfer Characteristics****On-Resistance vs. Drain Current****Capacitance****Gate Charge****On-Resistance vs. Junction Temperature**

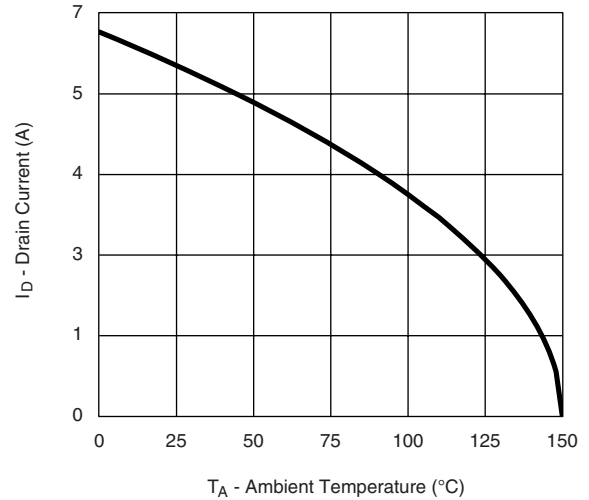
SUD50N04-37P

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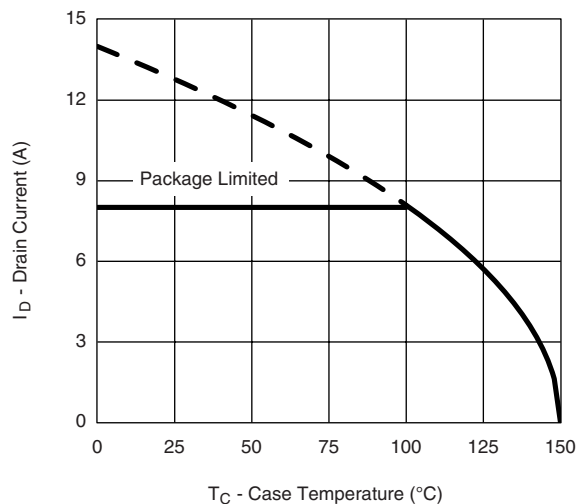
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted**Source-Drain Diode Forward Voltage****On-Resistance vs. Gate-to-Source Voltage****Threshold Voltage****Single Pulse Power, Junction-to-Ambient****Single Pulse Power, Junction-to-Case*** $V_{GS} >$ minimum V_{GS} at which $r_{DS(on)}$ is specified**Safe Operating Area, Junction-to-Ambient**

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

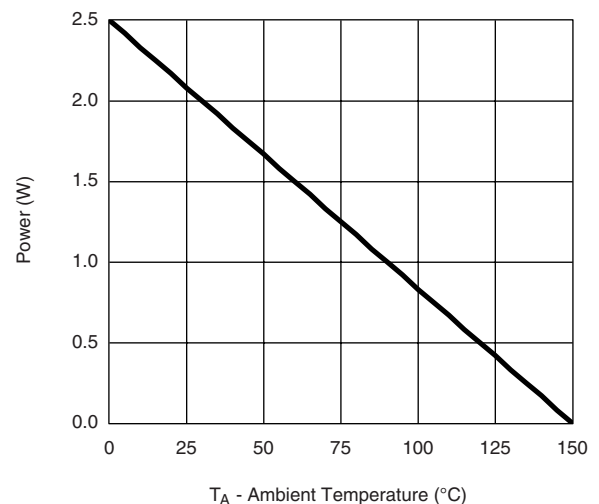
Safe Operating Area, Junction-to-Case



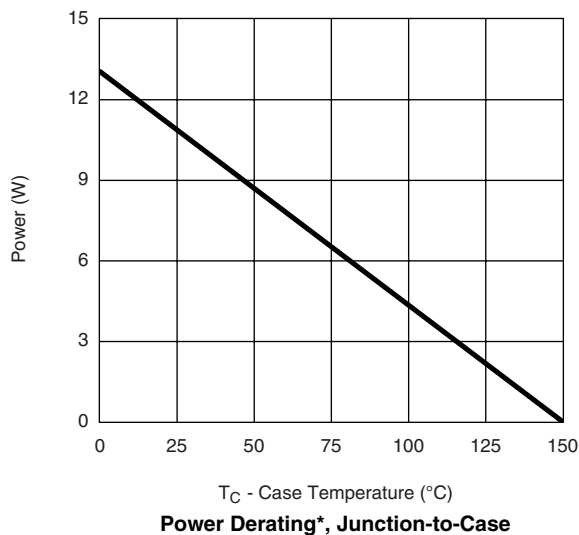
Current Derating*, Junction-to-Ambient



Current Derating*, Junction-to-Case



Power Derating*, Junction-to-Ambient

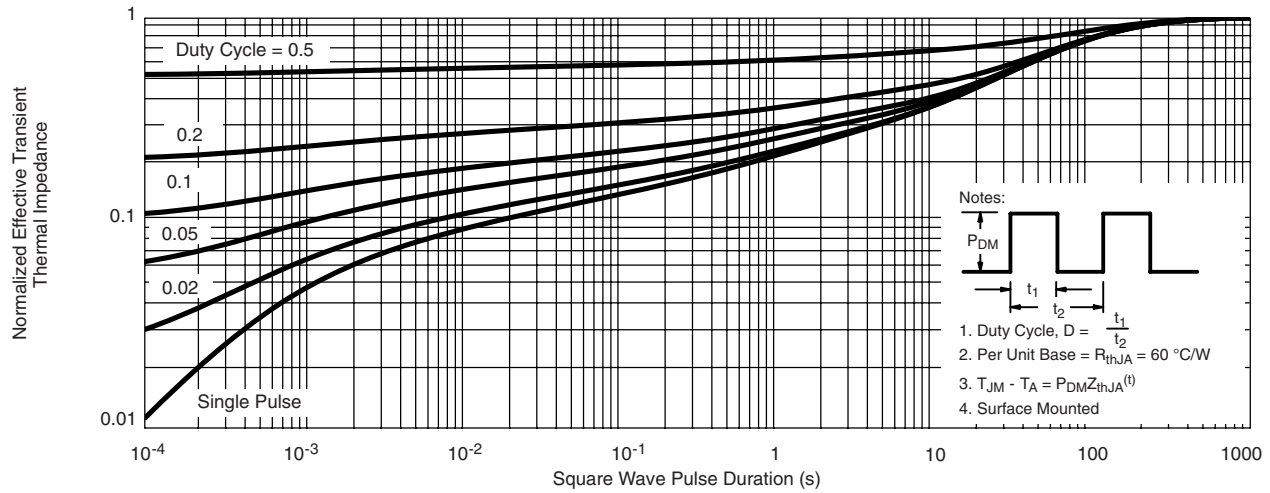
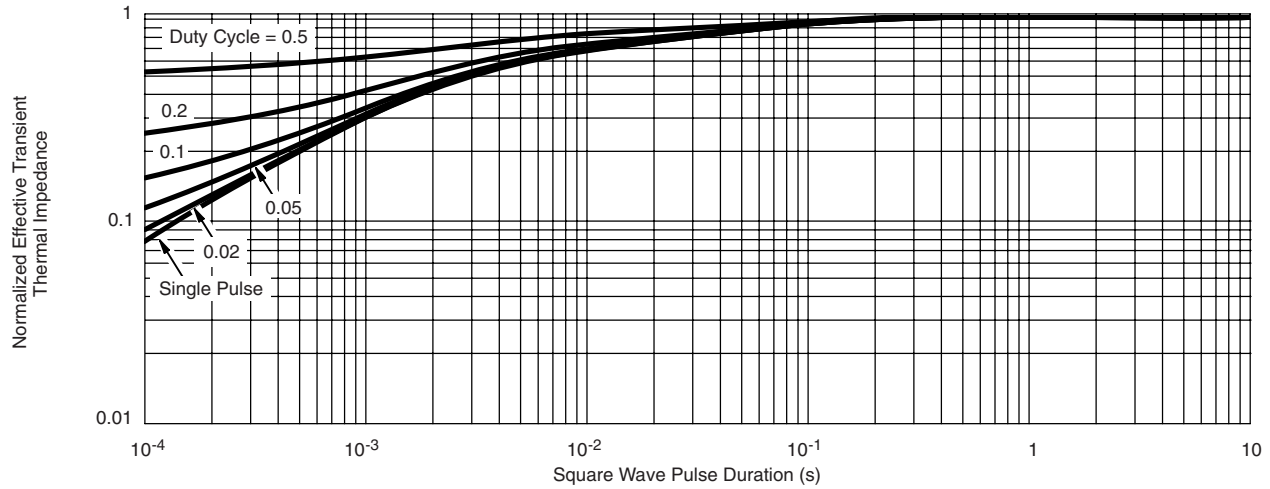


Power Derating*, Junction-to-Case

* The power dissipation P_D is based on $T_{J(max)} = 175^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

SUD50N04-37P

Vishay Siliconix

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted**Normalized Thermal Transient Impedance, Junction-to-Ambient****Normalized Thermal Transient Impedance, Junction-to-Case**

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