M5M5255CP,FP,KP-55LL,-55XL, -70LL,-70XL

262144-BIT (32768-WORD BY 8-BIT) CMOS STATIC RAM

DESCRIPTION

This M5M5255CP,FP,KP is a 262144-bit CMOS static RAMs organized as 32768-words by 8-bits which is fabricated using high-performance 3 polysilicon CMOS technology. The use of resistive load NMOS cells and CMOS periphery result in a high-density and low-power static RAM. M5M5255CP,FP,KP provides two chip select input($\overline{S}_1$,S_2). Stand-by current is small enough for battery back-up application. It is ideal for the memory systems which require simple interface.

FEATURES

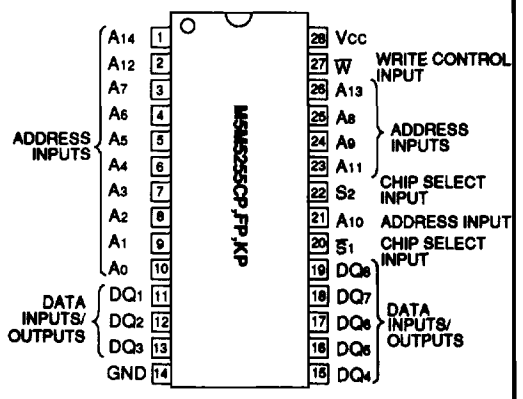
Type name	Access time (max)	Power supply current	
		Active (max)	Stand-by (max)
M5M5255CP,FP,KP-55LL M5M5255CP,FP,KP-70LL	55ns 70ns	60mA (V_{CC}=5.5V)	20 μA (V_{CC}=5.5V)
M5M5255CP,FP,KP-55XL M5M5255CP,FP,KP-70XL	55ns 70ns		5 μA (V_{CC}=5.5V) 0.05 μA (V_{CC}=3V,Typ)

- Single +5V power supply
- No clocks, no refresh
- Data-hold on +2V power supply
- Directly TTL compatible: All inputs and outputs
- Three-state outputs: OR-tie capability
- Simple memory expansion by $\overline{S}_1$, S_2
- Common data I/O
- Low stand-by current ..... 0.05 μA (V_{CC}=3V、typ)
- Package
  - M5M5255CP ..... 28 pin 600 mil DIP
  - M5M5255CFP ..... 28 pin 450 mil SOP
  - M5M5255CKP ..... 28 pin 300 mil DIP

APPLICATION

Small capacity memory units

PIN CONFIGURATION (TOP VIEW)



Outline 28P4(P)
28P2W-C(FP)
28P4Y(KP)

FUNCTION

The operation mode of the M5M5255CP,KP,FP is determined by a combination of the device control inputs $\overline{S}_1$,S_2 and $\overline{W}$. Each mode is summarized in the function table.

A write cycle is executed whenever the low level $\overline{W}$ overlaps with the low level $\overline{S}_1$ and the high level S_2. The address must be set up before the write cycle and must be stable during the entire cycle.

The data is latched into a cell on the trailing edge of $\overline{W}$, $\overline{S}_1$ or S_2, whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained.

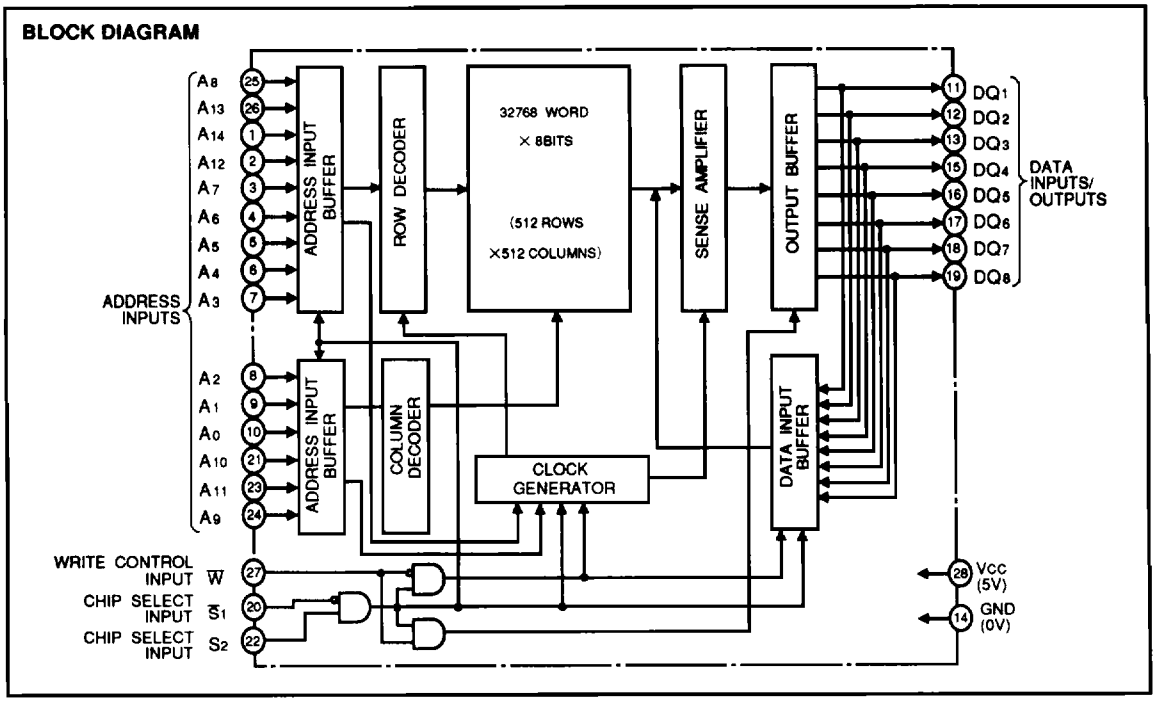
A read cycle is executed by setting $\overline{W}$ at a high level while $\overline{S}_1$ and S_2 are in an active state ($\overline{S}_1$="L", S_2="H").

When setting $\overline{S}_1$ at a high level or S_2 at a low level, the chip is in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by $\overline{S}_1$ and S_2. The power supply current is reduced as low as the stand-by current which is specified as I_{CC3} or I_{CC4}, and the memory data can be held +2V power supply,enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

FUNCTION TABLE

$\overline{S}_1$	S_2	$\overline{W}$	Mode	DQ	Icc
H	X	X	Non selection	High-impedance	Stand-by
L	L	X	Non selection	High-impedance	Stand-by
L	H	L	Write	D_{IN}	Active
L	H	H	Read	D_{OUT}	Active

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	−0.3～7	V
V_I	Input voltage	With respect to GND	−0.3*～Vcc+0.3	V
V_O	Output voltage	With respect to GND	0～Vcc	V
P_d	Power dissipation	Ta=25℃	700	mW
T_{opr}	Operating temperature		0～70	℃
T_{stg}	Storage temperature		−65～150	℃

* −3.0V in case of AC (Pulse width≦30ns)

DC ELECTRICAL CHARACTERISTICS (Ta=0～70℃, Vcc=5V±10%, unless otherwise noted.)

Symbol	Parameter	Test conditions		Limits Min	Limits Typ	Limits Max	Unit
V_{IH}	High-level input voltage			2.2		Vcc+0.3V	V
V_{IL}	Low-level input voltage			−0.3*		0.8	V
V_{OH}	High-level output voltage	I_{OH}=−1mA		2.4			V
		I_{OH}=−0.1mA		Vcc−0.5V			
V_{OL}	Low-level output voltage	I_{OL}=2mA				0.4	V
I_I	Input leakage current	V_I=0～Vcc				±1	μA
I_O	Output leakage current	$\overline{S}_1$=V_{IH} or S_2=V_{IL}, $V_{I/O}$=0～Vcc				±1	μA
I_{CC1}	Active supply current (AC,MOS level)	$\overline{S}_1$≦0.2V, S_2≧Vcc−0.2 Other inputs≦0.2V or≧Vcc−0.2V Output open Min.cycle	55ns		35	55	mA
			70ns		30	50	
I_{CC2}	Active supply current (AC,TTL level)	$\overline{S}_1$=V_{IL} or S_2=V_{IH} Other inputs=V_{IH} or V_{IL} Output open Min.cycle	55ns		40	60	mA
			70ns		35	55	
I_{CC3}	Stand-by supply current	1) S_2≦0.2V, Other inputs=0～Vcc 2) $\overline{S}_1$≧Vcc−0.2V, S_2≧Vcc−0.2V, Other inputs=0～Vcc	-LL			20	μA
			-XL		0.1	5	μA
I_{CC4}	Stand-by supply current	1) S_2=V_{IL}, 2). $\overline{S}_1$=V_{IH}, S_2=V_{IH} Other inputs=0～Vcc				3	mA

* −3.0V in case of AC (Pulse width 30ns)

CAPACITANCE (Ta=0～70℃, Vcc=5V±10%, unless otherwise noted.)

Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
C_I	Input capacitance (Ta=25℃)	V_I=GND, V_I=25mVrms, f=1MHz			6	pF
C_O	Output capacitance (Ta=25℃)	V_O=GND, V_O=25mVrms, f=1MHz			8	pF

Note1: Direction for current flowing into IC is indicated as positive. (no mark)
2: Typical value is Vcc=5V, Ta=25℃.
3: C_I, C_O are periodically sampled and are not 100% tested.

AC ELECTRICAL CHARACTERISTICS (Ta=0～70℃, Vcc=5V±10%, unless otherwise noted.)

(1) MEASUREMENT CONDITIONS

Input pulse level ..... V_{IH} = 2.4V, V_{IL} = 0.6V
Input rise and fall time 5ns
Reference level ..... V_{OH} = V_{OL} = 1.5V
Transition is measured ±500mV from steady state voltage. (for t_{en}, t_{dis})
Output loads ..... Fig.1, C_L = 50pF
C_L = 5pF (for t_{en}, t_{dis})

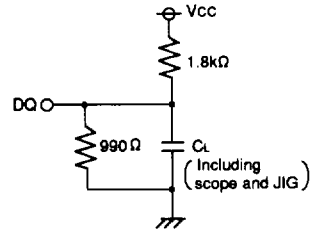


Fig.1 Output load

(2) READ CYCLE

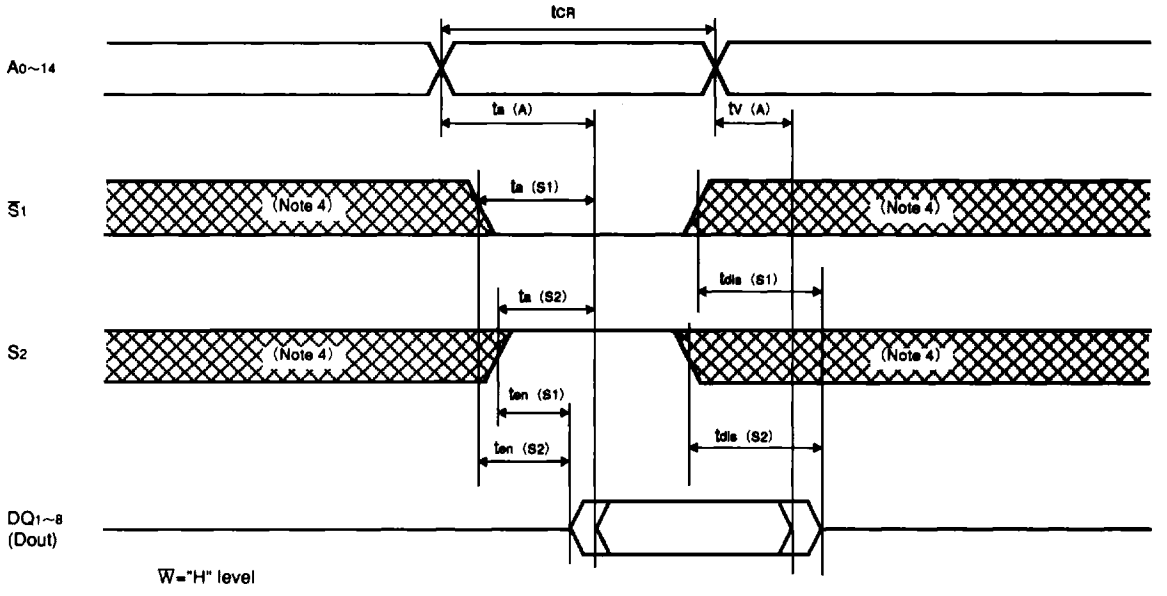
Symbol	Parameter	Limits				Unit
		M5M5255C-55LL, -55XL		M5M5255C-70LL, -70XL		
		Min	Max	Min	Max	
t_{CR}	Read cycle time	55		70		ns
$t_{a(A)}$	Address access time		55		70	ns
$t_{a(S1)}$	Chip serect 1 access time		55		70	ns
$t_{a(S2)}$	Chip serect 2 access time		55		70	ns
$t_{dis(S1)}$	Output disable time after $\overline{S_1}$ high		20		25	ns
$t_{dis(S2)}$	Output disable time after S_2 low		20		25	ns
$t_{en(S1)}$	Output enable time after $\overline{S_1}$ low	5		5		ns
$t_{en(S2)}$	Output enable time after S_2 high	5		5		ns
$t_{v(A)}$	Data valid time after address change	10		10		ns

(3) WRITE CYCLE

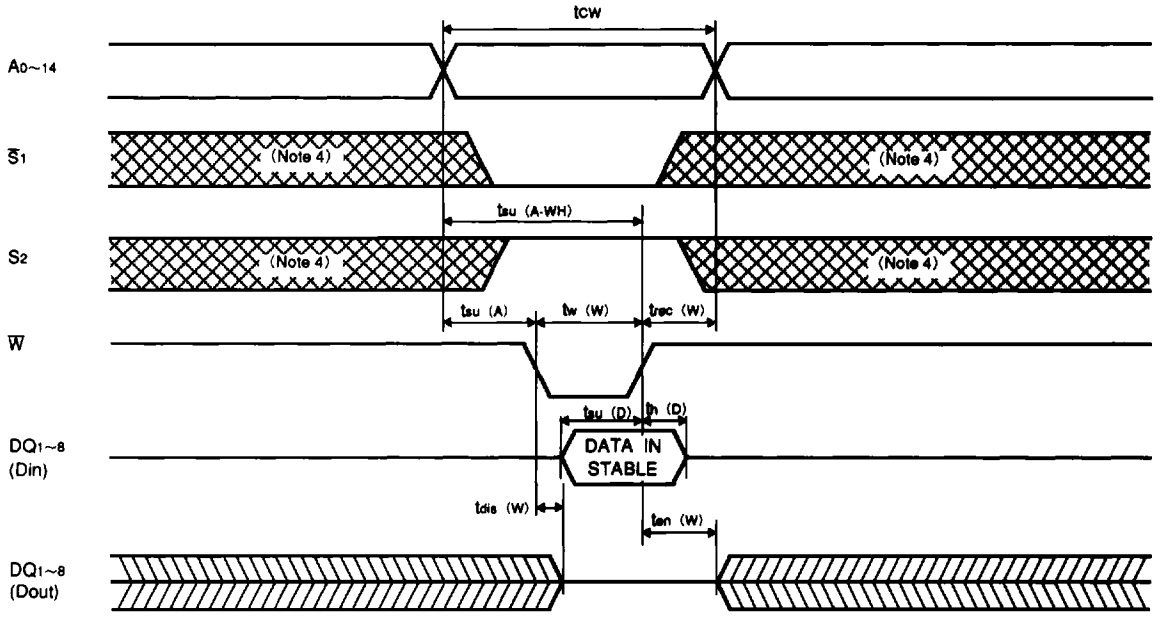
Symbol	Parameter	Limits				Unit
		M5M5255C-55LL, -55XL		M5M5255C-70LL, -70XL		
		Min	Max	Min	Max	
t_{CW}	Write cycle time	55		70		ns
$t_{w(W)}$	Write pulse width	45		55		ns
$t_{su(A)}$	Address set up time	0		0		ns
$t_{su(A-WH)}$	Address set up time with respect to $\overline{W}$ high	50		65		ns
$t_{su(S1)}$	Chip select 1 set up time	50		65		ns
$t_{su(S2)}$	Chip select 2 set up time	50		65		ns
$t_{su(D)}$	Data set up time	25		30		ns
$t_{h(D)}$	Data hold time	0		0		ns
$t_{rec(W)}$	Write recovery time	0		0		ns
$t_{dis(W)}$	Output disable time after $\overline{W}$ low		20		25	ns
$t_{en(W)}$	Output enable time after $\overline{W}$ high	5		5		ns

(4) TIMING DIAGRAMS

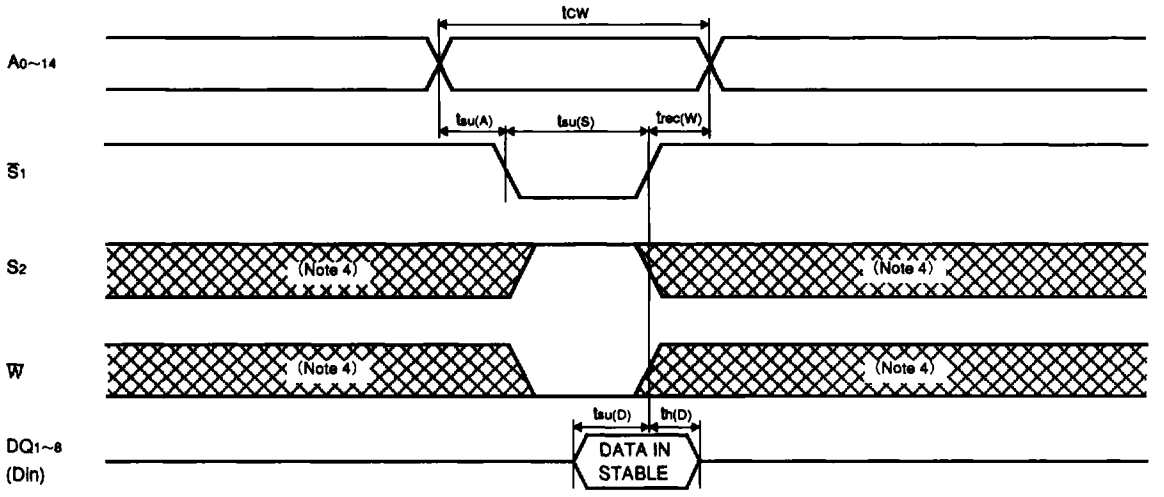
Read cycle



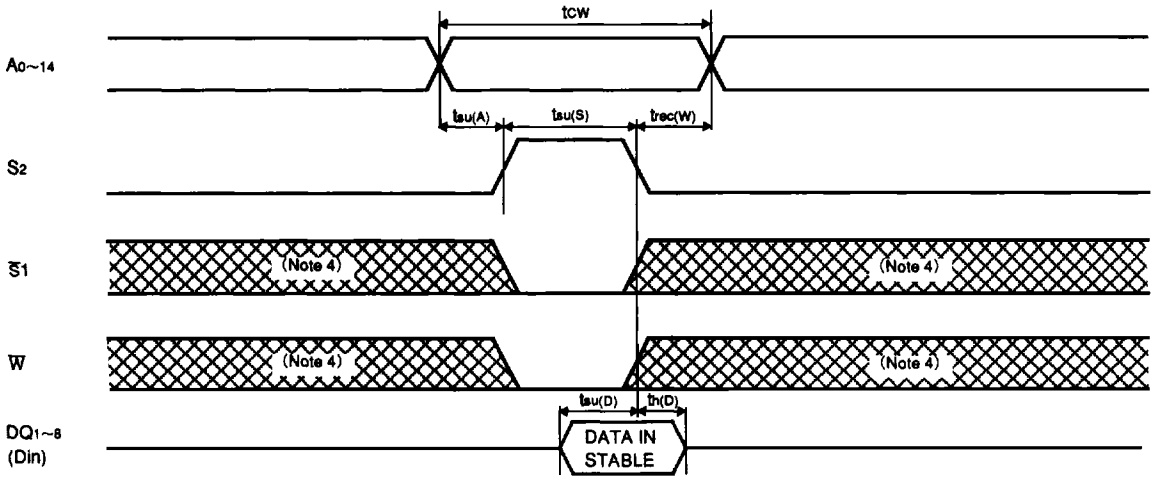
Write cycle (W control)



Write cycle ($\overline{S}_1$ control)



Write cycle (S_2 control)



Note 4: Hatching indicates the state is don't care.
5: Writing is executed while S_2 high overlaps $\overline{S}_1$ and $\overline{W}$ low.
6: If $\overline{W}$ goes low simultaneously with or prior to $\overline{S}_1$ low or S_2 high, the output remains in the high-impedance state.
7: Don't apply inverted phase signal externally when DQ pin is in output mode.
8: ten,tdis are periodically sampled and are not 100% tested.

POWER DOWN CHARACTERISTICS

(1) ELECTRICAL CHARACTERISTICS (Ta=0~70℃, Vcc=5V±10%, unless otherwise noted.)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
$V_{CC(PD)}$	Power down supply voltage			2			V
$V_{I(\overline{S}1)}$	Chip select input $\overline{S}_1$	2.2V≦$V_{CC(PD)}$		2.2			V
		2V≦$V_{CC(PD)}$≦2.2V			$V_{CC(PD)}$		
$V_{I(S2)}$	Chip select input S_2	4.5V≦$V_{CC(PD)}$				0.8	V
		$V_{CC(PD)}$<4.5V				0.2	
$I_{CC(PD)}$	Power down supply current	Vcc=3V Other inputs=0~3V 1) S_2≦0.2V or 2) $\overline{S}_1$≧Vcc−0.2V, S_2≧Vcc−0.2V	-LL			10*	μA
			-XL		0.05	2**	μA

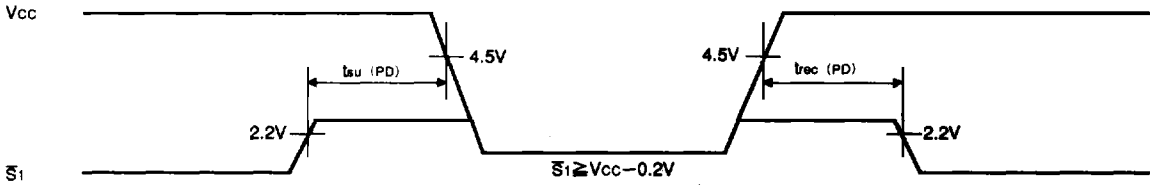
* Ta=25℃, $I_{CC(PD)}$=1 μA(max).
** Ta=25℃, $I_{CC(PD)}$=0.2 μA(max).

(2) TIMING REQUIREMENTS (Ta=0~70℃, VCC=5V±10%, unless otherwise noted.)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{su(PD)}$	Power down set up time		0			ns
$t_{rec(PD)}$	Power down recovery time		t_{CR}			ns

(3) POWER DOWN CHARACTERISTICS

$\overline{S}_1$ control mode



S_2 control